

SourcePoint

Getting Started Guide for the

AAEON UP Xtreme i11

Revision 2.3



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Revision History

| Revision Number | Description | Date |
|------------------------|--|-------------------|
| 1.0 | Original document, describes v0000 | November 28, 2021 |
| | board support | |
| 2.0 | Added content for new support of v0001 | May 30, 2022 |
| | (with the Type-C connector removed) | |
| | AAEON UP Xtreme i11 board | |
| 2.1 | Updated for WinDbg support and other | December 3, 2023 |
| | perfective changes | |
| 2.2 | Update for beta release SourcePoint | March 31, 2024 |
| | 7.12.52 | |
| 2.3 | Production release documentation for | May 5, 2024 |
| | 7.12.53. | |





Welcome!

Thank you very much for your SourcePoint purchase! We appreciate you acquiring our best-in-class debugger, and hope you enjoy using it. We strive to deliver the most powerful, easy-to-use and polished product as possible. So, please feel free to share your feedback directly at our support site at <u>https://www.asset-intertech.com/support/</u>, or via your favorite social media outlet.

As with any new tool, mastering SourcePoint takes an investment in terms of time and effort. JTAG-based debug is a fairly specialized area, and low-level "on the metal" firmware development on x86 platforms is even more so. So, in your use of the tool, you may encounter behavior that seems non-intuitive or even wrong. You may be encountering a tool corner case, a limitation inherent in JTAG or DCI, or even a bug. If so, try a few different options as may be referenced in the <u>Troubleshooting</u> section of this Guide, and if it persists, give us a call. We are happy to support you.



Boards and Cables

The board covered in this document is the AAEON UP Xtreme i11 board, based upon the Intel Tiger Lake CPU.

The Tiger Lake boards come in four flavors: Celeron, i3, i5 and i7. As of this writing, all boards are suited for Windows debugging. The Celeron boards is the least expensive and supports all the latest Intel debug and trace features such as Intel Processor Trace (Intel PT), Intel Trace Hub, Architectural Event Trace (AET), and others.





WARNING:

Do <u>NOT</u> plug a regular USB cable into the target and attempt to use DCI. Specialty cables, with VBUS snipped, are required; using a regular USB cable may possibly fry your target, or worse.

The main source to purchase the specialty DCI cable needed for SourcePoint debugging is ASSET InterTech. This target has its Type-C port enabled for DCI. If you have a debug host with a Type-A port, you'll need to purchase the part # ITPDCIAMCM1MU (1.0 meter) cable. The longer 1.8-meter ITPDCIAMCM2MU cable will work as well. If your host has a Type-C port, purchase the ITPDCIC2CD2U1M. Using Type-A/C hubs have been seen to work, but are not warranted. Type A/C adapters have been seen <u>not</u> to work.

Contact your ASSET representative to obtain the cable needed for your configuration.



BIOS Settings

The AAEON UP Xtreme i11 boards come equipped with an AMI Aptio BIOS that is based upon typical Intel Customer Reference Board (CRB) BIOS.

Luckily, the platform comes with all the necessary hardware hooks and firmware straps to support Intel Direct Connect Interface (DCI) out of the box.

The USB Type C port on the board is the port of interest:



There are only a few BIOS settings to change for the board to work with SourcePoint and DCI: disable the board's Watchdog Timer (WDT), ensure that Windows doesn't wake it up, and turn on the Intel Trace Hub.

Go into the BIOS Boot menu (this is accomplished by rebooting the board, at the same time holding down the F7 key, and you'll be promoted for the password for the "CRB Advanced" BIOS menu. Note that CRB is Customer Reference Board, an Intel reference:

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The password is upassw0rd.

And that is a number "zero" (0) in the password, not the letter "o".

Enter Setup, and use the arrow key to move over to the Boot menu. and set WDT Timer -> Disabled. If you don't, run-control will be successful, but the board will power-cycle every 30 seconds; putting a real crimp in your debugging!

| Main Advanced | Aptio Setup – AMI Chipset Security Boot Sav | e & Exit |
|--|--|---|
| Boot Configuratio | n | Enables or disables Quiet Boot option |
| Quiet Boot | [Enabled] | |
| WDT Timer | [Disabled] | |
| FIXED BOOT ORDER Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 | Priorities [USB Hard Disk] [USB CD/DVD] [USB Key] [USB Floppy] | ++: Select Screen |
| Boot Option #5 | [USB Lan] | ↑↓: Select Item |
| Boot Option #6 | [Hard Disk] | Enter: Select |
| Boot Option #7 | [NVME:Windows Boot Manager (KINGSTON OM8SEP4256Q-AO)] | +/-: Change Opt. F1: General Help F2: Previous Values |
| Boot Option #8 | [CD/DVD] | F3: Optimized Defaults |
| Boot Option #9 | [Network] | ▼ F4: Save & Exit ESC: Exit |
| | Version 2.21.1278 Copyright | (C) 2021 AMI |

There is another setting within the CRB Advanced menu to Disable the TCO Timer from being re-enabled by Windows; this is set to Disabled by default when shipped from AAEON, but if you run into issues with run-control stability, you might want to check this:

CRB Setup > CRB Chipset > PCH-IO Configuration > Enable TCO Timer **must be set to** Disabled.



| Main | Aptio Setup – AMI | | | |
|---|--|---|--|--|
| Compatible Revision ID Legacy IO Low Latency PCH Cross Throttling PCH Energy Reporting LPM S0i2.0 LPM S0i2.1 LPM S0i2.2 LPM S0i3.0 LPM S0i3.1 LPM S0i3.2 | [Disabled] [Disabled] [Enabled] [Enabled] [Enabled] [Enabled] [Enabled] [Enabled] [Enabled] [Enabled] | Enable/Disable TCO timer. When disabled, it disables PCH ACPI timer, stops TCO timer, and ACPI WDAT table will not be published. | | |
| LPM SOIS.3 LPM SOIS.4 C10 Dynamic threshold adjustment IEH Mode Enable TCO Timer Enable Timed GPIO0 Enable Timed GPIO1 | [Enabled] [Enabled] [Disabled] [Enabled] [Enabled] [Enabled] | <pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre> | | |
| Version 2.21.1278 Copyright (C) 2021 AMI | | | | |

Finally, go to CRB Setup > CRB Advanced > Debug Settings and set
Platform Debug Consent to Enabled (USB2 DbC):

| Main | Aptio Setup – AMI | | | |
|---|---|--|--|--|
| Debug Settings Kernel Debug Serial Port Kernel Debug Patch Platform Debug Consent VT-d Debug Settings Advanced Debug Settings | [Legacy UART] [Disabled] [Enabled (USB2 DbC)] | To 'opt-in' for debug, please select 'Enabled' with the desired debug probe type. Enabling this BIOS option will override other debug-related BIOS options. ++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit | | |
| Version 2.21.1278 Copyright (C) 2021 AMI | | | | |





Remember to do a "Save & Exit" with the F4 key after the changes! Otherwise, your changes won't be saved.

Power Tip: We have observed that, on very rare occasions, the saved settings that you've made will be undone by a "BIOS restore". If you begin to observe strange effects, like autonomous platform resets while in run-control mode, check to ensure that the changes you've made have not been undone.

You are now ready to test your connection, and then launch SourcePoint and begin debugging.



DbCStatus.exe: Red is Bad, Green and Yellow are Good

Luckily, there is a convenient application in the SourcePoint install directory that will tell you that the DCI driver is successfully installed on your computer, and it is possible to make a connection between SourcePoint and the target.

Navigate to C:\Program Files (x86)\Arium\SourcePoint 7.12.53 (where 53 is your current SourcePoint release), and launch the DbCStatus.exe. You should see the red ball, indicating that there is no connection:

| DbC Connection Status | ; | |
|-----------------------|---------------|-------|
| Connection status: | No connection | |
| DCI driver version: | 1.10.0.0 | |
| | | Close |

Ensure that the Type-C cable is firmly connected to both the host and target, and power up the UP Xtreme i11. In a moment the ball should turn green:

| DbC Connection Status | | |
|-----------------------|----------|-------|
| Connection status: | USB 2.0 | |
| DCI driver version: | 1.10.0.0 | |
| | | Close |

Let the platform boot to the UEFI shell. Congratulations! You have a working DCI connection. It's smooth sailing from here.

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Power Tip: If you are using SourcePoint WinDbg for debugging this board, and have Windows already installed, there may be situations where you want to go to BIOS setup before booting all the way up to Windows. In this case, press F7 after powering on to stop at the BIOS setup.

Power Tip: The very latest version of the Celeron board will not power up successfully after a power cycle. Here's the workaround:

- 1. Apply power back to the target. You will see that it doesn't power up, and the blue light does not light up on the power switch.
- 2. Unplug the DCI cable from the Type-C plug.
- 3. The board will start to power up. Press F7 and you will stop at the UEFI menu password screen.
- 4. Hot Plug the Type-C cable back in. Your DCI connection will be restored, and you will see the DbCStatus ball turn green. You may continue your Windows debugging session.



Getting Started with SourcePoint

When you launch SourcePoint for the first time, you will see the main screen, mostly gray:

| 8 SourcePoint | | | | | | - 0 | × |
|---|---|-----------|---------|-----------|----------------|------|-----|
| File Edit View Processor Options Window Help | | | | | | | |
| 19 19 19 19 19 19 19 19 19 19 19 19 19 1 | ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ | 8 B B A A | | © 🕒 🔪 🔛 🔳 | IP 🔍 🖋 👀 🔍 🖫 🇖 | 回口並回 | # B |
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| | | | | | | | |
| F1:Help, F5:Go, Shift+F5:Stop, F8:Step Into, F10:Step Over, Shift+F12:Reset | | | | No power | | | |

SourcePoint uses Projects (files with suffix .prj) as containers for your debugging session. You can create as many Projects as you want, with all your own preferences saved. Often, once you have the SourcePoint Project configured to your liking, you'll save it and use it repeatedly during your separate debugging sessions. Other users may wish to save a separate Project for each separate debugging session. That's really a matter of user preference and what you're debugging – it's your choice.

Now it's time to create the Project. Under File > Project... select New Project:





You'll be presented with the New Project Wizard (NPW). The emulator connection should be via DCI:





| New Project Wizard: Welcome | × |
|---|------|
| Welcome to the New Project Wizard | |
| This wizard helps you: | |
| - Select or add an emulator connection. | |
| - Create a new project file. | |
| DCI, DCI · Add/Edit | |
| Select an emulator connection and click Next. | |
| < Back Next > Cancel | Help |

After hitting Next, you'll be prompted for the Project Name, Location to store the Project, and the location of the Target Configuration file:



| New Project Wiz | zard: Project File | × |
|----------------------------|------------------------------|---|
| Project file File name: | myproject | |
| Target conf | iguration file Browse Browse | |
| | Identify Target | |
| | | |
| | < Back Next > Cancel Help | |

Note that the Target Configuration (TC) files located in C: \My

Documents\Arium\Targets are used in conjunction with the jtag-devices.xml file to define the specific silicon and SourcePoint settings necessary to ensure a successful DCI connection.

For the UP Xtreme i11 boards, custom TC files have been created, so you shouldn't do an Identify Target to automatically select the TC file of interest. Rather, manually select the specific TC file that is customized for this target (TGL\UP-Xtremei11_DbC.tc) and hit Open:



| 🛞 Open | | | × |
|-----------------------|--|---|---------------------------------------|
| ← → ∽ ↑ 🖡 « Sour | cePoint-IA_7.12.20 > Targets > TGL > TGL-U | ע גע אין אין ער אין | h TGL-U |
| Organize 🔹 New folder | | | · · · · · · · · · · · · · · · · · · · |
| iCloud Drive * ^ | Name | Date modified | Туре |
| Documents | TGL.tc | 10/29/2021 4:15 AM | TC File |
| 📙 Intel | TGL_DbC.tc | 10/29/2021 4:15 AM | TC File |
| Screenshots | UP-Xtreme-i11_DbC.tc | 11/19/2021 2:10 AM | TC File |
| SourcePoint-IA_7 | | | |
| 😽 Dropbox | | | |
| OneDrive - Person | | | |
| 🗢 This PC | | | |
| 🗊 3D Objects | | | |
| 🔜 Desktop | | | |
| 🖆 Documents 🗸 🗸 | < Comparison of the second sec | | > |
| File nam | e: UP-Xtreme-i11_DbC.tc | Target ConfOpen | iguration Files (*.tc) V |

Then, your screen should look something like this, after you've replaced the default Project file File name with your preferred name (in this instance, My Tiger Lake Project):



| New Project Wi | zard: Project File | × |
|----------------|--|------|
| Project file | | |
| File name: | My Tiger Lake Project | |
| Location: | C:\Users\alans\Documents\Arium\SourcePoint-IA_ Browse | |
| Target conf | figuration file | |
| C:\Users\a | alans\Documents\Arium\SourcePoint-IA_7.12.15\Ta Browse | |
| | Identify Target | |
| | | |
| | | |
| | | |
| | | |
| | < Back Next > Cancel | Help |

Hit Next, then Finish, and SourcePoint should successfully connect to the target. You should see "JtagTest: Successful operation" followed by "Configuration state: Connected" in the Status bar at the bottom left:





Now the fun part begins. Click on the buttons at the top to set up the Viewpoint, Code, Command, Registers and other windows to your own preference. Move the windows around and resize them to take best advantage of your available screen real estate. You can right-click in the title bar of each window to change its type and, for example, to dock the window to the bottom, right side, etc.



A sample layout is below:



| 🖀 SourcePoint v7.12.0 [DCI] - TigerLake - C:\Users\alans\D | ocuments\Arium\SourcePoint-IA_7.12.15\My Tiger Lake Project.prj (safe mode) | | | | - 0 | × |
|--|---|----------------|-------------------|---|-------------|----------|
| File Edit View Processor Options Code Window Help | | | | | | |
| 월 📽 🔛 😂 🔛 🚔 🔛 🚅 | 🥨 Load UEFI Macros 🥵 🥨 👹 🖶 📔 🔐 🗊 🗊 🗊 💼 🚔 🥵 😑 Breakpoints 🕀 Code 🕨 Command 📓 | Loa 🎹 Memory | IP Registe | rs 🔍 Symbols 🧈 Trace I | 0 Viewpoint | Q. Watch |
| | | 5_ , | 3 | | | Ý 💡 |
| | | | | | | • |
| Code (P0*) Tracking IP | | OViewpoint | | | | |
| 🕼 No Data Available - Processor not av | ailable | Name | | Description | | Status |
| | | * PO | TigerLak | e | Running | |
| | | • P1 | TigerLak | e | Running | |
| | | ◇ P2 | TigerLak | e | Running | |
| | | • P3 | TigerLak | e | Running | |
| | | | | | | |
| | | | | | | · · · |
| | | TP Concret Rev | | | | |
| | | General Ke | gisters (PU) | | | |
| | | ■IA-32 | Name | Value | 0 | |
| | | Intel 64 | RAX | 222222222222222222222222 | r 2 | |
| | | General | - DCV | 22222222222222222222222 | 7 2 | |
| | | Floating | RDX | 333333333333333333333 | ? | |
| | | Segment | RBP | 2222222222222222222 | ? | |
| | - | Control | RSI | 222222222222222222222222222222222222222 | ? | |
| | | Debug | RDI | ??????????????????????????????????????? | ? | |
| Unknown V P Source V Go (| Cursor Set Break Track IP View IP Refresh | MMX | RSP | ??????????????????????????????????????? | ? | |
| | | YMM - SI | R8 | 222222222222222222222222222222222222222 | ? | |
| | 📾 Breakpoints 🗖 🗖 🔀 | YMM - D | R9 | 222222222222222222222222222222222222222 | ? | |
| | Identifier Address Attributes | YMM - In | R10 | ??????????????????????????????????????? | ? | |
| | Address Address | MSR | R11 | ??????????????????????????????????????? | ? | |
| | | User | R12 | ??????????????????????????????????????? | ? | |
| | | | R13 | ??????????????????????????????????????? | ? | |
| | | | R14 | 222222222222222222222222222222222222222 | 2 | |
| | Edit Add Remove Remove All Enable Disable All | | R15 | 20000 | <i>;</i> | |
| | | - | CS DR | 2222 | | |
| 🗟 Log | | | 99 | 2222 | | _ |
| Date Time Component | Message | 1 | ES | 2222 | | |
| 11/16/2021 17:11:49.685 RefillDisplay | YList Could not refill the display due to a lack of known code position | d | FS | 2222 | | |
| | | | GS | ???? | | |
| | | | RIP | ??????????????????????????????????????? | ? | |
| | | < > | RFLAGS | ??????????????????????????????????????? | ? | |
| | | | | | | |
| | | | _ | | _ | |
| Command | | | | | | |
| Configuring Devices | | | | | | ^ |
| Connecting | | | | | | |
| Loading Command Language Extensions: C | :\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\aa\aaextend.mac | | | | | |
| PO> | | | | | | |
| 50> | | | | | | |
| | | | | | | |
| | | | | | | |
| 1 | | | | | | ~ |
| F1:Help, F5:Go, Shift+F5:Stop, F8:Step Into, F10:Step Over | r. Shift+F12:Reset | P0 1F: Ri | unning | | Halt Mode | |

Power Tip: the window layout can be saved as a separate file. That way, when you create a new Project, you can just Load the layout file separately, without having to create and move the windows around again. Choose File > Layout > Save Layout... to create a .lyt file, and then do a Load Layout... to save yourself time every time you create a new Project.

Power Tip: Exploring Options > Preferences... and some of the other menu items may give you some more labor-saving ideas. For instance, I like to ensure that both Load last project on startup and Save project on exit are disabled. This gives me more control on entry and exit from the application:



| Preference | S | | | | | | | | × |
|------------|--------------|-----------------|-----------|-------------|------------|------------|---------|--------|---|
| General | Emulator | Breakpoints | Code | Memory | Program | IPC | Colors | | |
| Project | | | | | | | | | |
| Lo | ad last pro | ject on startu | D | | | | | | |
| 🖂 Pr | ompt befor | e automaticall | y saving | project | | | | | |
| 🗌 Sa | ve project | on exit | | | | | | | |
| Lo | ad target o | onfiguration fi | le when | project loa | aded | | | | |
| Fi | le name: | C:\Users\alar | is\Docun | nents\Ariur | m\SourcePo | oint-IA_7 | .12.1 | Browse | |
| | | | | | | | | | |
| User ir | terface | | | | | | | | |
| ⊡ Sł | now advanc | ed configurati | on settir | ngs | Preferre | ed editor: | notepad | - k | |
| 🖂 Sł | now tooltips | 5 | | | | | | | |
| □ Ti | med windo | w refresh | | | | | | | |
| int | erval: 10 | second | S | | | | | | |
| | | | | | | | | | |
| | | | | Γ | OK | | Cancel | Help | |
| | | | | L | UK | | Cancer | Tielp | |

Others prefer to check Save project on exit. It's a matter of preference.

This is a good point to do a Project > Save Project... That way, you don't have to start all over, if for some reason your project gets messed up.

At this point, you are ready to fully begin your debug session. Many of the operations can be accessed via the toolbar at the top of the screen. You can issue a Stop on the target, Step Into, Reset and halt at the reset vector, set some breakpoints, Go to the breakpoint, and so on. Use the buttons at the top, in the SourcePoint Icon toolbar section, to initiate these actions. Use the function keys (i.e. F8 for Step Into) as you gain experience.



| SourcePoint v7.12.0 [DCI] - TigerLake - C.\Users\alans\Documents\Arium\SourcePoint-IA.,7.12.15\My Tiger Lake Project.prj | | | | | |
|--|----------------|---------------------|---|-------------|---------|
| File Edit View Processor Options Code Window Help | | | | | |
| 👺 🎬 🔚 🖆 🔛 🎼 🚱 🗰 🥵 🐝 🐝 📾 📾 🖬 🖬 🖬 🖬 👘 🖬 👘 👘 👘 👘 👘 👘 👘 👘 👘 👘 👘 👘 👘 | og 🎹 Memory | IP Registers | Symbols Irace | 0 Viewpoint | Q Watch |
| | , , | 3 | - / - | | Ý 💡 |
| | | | | | |
| GCode (P0*): (64-bit) Tracking IP 00000000000000 - FFFFFFFFFFFEL | COViewpoint | | | | - 23 |
| 0000000640D200FL 498B80C0000000 MOV RAX,QWORD PTR [R8]+000000c0 A | Name | D | escription | a. 1 | Status |
| 0000000640D2016L BBCA MOV ECX, EDX | * P0 | TigerLake | | Stopped | |
| 0000000640D201BL CLEI02 SAL ECA, 2 0000000640D201BL SB0001 MOV EX DWORD PTP [PCV1[Day] | • P1 | TigerLake | | Stopped | |
| | 0 23 | TigerLake | | Stopped | |
| 00000000640D2023L 3C02 CMP AL,02 | - 15 | TIGGIDAKO | | bcopped | |
| 0000000640D2025L 499B80C0000000 MOV RAX,QWORD PTR [R8]+000000c0 | ٢ | | | | > |
| 00000006401202CL /50C JNE short ptr 0000000640d205aL | (100) | | | |] |
| 000000066022031L OFB70401 MOVZX EAX.WORD PTR [RCA][RCA] | IP General Reg | gisters (PO*) | | | |
| 0000000640D2035L E9C4000000 JMP 000000640d20feL | ■IA-32 | Name | Value | | |
| 0000000640D203AL 8BCA MOV ECX,EDX | Intel 64 | RAX | 000000000000000000000000000000000000000 | 0 | |
| 0000000640D203CL 8A0401 MOV AL, BYTE PTR [RCX] [RAX] | General | RBX | 00000000606BF75 | 0 | |
| 0000000640D203FL 535A000000 JMP 000000640201eL | Floating F | PDY | 000000000000000000000000000000000000000 | 8 | |
| 00000006401204BL 485C0 TEST RAX, RAX | Segment | RBP | 0000000061DD699 | 8 | _ |
| 00000000640D204EL 74A5 JE short ptr 0000000640d1ff5L | Control | RSI | 0000000061CF214 | 4 | |
| | Debug | RDI | 0000000061DD699 | 8 | |
| UUUUUUUUHUUZUIEL V V Disassembiy V Go Cursor Set Break V Track IP View IP Refresh | VMM - SI | RSP | 00000000606BF69 | 0 | |
| | YMM - D | R8 | 0000000061DD699 | 8 | |
| 🐨 Breakpoints 👘 🔛 | YMM - In | R9 | 0000000061CF101 | 8 | |
| Identifier Address Attributes | • MSR | P11 | 000000601D34203 | 0 | |
| | User | R12 | 000000000000000000000000000000000000000 | 0 | |
| | | R13 | 00000000000003E | 8 | |
| | | R14 | 0000000061CF214 | 4 | |
| Edit Add Remove Remove All Enable Disable All | | R15 | 0000000061DD699 | 8 | |
| | | CS | 0038 | | |
| 🔄 Log | | DS | 0030 | | |
| Date Time Component Message | | 55 | 0030 | | |
| 1/17/2021 14:04:20.282 Exception Handling Exception: Translation error in 00000000640D201EL | | FS | 0030 | | _ |
| | | GS | 0030 | | |
| | | RIP | 00000000640D201 | E | |
| | < > | RFLAGS | 000000000001020 | 6 | |
| | | | | | |
| | | | | | _ |
| Command | | | | | 1 |
| Scanning Uncore | | | | | ^ |
| Configuring Uncore | | | | | |
| Configuring Devices | | | | | - 10 |
| Connecting | | | | | |
| Loading Command Language Extensions: C:\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\aa\aaextend.mac | | | | | |
| Po> | | | | | |
| 502 | | | | | ~ |
| F1:Help, F5:Go, Shift+F5:Stop, F8:Step Into, F10:Step Over, Shift+F12:Reset | P0 18: St | topped | 64 Bit | Halt Mode | |

Hit the Refresh button in the Code window after the first Stop. This is only necessary once, to get out of Safe Mode; the Code window will automatically refresh with all run-control operations (stop, go, single-step, etc.) afterwards.

Refer to the <u>SourcePoint User Guide</u> in your install directory for detailed instructions on using all of the tool's features.

The board will halt automatically at the reset vector when you hit the SourcePoint Reset button (don't do this yet!):



| 🕑 Code (P0*): (1 | 6-bit) Tracking I | P 00000000L - FFFFFF | 1 | |
|--------------------|-------------------|----------------------|--|---|
| FFFFFEBL | 0000 | ADD ADD | BYTE PTR [BX+SI], AL | ^ |
| FFFFFFFFF | 0000 | DB | DILE FIR [BA+SI],AL | |
| □ FFFFFFF0L | 90 | NOP | | |
| FFFFFFF1L | 90 | NOP | | |
| FFFFFFF2L | E923C0 | JMP | near16 ptr ffffc018L | |
| FFFFFFF5L | 0000 | ADD | BYTE PTR [BX+SI],AL | |
| FFFFFFF7L | OOFB | ADD | BL,BH | |
| FFFFFFF9L | 0000 | ADD | BYTE PTR [BX+SI],AL | |
| FFFFFFBL | 0000 | ADD | BYTE PTR [BX+S1],AL | |
| FFFFFFF | UUFC FF | ADD | AH, BH | |
| | L L | | | |
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| FFFFFFOL | ~ | Disassembly ~ G | io Cursor Set Break 🗸 Track IP View IP Refresh | |

This is NOT desirable, because the latest AAEON Tiger Lake boards have issues recovering from the reset vector to implement AET. It is recommended that you disable the default halt at the reset vector by going to the Options > Emulator Configuration > Target Reset and click on "Run the target" in the "After SourcePoint reset" box:





| Emulator Configuration | × |
|--|---|
| General JTAG Target Reset Switches | |
| Target reset signal is: O Bidirectional O Output only (driven by emulator) | |
| Input only (sensed by emulator) | |
| SourcePoint reset causes the emulator to: After SourcePoint reset: Action: Wait on manual (external) target reset Reset time: 60 60 ms After target reset, emulator will wait 5500 ms to ensure stability Description Target reset signal input only | |
| OK Cancel Defaults Help | |

Congratulations, you have mastered SourcePoint's basic capabilities, and are using run-control. Many users are content to just use these basic operations, because run-control by itself is very powerful. However, if you wish to master the product and use some of its more advanced features, read on.



Advanced Topics: Using Trace

Trace is by far one of the most useful debugging utilities for triaging the most difficult, hard-to-reproduce bugs. Fortunately, the Tiger Lake CPU is equipped with all the latest-and-greatest Intel trace logic, and SourcePoint supports them all.

Let's look at a few of them, and how to configure their use in SourcePoint.

First Step: Configuring the Intel Trace Hub

Event tracing on the TGL platform is accomplished by the Intel Trace Hub. Fortunately, using DCI, events supported by the Intel Trace Hub can be streamed directly out of the system, well before Windows boots.

Boot to the UEFI shell. This is accomplished by powering on the target, and pressing the F7 key until you come to the password entry screen. Note the <u>Power Tip</u> above that references the newer Celeron boards, and the workaround necessary to get the target to power up.

Click on the Trace button in the toolbar at the top, to open the Trace window; then click on the Configure... button; then click on the Trace Hub tab. Set the settings as below:



| | Trace Hub AET Intel PT Intel PT Memory |
|--|--|
| Masters to | trace |
| ○ None | |
| () All | |
| List: | 18 |
| Trace rout | ing |
| Trace Hu | b: DbC ~ |
| Intel PT: | System Memory 🗸 🗸 |
| AET: | Trace Hub 🗸 |
| Use So | urcePoint settings |
| The second secon | |
| Base add | 16k v |
| Base add | 10% |
| Base add Length: Timestam |) |
| Base add Length: Timestamp | ent packets Frequency: CTC 16 |
| Base add Length: Timestam; Alignme | ent packets Frequency: CTC 16 |
| Base add Length: Timestamp Alignme Master / C | hannel definitions |

Architectural Event Trace

Once the Trace Hub has been enabled for the features you need, click on the AET tab, select All as Processors to trace, and select RDMSR/WRMSR and Port In/Out as events to trace:





| | Trace Hub | AET | Intel PT | Intel PT M | lemory |
|---|------------------|--------|----------|------------|----------|
| Processo | rs to trace | | | | |
| None | | | | | |
| Onone | | | | | |
| | | | | | |
| O List. | DO | | | | |
| ULBC. | PU | | | *** | |
| | (e.g., P0, P4-P | 7) | | | |
| Event sh | aring | | | | |
| 0 | | | | | |
| Apply | events to all pr | ocesso | rs | | |
| () Apply | events to: | | | | |
| 0.0000000000000000000000000000000000000 | | | | | |
| | | | | | |
| Event | | | Enable | ed IBR | ^ |
| HW/SW : | Interrupt | | | | |
| IRET | | | | | |
| Except: | ion | | | | |
| RDMSR/1 | WRMSR | | | | |
| Port In | n/Out | | I | | |
| Code b: | reakpoint | | | | |
| Data b: | reakpoint | | | | |
| BTM | | | | | |
| SMI/NM | I/RSM | | | | |
| MONITO | R/MWAIT | | | | |
| | | | | | |
| WBINVD | | | | | ~ |
| WBINVD SGX | | | | | |
| WBINVD SGX | | | dvanced | Clea | ir all |
| WBINVD SGX | | P | dvanced | Clea | ir all |

Now, you can simply do a Go/Stop to capture the event trace data. Below shows using the Command window to simulate a break on any read/write of port x'CF8', the PCI CONFIG_ADDRESS. This is done by typing the following into the Command window:

go til cf8io

This will run the target until the next IN or OUT to CF8.

After issuing the command, you'll see something like this:

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| Pike - MUNU First Tace First | | | Load UEFI Macros 🏶 | 1454 8 8 9 9 9 | ំបើ 🗋 🛊 🛊 🖉 | Breakpoints 🕒 Code 🕻 Command 📗 | 🛛 Log 🎹 Memory 🏼 IP Registers 🔍 Symb | ols 🧨 Trace 👀 Viewpoint 🔾 |
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| Desk Composition Composition <thcomposition< th=""> <thco< th=""><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></thco<></thcomposition<> | | | | | | | | |
| FE ADDR TIME Photo ADDR TIMESTAP ADDR Burged Burged <thburged< th=""> <thburged< th=""> <thburge< th=""><th>ice Hub - SW/FW Trace</th><th>Event Trace</th><th></th><th></th><th></th><th></th><th></th><th></th></thburge<></thburged<></thburged<> | ice Hub - SW/FW Trace | Event Trace | | | | | | |
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| -000000566 PD Condition Control (1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1 | ata available - Unable | STATE | Pn ADDR | INSTRUCTIO | JN Dete-000000EE | | TIMESTAMP | Stopped (h) |
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| 000000514 E00 000000000000000000000000000000000000 | | 00000000000 | Event: Roi | rt In: Port=1830 | DATIM | | 00.400 us | |
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| 0000000478 P0 000000000000000000000000000000000000 | | | Event: Por | ct In: Port=1830. | Data=80002033 | | | |
| 000000042 PD 000000007EE16180 UT DX, EXX -62.240 us 000000 00000042 PD 000000067EE178 US EXX, DX -62.240 us 000000 00000330 PD 000000067EE178 US EXX, DX -48.281 us 000000 00000299 PD 000000067EE178 US EXX, DX -46.484 us B3100 00000226 PD 000000007EE178 US EXX, DX -46.484 us B3100 00000226 PD 000000007EE178 US EXX, DX -46.354 us B3100 000000226 PD 0000000067EE174 OUT DX, EXX -44.115 us 0000000 000000226 PD 0000000067EE174 OUT DX, EXX -44.115 us 0000000 000000226 PD 0000000067EE174 OUT DX, EXX -44.115 us 0000000 000000226 PD 0000000067EE174 OUT DX, AL -17.161 us -42.318 us 0000000275 Disasemby Event: Port-0ut: Port-0ut: Port-0ut: Data-000000FF -24.92.92 us 0000000 0000000067EE174 DD OT DX, AL -17.161 us -44.9.791 ns -0000000267EE170 DT 17/2021 16:35:49.222 -0000000067EE176 DT DX, AL -49.099 us -49.099 us -49.099 us <td></td> <td>-000000478</td> <td>P0 00000006</td> <td>TEE16DD IN</td> <td>EAX.DX</td> <td></td> <td>-64.036 us</td> <td></td> | | -000000478 | P0 00000006 | TEE16DD IN | EAX.DX | | -64.036 us | |
| -000000442 P0 000000007EEEISI OUT DX, EAX -62.240 us 000000 -000000466 P0 000000007EEI798 IN EAX, DX -51.406 us 000000 -000000370 P0 000000007EEI798 IN EAX, DX -48.281 us 000000 -000000334 P0 000000007EEI796 OT DX, EAX -46.484 us BB1000 -00000029 P0 000000007EEI796 OT DX, EAX -46.484 us BB1000 -00000026 P0 000000007EEI796 OT DX, EAX -46.484 us BB1000 -00000028 P0 000000007EEI740 IN EAX, DX -46.354 us BB1000 -00000026 P0 000000007EEI740 IN EAX, DX -44.115 us DA3CC0 -00000026 P0 000000007EEI740 IN EAX, DX -44.115 us DA3CC0 -00000026 P0 000000007EEI740 IN EAX, DX -42.318 us A32018 -00000026 P0 000000007EEI740 IN IX, EAX -42.318 us A32018 -00000026 P0 000000067EEI7470 IN IX, AL -17.161 us A23018 -00000019 P0 000000067EEI7470 IN IX, AL -17.161 us A23018 -000000018 P0 00000 | | | Event: Por | ct Out: Port=1830 | . Data=80002030 | | | |
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| Big Section Big Section Display Fiter Calibrate 0000075 0000000640CEFE 00000075 Big Section Configure Display Fiter Calibrate Refresh 000000000000000000000000000000000000 | | -000000406 | P0 00000006 | ZEE179B IN | EAX, DX | | -51.406 us | 000000 |
| -00000370 P0 0000000000000000000000000000 | | | Event: Por | ct In: Port=1830, | Data=80002033 | | | 000CF8 |
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| 000000334 P0 000000000000000000000000000000000000 | | | Event: Por | t Out: Port=1830 | , Data=80002033 | | | 00000 |
| D00375 Disassembly -00000067EE17A OUT DX, AL -44.115 US D00375 Disassembly -00000067EE17A OUT DX, AL -42.318 US 000375 Disassembly -00000067EE17A OUT DX, AL -24.922 US 00000067EE17A OUT DX, AL -24.922 US DA3AFO 0000067EE17A OUT DX, AL -24.922 US -00000067EE17A OUT DX, AL -24.922 US -000000190 PO 000000067EE17A OUT DX, AL -17.161 US -000000190 PO 000000067EE17A OUT DX, AL -17.161 US -000000190 PO 0000000067EE17A OUT DX, AL -494.791 US -0000001818 PO 00000000640CE1E64 OUT DX, AL -494.791 US -0000000282 PO 00000000640CE1E64 OUT DX, AL -494.791 US -0000000084 PO OU000000640CE1E64 OUT DX, EAX -00 US US -000000084 PO OU000000640CE1E64 OUT DX, EAX -00 US US | | -000000334 | P0 000000067 | /EE179F OUT | DX, EAX | | -46.484 us | B81C00 |
| 000000298 P0 000000000000000000000000000000000000 | | | Event: Por | t In: Port=1830 | | | | 0032040 |
| D00375 Disassembly -00000067EE17A OUT DX, EAX -44.115 us D00000 D00375 Disassembly -00000067EE17A OUT DX, EAX -42.318 us D0376 D00375 Disassembly -00000067EE17A OUT DX, EAX -42.318 us D0376 D00375 Disassembly -00000067EE17A OUT DX, AL -24.922 us D0308 -000000128 PO 000000067EE17A OUT DX, AL -17.161 us D000018 s Time Event: Port Out: Port OUT DX, AL -17.161 us D00000067EE17A OUT DX, AL -17.161 us -000000118 PO 0000000067EE17A OUT DX, AL -494.791 ns D000000000000000000000000000000000000 | | -000000298 | P0 000000067 | VEE17AO IN | EAX, DX | | -46.354 us | E0D3P0 |
| 000000262 P0 0000000067EE17A0 IN EXX,DX -44.115 us 000000 Event: Port 013:0, Data=30002033 -42.318 us -42.318 us 000000 00000226 P0 000000067EE17A4 OUT DX,EAX -42.318 us 000000 00000190 P0 0000000067EE17D0 OUT DX,AL -24.922 us 0000002 -00000190 P0 000000067EE17E7 OUT DX,AL -17.161 us 000002 -00000119 P0 000000067EE17E7 OUT DX,AL -17.161 us 000002 -00000118 P0 00000006402E16E OUT DX,AL -17.161 us 0000002 -00000012 P0 00000006402E16E OUT DX,AL -494.791 ns -000000082 P0 00000006402E16E OUT DX,AL -0000000250 Disassembly Configure Display Fiter Calibrate Refresh -00000006402E14 OUT DX,EAX +0 ns -0000000550 Disassembly Configure Display Fiter Calibrate Refresh -0000000550 Disassembly Configure Display Fiter Calibrate Refresh -000000064 OC Distance Configure Display Fiter Calibrate Refresh -0000000550 Disassembly Configure Display Fiter Calibrate Refresh -0000000064 OC Distance Configure Other | | | Event: Por | tt In: Port=1830, | Data=80002033 | | | E9D3B0 |
| D00375 Disassembly 000000677E217A4 OUT DX, EAX -000000677E217A4 OUT DX, AL -24.922 us -000000677E217A7 OUT DX, AL -24.922 us -00000154 P0 000000677E217A7 OUT DX, AL -17.161 us -00000018 P0 000000040C21164 OUT DX, AL -494.791 ns Event: Port Out: Port OUT, DX, EAX -000000046 P0 0000000464 P0 O0000000464 P0 O0000000464 P0 O0000000464 P0 O000000464 P0 Outers Alans/Documents Arium/SourcePoint=IA, 7, 12, 15 Macros Intel \ADL_TCO_Timer_Disable.mac Calabrate ("ergcie=1", "taat=1") til cffio til cffio<td></td><td>-000000262</td><td>P0 000000067</td><td>/EE17A0 IN</td><td>EAX, DX</td><td></td><td>-44.115 us</td><td>OCOCE</td> | | -000000262 | P0 000000067 | /EE17A0 IN | EAX, DX | | -44.115 us | OCOCE |
| 00000226 P0 000000000000000000000000000000000000 | | | Event: Por | rt Out: Port=1830 | , Data=80002033 | | | 000000 |
| Disassembly Event: Port Out: Port-0021, Data=00000FF 00000190 Disassembly 000000197E2170 OUT bissembly 000000197E2170 OUT 000000197E2170 OUT DX, AL s Time c:00000197E2170 OUT DX, AL -000000184 DO Display -000000185 P0 O000000000000000000000000000000000000 | | -000000226 | P0 000000067 | EE17A4 OUT | DX, EAX | | -42.318 us | UAJAFU |
| 00000190 P0 000000000000000000000000000000000000 | | | Event: Por | rt Out: Port=0021. | , Data=000000FF | | | A23018 |
| 200375 Disassembly Event: Port Out: Port-00Al, Data=00000FF e Time 000000154 PD 00000006782172 OUT DX, AL -17.161 us e Time Event: Port Out: Port-0070, Data=00000082 -8.099 us 17/2021 16:35149-222 -0000001640C1166 OUT DX, AL -494.791 ns event: Port Out: Port-OTC, Data=0000005 -0000000460C1164 OUT DX, AL -0000001640C1160 OUT DX, AL -494.791 ns -0000000500 Disassembly Configure Display -0000000500 Disassembly Configure Display -00000000640C1164 OUT DX, EAX -00 -000000050 Disassembly Configure Display -000000050 Di | | -000000190 | P0 000000067 | /EE17DD OUT | DX,AL | | -24.922 us | 000002 |
| -00000154 P0 00000067E217E7 OUT DX,AL -17.161 us E Vent: PortOut: Port-0070, Data=00000082 -0000018 P0 000000640CE166 OUT DX,AL -8.099 us EVent: PortOut: Port-0076, Data=00000005 -000000082 P0 0000000640CE164 OUT DX,AL -494.791 ns E Vent: PortOut: Port-0076, Data=0000008 -000000064 D0 0000000640CE164 OUT DX,EAX +0 ns -0000000550 Disassembly Configure Display Filter Calibrate Refresh -000000550 Disassembly Configure Display Filter Calibrate Refresh -000000550 Disassembly Configure Display Filter Calibrate Refresh -0000000550 Disassembly Configure Display Filter Calibrate Refresh -00000000550 Disassembly Configure Display Filter Calibrate Refresh | 000375 Disassembly ~ | | Event: Por | rt Out: Port=00A1. | , Data=000000FF | | | 000001 |
| <pre>Event: Port Out: Port-0070, Data=00000082 T/2021 16:35:39.976 F T/2021 16:35:39.976 F T/2021 16:35:49.222 F O00000082 P0 0000000640CEIE6 OUT DX, AL O00000082 P0 0000000640CEIE4 OUT DX, AL O00000084 COEIE4 OUT DX, AL O000000550 Disassembly Configure Display Fiter Calbrate Refresh Composed Calter: C:\Uners\alans\Documents\Arium\SourcePoint=IA_7.12.15\Macros\Intel\ADL_TCO_Timer_Disable.mac Fiter: C:\Uners\Alans\Documents\Arium\SourcePoint=IA_7.12.15\Macros\Intel\ADL_TCO_TIME_IDI Fiter: C:\Uners\Alans\Documents\Arium\SourcePoint=IA_7.12.15\Macros\Intel\ADL_TCO_TIME_IDI Fiter: C:\Uners</pre> | | -000000154 | P0 000000067 | EE17E7 OUT | DX,AL | | -17.161 us | |
| e Time -0000000118 P0 0000000640CE1B6 OUT DX,AL -8.099 us 17/2021 16:35:39.976 ft Event: Port_OUT: Data=0000005 -494.791 ns Event: Port OUT: Data=000000064 Display -494.791 ns e 0000000640CE1E4 OUT DX,AL -494.791 ns e 0000000640CE1E4 OUT DX,EAX +0 ns e 0000000550 Disassembly Configure Display Filter e 000000000000000000000000000000000000 | | | Event: Por | rt Out: Port=0070. | , Data=000000B2 | | | |
| 1/7/2021 16:35:39.976 II Event: Port Out: Port-0076, Data=0000005 1/7/2021 16:35:49.222 I 0000000082 PO 00000000640CEICE OUT DX, AL -000000082 PO 0000000640CEIE4 OUT DX, EAX +0 ns -0000000050 Disassembly Configure Display Fiter Calbrate Refresh vd -000000050 Disassembly Configure Display Fiter Calbrate Refresh vd -000000006(*OccEIe4 OUT DX, EAX +0 ns * vd -000000006(*OccEIe4 OUT DX, EAX +0 ns * vd -000000000000000000000000000000000000 | e Time (| -000000118 | P0 000000064 | OCE1B6 OUT | DX,AL | | -8.099 us | |
| <pre>1/2021 10:35:49-222 E = 0000000082 P0 0000000640CE1CD OUT DX,AL -494.791 ns Event: Port OUT: Data=80000008</pre> | 17/2021 16:35:39.976 F | | Event: Por | ct Out: Port=0076. | , Data=00000005 | | | |
| by the field of th | 1772021 16:35:49.222 g | -000000082 | P0 000000064 | OCE1CD OUT | DX, AL | | -494.791 ns | |
| <pre>d</pre> | | | Event: Por | rt Out: Port=0CF8. | , Data=80000008 | | | |
| v ind ind ind ind ind ind ind ind | | -000000046 | P0 000000064 | OCE1E4 OUT | DX,EAX | | +0 ns | |
| | | | | | | | | ~ |
| <pre>id g Reset (after): C:\USers\alans\Documents\Arium\SourcePoint=IA_7.12.15\Macros\Intel\ADL_TCO_Timer_Disable.mac til cf8io til cf8io til cf8io til cf8io til cf8io</pre> | | -000000550 | Disassembly v Co | onfigure Display | Filter | Calibrate Refresh | | |
| d g Reset (after): C:\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\Intel\ADL_TCO_Timer_Disable.mac EnableForce("cpcie=1", "tsact=1") til cf8io til cf8io til cf8io til cf8io | | | | onphay | | Trenesh | | |
| nd ng Reset (after): C:\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\Intel\ADL_TCO_Timer_Disable.mac EmableForce("cpcie=1", "tsact=1") til cf8io til cf8io til cf8io til cf8io | | | | | | | | |
| " gReset (after): C:\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\Intel\ADL_TCO_Timer_Disable.mac EnableForce("cpcie=1", "tsact=1") til cf8io til cf8io til cf8io til cf8io | | | | | | | | |
| ng Reset (alter): Crosers (alans bocuments (arium (sourceroint in_/.12.13 (macros (inter (abl_100_1imer_bisable.mac til cf8io til cf8io til cf8io til cf8io | an Deast (after) . Gall | | Demonster (Demissre) C | augus Dalat IN 2 1 | 2.15\Magazak | ling mon miner Dischla man | | |
| til cf8io til cf8io | kEnableForce("cpcie=1" til cf8io til cf8io | , "tsact=1" |) | ourceroine in_/.1 | 2.13 (100103 (110 | SI (HDI_100_11me1_DIOUDIC.muc | | |
| til cf8io | til cf8io | | | | | | | |
| | | | | | | | | |
| | til cf8io | | | | | | | |
| | til cf8io | | | | | | | |

Scrolling up a little, you'll see a mix of Port In/Out and RDMSR/WRMSR, all timestamped.

Power tip: The Last Branch Record (LBR) stack associated with each event can be captured as well. This is a very powerful debugging utility, especially when troubleshooting code execution leading up to events before system memory is initialized and Intel Processor Trace is available.



| ce Config | uration | | | | × |
|-----------|-----------------------|----------|------------|--------------|------|
| BR BT | S Trace Hub | AET | Intel PT I | ntel PT Memo | ry |
| Processo | rs to trace | | | | |
| ○ None | | | | | |
| | | | | | |
| | | | | | |
| • List: | p0 | | | | |
| | (e.g. D0 D4-D7 | 7) | | | |
| | (e.g., r0, r4-r) |) | | | |
| Event sha | aring | | | | |
| | - events to all pr | CASSOFS | | | |
| | | 50035015 | | | |
| | v events to: | | \sim | | |
| | | | | | |
| | | | | | _ |
| Event | . | | Enabled | LBR | |
| HW/SW | Interrupt | | | | |
| IRET | | | | | |
| Except | ion | | | | |
| RDMSR/ | WRMSR | | V | | |
| Port I | n/Out | | ⊻ | | |
| Code b | reakpoint | | | | |
| Data b | reakpoint | | | | |
| BTM | | | | | |
| SMI/NM | I/RSM | | | | |
| MONITO | R/MWAIT | | | | |
| WBINVD | | | | | |
| SGX | | | | | |
| 1 | | | | | |
| | | Ad | vanced | Clear all | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | OK | Cano | el | Help |
| | | | | | |



Intel Processor Trace

Intel Processor Trace (Intel PT) is available only after system memory is initialized.

It's easy to set up. Click on the Trace button in the top toolbar, click the Configure... button, click on the Intel PT tab, put p0 in Processors to trace, and be sure that TSC and Cycle accurate under the Timestamp heading are enabled:

| Trace Configuration | X |
|--|---|
| LBR BTS Trace Hub AET Intel PT Intel PT Memory | |
| Processors to trace | |
| ○ None | |
| | |
| ● List: p0 | |
| Share filter / timestamp settings | |
| Filters | |
| Range 1: Enter symbol or start-end | |
| Range 2: Enter symbol or start-end | |
| CPL: User ~ | |
| □ CR3: | |
| Timestamp | |
| ⊡ TSC | |
| Trequency: CTC 6 | |
| Cycle accurate Threshold: 0 (fine) | |
| OK Cancel Help | |

That's all. Then use the go til cf8io trick to capture some instruction trace data:



| 🔛 🔁 🔛 🥔 🐨 🖓 | ace window help | Load | UEFI Macros | 4 | 141 * 1 | u u u u | 🛚 🏶 🍰 💿 Bre | akpoints 🕒 | Code > | Command | Log 🎹 M | Memory IP Re | gisters 🔍 Symb | ools 🧨 Tra | ace 🔍 Viewpoint 🤇 |
|----------------------|--|------------|-------------|------------|----------------|---------------|--------------|------------|----------|----------|-----------|--|----------------|------------|-------------------|
| | | | | | | | | | | | | | | | |
| | | | | | | | | | 1 1 | | COMIN | i i al a factoria de la compañía de | | | |
| TE ADDR | Event Trace | | | | | | | | | | | | | 23 | |
| ata available - Unab | 1e STATE | Pn | ADDR | _ | INSTRU | JCTION | | | | | | TIMES | TAMP | ^ | Stopped (h |
| | -000000658 | PĤ | Event: Po | or 67 . | Intel Processo | Trace (P0*) | | | | | | | | | |
| | | | Event: Po | or | STATE Pn | ADDR | INSTR | JCTION | | | | | | | TIMESTAMP |
| | -000000622 | P0 | 00000000 | 67 - | 00415 P0 | 00000005E | FOB14C2 MOV | RA | X,RBX | | | | | | -267.970 us |
| | | | Event: Po | or | PO | 00000005E | OB14C5 MOV | [0 | 0000000 | 05f0bb0b | b8],RDI | | | | |
| | -000000586 | PO | 00000000 | 67 | PO | 00000005E | OB14CC MOV | RB | X, [RSP] |]+30 | | | | | |
| | | | Event: Po | or | PO | 00000005E | OB14D1 ADD | RS | P,00000 | 0020 | | | | | |
| | -000000550 | PO | 000000000 | 67 | PO | 00000005E | TOB14D5 POP | RD | I | | | | | | |
| | | | Event: Po | or | PO | 00000005E | OB14D6 RETN | | | | | | | | |
| | -000000514 | PO | 00000000 | 67 - | 00409 P0 | 000000064 | OCD67D XOR | EC | X,ECX | | | | | | -267.969 us |
| | 101050200000000000000000000000000000000 | | Event: Po | or | PO | 000000064 | OCD67F MOV | RB | X,RAX | | | | | | |
| | -000000478 | PO | 00000000 | 67 | PO | 000000064 | OCD682 CALL | 00 | 000000 | 640ce020 | 0L | | | | |
| | | | Event: Po | or | PO | 000000064 | OCE020 MOV | [R | SP]+08, | , RBX | | | | | |
| | -000000442 | PO | 00000000 | 67 | b 0 | 000000064 | OCE025 MOV | [R | SP]+10, | ,RSI | | | | | |
| | | | Event: Po | or | PO | 000000064 | OCE02A PUSH | RD | I | | | | | | |
| | -000000406 | P0 | 000000000 | 67 | P0 | 000000064 | IOCE02B SUB | RS | P,00000 | 0020 | | | | | |
| | and the second sec | | Event: Po | or | PO | 000000064 | IOCE02F LEA | RS | I,[0000 | 00000640 | 0cd000] | | | | |
| | -000000370 | P0 | 00000000 | 67 | PO | 000000064 | IOCE036 MOV | DI | L,CL | | | | | | |
| | | | Event: Po | or | P0 | 000000064 | IOCE039 TEST | CL | ,CL | | | | | | |
| | -000000334 | P0 | 000000000 | 67 | PO | 000000064 | IOCE03B JE | 00 | 0000000 | 640ce120 | dL. | | | | |
| | | | Event: Po | or | PO | 000000064 | IOCE12D MOV | RA | X,[0000 | 00000640 | Dce338] | | | | |
| | -000000298 | PO | 000000000 | 67 | PO | 000000064 | IOCE134 XOR | EB | X,EBX | | | | | | |
| | | | Event: Po | or | P0 | 000000064 | OCE136 JMP | 00 | 0000004 | 640ce14 | BL | | | | |
| | -000000262 | PO | 000000000 | 67 | PO | 000000064 | IOCE148 TEST | RĂ | X,RAX | | | | | | |
| 000375 Disassembly ~ | | 1000 | Event: Po | or | PO | 000000064 | OCE14B JNE | 00 | 0000000 | 640ce13 | BL | | | | |
| | -000000226 | P0 | 000000000 | 67 | PO | 000000064 | OCE14D TEST | DI | L,DIL | | | | | | |
| e Mime | | | Event: Po | or | P0 | 000000064 | OCE150 JNE | 00 | 000000 | 640ce21 | 1L | | | | |
| 17/2021 16.25.40 222 | -000000190 | P0 | 000000000 | 67 | PO | 000000064 | OCE156 DEC | [0 | | 0640ce31 | b8] | | | | |
| 17/2021 16:51:03 122 | H | | Event: Po | or | PO | 000000064 | IOCE15C MOV | EA | X, [0000 | 00000640 | Oce3b8] | | | | |
| 1772021 10.51.05.122 | -000000154 | P 0 | 000000000 | 67 | PO | 000000064 | IOCE162 CMP | EA | X,00000 | 000a | 220 | | | | |
| | 000000110 | - | Event: Po | OT | P0 | 000000064 | IOCEI65 JNC | 00 | 0000004 | 640ce21. | 11 | | | | |
| | -000000118 | P0 | 00000000 | 64 | PO | 000000064 | IUCEI6B MOV | LA | X, [0000 | 00000640 | nce3ps1 | | | | |
| | - | | Event: Po | 100 | PO | 000000000 | IUCEI/I LEA | KA | A. 18/4A | TIRMAAZ | | | | | |
| | -000000586 | Disass | embly ~ | Co | -00409 | Disassembly ~ | Configure | Display | Fill | ter | Calibrate | Refresh | | | |
| | -00000586 | Disass | embly ~ | Co | 00105 | Chausachildhy | Configure | Display | 1.10 | 101 | Calibrate | Refresh | | | |
| | | | | | | | | | | | | | | | |
| til cf8io | | | | | | | | | | | | | | | |
| til cf8io | | | | | | | | | | | | | | | |
| til aflio | | | | | | | | | | | | | | | |
| LII CI810 | | | | | | | | | | | | | | | |
| til ciolo | | | | | | | | | | | | | | | |
| LII CI010 | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | |

There's a lot more that you can see and do with these Trace utilities. SourcePoint can use Intel PT to display a Call Chart and Call Tree. You can open up Code Tracking windows that update dynamically as you walk through the code, showing you exactly where you are and the interaction between code and events. When you have source and symbols available, the firmware flow becomes much more intuitive and visual. Indulge your curiosity and imagination.

The video at <u>https://www.asset-intertech.com/wp-content/uploads/2021/11/UP-Xtreme-i11-Getting-Started.mp4</u> shows some of these capabilities. The <u>SourcePoint User Guide</u> also provides a very thorough, comprehensive review of the tool. And visit our <u>SourcePoint Academy</u> for helpful "How To" content.



Troubleshooting Tips

At some point, you'll run into something strange. We're the first to admit that JTAGbased run-control and trace are not always deterministic. JTAG is a 30-year hardware protocol, and when something goes astray at a very low level, SourcePoint tries to (but sometimes doesn't) recover gracefully. There will be times that the board will power cycle on its own. Or the firmware thinks that a thread is running but gets out of sync with the SourcePoint software, which thinks it's halted. Or the DbCStatus.exe ball stays red instead of turning green, while you swear you have a good DbC connection. Sometimes you have no choice but to quit SourcePoint and power cycle the target. That usually clears up the one-of's. But if the issue is repeatable, we ask that you collect as much information as you can, and open a ticket with us at <u>https://www.assetintertech.com/support/</u>. We'll respond as soon as possible.

In the meantime, here are a few errata that we've noticed on the UP Xtreme i11, and the steps needed to mitigate.

Firmware gets out of sync with software

On the host PC using DCI, functionality is roughly partitioned between software (SourcePoint application with its GUI) and a process called AssetDCI. Broad-brushing it, SourcePoint software on the host communicates with AssetDCI, that encapsulates JTAG traffic into packets which are sent to the PCH, which in turn performs the JTAG mastering function.

Somewhere along the line, the firmware may get out of sync with the software. You may see symptoms like:

In the Viewpoint window, the threads are shown as Running, whereas the Status Bar at the bottom right shows Stopped.

P0 in the Viewpoint window is Running, with one or more threads below it are in the Stopped state.

If this happens, you'll likely have to quit SourcePoint, kill the AssetDCI process (see below), power-cycle the target, then start over. Sorry. Then please enter <code>aalog = 20987</code> in the <code>Command</code> window to get verbose logs, and try to reproduce. We're extremely interested in these cases, so capture the verbose logs in the <code>Log</code> window and send to us.

Trace buffer overflows

DCI traffic processing has its limitations. When you try to collect too much trace data, the trace buffer overflows, causing aberrant behavior.



Although the trace data is highly compressed, some trace sources, specifically with AET, running through the Trace Hub can exceed the capacity of the USB 2.0 connection. In theory running at 480Mbps, in practicality SourcePoint can only process trace data at approximately 100Mbps. Beyond that, we collect ~ 20kB of trace data before a buffer in SourcePoint overflows, and we don't recovery gracefully.

| A 12 A A | | | COOL OF M | 100105 T2 T2 T2 T | | | | asponits 🔾 code . | Command 📷 Log | internoty 1 | augusters 🦏 symbo | a y nace de | / wewpoint | e volte |
|--|---------------------------|----------------------------------|-------------------|-------------------|--------------|------------|------------------------|-------------------|-----------------|-------------|-------------------|-------------|---------------|---------|
| | Trace Hub - S | SW/FW Trace | | | | | | | | - • × | | | | |
| Lode (P0*): (64 | STATE | ADDR ow Snip | INSTRUCT | ION | | | | | TIMESTAMP | | Description | | | |
| 00000067 | 024948849 | | GLOBA | L=0249F0000 | 0 | | | | | | Description | 1 | the second of | Status |
| 000000067 | -024948839 | | AET-1 | 8:C01=00000 | 00067EF94B1 | | | | | | Lake | 5 | topped | |
| 000000067 | -024948830 | | AET-1 | 8:C01=00001 | 80800EFD2C1 | | | | | | Lake | S | topped | |
| 000000067 | -024948821 | | AET-1 | 8:C01=00034 | 5000004FADE | | | | | | Lake | S | topped | |
| 000000067 | -024948812 | | AET=1 | 8:001=00000 | 0000A7998C21 | | | | | | Lake | S | topped | |
| 00000067 | -024940003 | | ADITI ADTTI | 8:001=00000 | 000007619461 | | | | | | | | | |
| 000000067 | -024948794 | | AET=1 | 8:001-00032 | 50000001808 | | | | | | | | | , |
| 00000067 | -024948776 | | AFT-1 | 8:001=000002 | 00007983015 | | | | | | | | | |
| 00000067 | -024948767 | | AET-1 | 8:001=00000 | 00067EF94B1 | | | | | | (PO*) | | | 9 XX |
| 00000067 | -024948758 | | AET-1 | 8:C01=00001 | 80800EFD2CC | | | | | | e Value | | | |
| 00000067 | -024948749 | | AET-1 | 8:C01=00034 | 5000004FADE | | | | | | 0000000 | 0FED000FF | | |
| 000000067 | -024948740 | | AET-1 | 8:C01=00000 | 0C0A79A3C49 | | | | | | 0000000 | 05F0A4C60 | | |
| 00000067 | -024948731 | | AET-1 | 8:C01=00000 | 00067EF94B1 | | | | | | 0000000 | 000000001 | | |
| 000000067 | -024948721 | | GLOBA | L=000000000 | 0000001 | | | | +333.522 sec | | 0000000 | /0000000A1 | | |
| 000000067 | | *** Overflow - | multiple m | asters *** | | | | | | | 0000000 | /063A335D0 | | |
| 000000067 | -024948709 | | GLOBA | L=01 | | | | | | | 0000000 | /05F0A4C68 | | |
| 00000675517 | -024948707 | | GLOBA | L=000000000 | 0000492 | | | | +333.522 sec | | 0000000 | 05F0A4CA8 | | |
| 0000007EE17 | -024948696 | | AET-1 | 8:C01=00032 | 5000004FADE | | | | | | 000000 | /05F0A4BE8 | | |
| | -024948687 | | AET-1 | 8:C01=00000 | OCOA7A11E1F | | | | | | 0000000 | 0000000000 | | |
| | -024948678 | | AET-1 | 8:C01=00000 | 00067EF94B1 | | | | | | 800000 | 00000000E | | |
| | -024948669 | | ALT=1 AET=1 | 8:001=00001 | 5000004FADE | | | | | | 0000000 | 0000000000 | | |
| | -024948651 | | AET-1 AET-1 | 8.001=000034 | 0C037312C09 | | | | | | 0000000 | 05F0A4B80 | | |
| | -024948642 | | AET-1 | 8:001=00000 | 00067EF94B1 | | | | | | 0000000 | 0000000000 | | |
| | -024948633 | | AET-1 | 8:C01=00000 | 00000001808 | | | | | | 0000000 | 000000001 | | |
| | -024948624 | | AET-1 | 8:C01=00032 | 5000004FADE | | | | | | 0000000 | | | |
| 10 | -024948615 | | AET-1 | 8:C01=00000 | 0C0A7A1D005 | | | | | | | | | |
| at a | -024948606 | | AET-1 | 8:001=00000 | 00067EF94B1 | | | | | | | | | |
| /17/2021 | -024948597 | | AET-1 | 8:C01=00001 | 80800EFD324 | | | | | | | | | ^ |
| /17/2021 | -024948588 | | AET=1 | 8:C01=00034 | 5000004FADE | | | | | | | | | |
| 1/1//2021 | -024948579 | | AET-1 | 8:C01=00000 | 0C0A7A1DC3D | | | | | | | | | |
| | -024948570 | | AET-1 | 8:C01=00000 | 00067EF94B1 | | | | | × | · | | | |
| | -024949259 | Disassembly ~ | Configure | Display | Filter | Calibrate | Refresh | | | | | | | |
| | | | comparent | e lopidy in | | | | | | | | | | |
| | | | | | | | | | | | | | | ~ |
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| nand | | | | | | | | | | | | | | |
| go til cf8 | io | | | | | | | | | | | | | ~ |
| go til cf8 | io | | | | | | | | | | | | | |
| go til cf8 | io | | | | | | | | | | | | | |
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| | | | | | | 0.15114 | - X T - 4 - 3 X T - 73 | mco mimor Di- | - hill - second | | | | | |
| ding Reset | (after): C | :\Users\alans\ | Documents\A: | rium\Source | Point-IA_7.1 | 2.15\Macro | s\intei\AD | -ico_iimer_bi | sable.mac | | | | | |
| <mark>ding Reset</mark> npkEnableF | (after): C orce("cpcie | :\Users\alans\ =1", "tsact=1" | Documents\A:) | rium\Source | Point-IA_7.1 | 2.15\Macro | slinteilAD | _ico_iimer_bi | sable.mac | | | | | - 1 |
| <mark>ding Reset</mark> npkEnableF | (after): C orce("cpcie | :\Users\alans\ =1", "tsact=1" | Documents\A:) | rium\Source | Point-IA_/.1 | 2.15\Macro | s (intei (ADI | _rco_rimer_br | sable.mac | | | | | |

You'll see these symptoms of this occurrence in the SW/FW Trace window:

A few of these overflows are no big deal. But, if you're tracing a huge amount of data, SourcePoint may spin, as it tries to process all that data, and deal with the mess. Sometimes, after maybe a few minutes, it recovers. Sometimes, you end up in limbo.

The only solution at this point is to quit SourcePoint, do an End task on the AssetDCI Background process, power cycle the target, and start over:



| 💐 Task Manager | _ | • | × | | | |
|--|-----|---------|---|--|--|--|
| File Options View | | | | | | |
| Processes Performance App history Startup Users Details Services | | | | | | |
| ^ | 31% | 84% | | | | |
| Name Status | CPU | Memory | | | | |
| Adobe Collaboration Synchronizer 21.7 (32 bit) | 0% | 1.2 MB | ^ | | | |
| 😂 Adobe Collaboration Synchronizer 21.7 (32 bit) | 0% | 1.1 MB | | | | |
| 🚔 Adobe Collaboration Synchronizer 21.7 (32 bit) | 0% | 2.0 MB | | | | |
| 🚔 Adobe Collaboration Synchronizer 21.7 (32 bit) | 0% | 2.2 MB | | | | |
| > Adobe Genuine Software Integrity Service | 0% | 1.2 MB | | | | |
| > III Adobe Genuine Software Service | 0% | 1.7 MB | | | | |
| Adobe Installer | 0% | 0.9 MB | | | | |
| 🗐 Adobe IPC Broker (32 bit) | 0% | 2.8 MB | | | | |
| > 💿 Adobe Update Service | 0% | 1.1 MB | | | | |
| Application Frame Host | 0% | 8.3 MB | | | | |
| 🔳 ariumImd daemon | 0% | 1.4 MB | | | | |
| ssetDCI (32 bit) | | 51.5 MB | | | | |
| CCLibraries | | 0.1 MB | | | | |
| CCXProcess | | 0.1 MB | v | | | |
| < | | | > | | | |
| Fewer details End task | | | | | | |

Ultimately, we're working on improving the performing of the AssetDCI driver, and behaving more graciously when an overflow is encountered. But, in the interim, it is key to ensure that the trace data collected is relatively "sparse". Focus your debugging in the specific area of interest. Don't try to collect all Port IN/OUT from the reset vector all the way through to the UEFI shell. At 750K I/Os per second, you'll swamp the host debugger processing, and you can't deal with all that data anyway.

Note that this only happens with AET – that is, you can only overflow by collecting too much AET data. It does not apply to LBR, SW/FW Trace, SVEN, or Intel PT. It may take some trial and error to limit the scope of your event data collection.

Intel Processor Trace – Slow!

When you configure Intel PT, you can specify the size of the buffer in system memory to collect trace data:





| Trace Configuration | | × | | | |
|-------------------------------|--------------------|-----------------|--|--|--|
| LBR BTS Trace | Hub AET Intel PT | Intel PT Memory | | | |
| Trace buffer | | | | | |
| O Use processor se | ttings | | | | |
| • Use SourcePoint settings: | | | | | |
| Base address: | 10000000P | P | | | |
| Length per core: | 16k ~ | | | | |
| Trace capture mode | 32k 64k 128k | | | | |
| Overwrite | 256k 512k | | | | |
| ○ Append | 1M 2M 4M | | | | |
| | 8M 16M | | | | |
| | 32M 64M 128M | | | | |
| | 256M 512M | | | | |
| | 1G 2G | | | | |
| | 20 | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| [| OK Ca | ancel Help | | | |

Note that Intel PT directs instruction trace data to system memory. Although highly compact and efficient, we are not streaming over DCI to the host in this case; we buffer the code execution data until the platform is halted, at which point SourcePoint uses JTAG over DCI to collect the trace data out of system memory, reconstruct and display

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it. JTAG operates at fairly low speeds, and for large buffer sizes the transfer of all that data can be slow. It starts to become noticeable beyond a buffer size of 64kB.

SourcePoint compensates for that by only pulling in the trace data that's local to the code display you are in. Scrolling up in the Intel PT window will prompt SourcePoint to pull in more trace data, and display it. Be patient when this happens. If you try to collect 1GB of data from system memory over JTAG, it will take a long while for this all to be available. Displaying the Call Chart for this much data will take a while. You'll see this after initial trace data collection (that only takes a few seconds), but scrolling to the top of the Intel PT window with a 1MB trace buffer (which gives you ~ 300ms of execution trace data) takes ~30 seconds, and then doing a Call Chart takes over 10 minutes. Be patient.

| Building trace display | | | | |
|------------------------|---|--|--|--|
| Status: | Analyzing Trace | | | |
| Progress: | | | | |
| | Processing trace This may take a few moments. | | | |
| Cancel | | | | |
| | | | | |

| Analyzing t | race data | |
|-------------|-----------|---------|
| Calls: | 3048 | |
| Progress: | | 4.6% |
| | | Suspend |



My board is not booting – what now?

Once in a while, especially during an intense debug session, we have found that the target goes into la-la land. You get to the UP splash screen, and then it just stops. Or the screen stays black. SourcePoint run-control continues to work, but it won't boot all the way up to the UEFI shell. Quitting SourcePoint, unplugging the DCI cable, killing the AssetDCI process, knocking out the AssetDCI process – all are good steps in this instance, when you need to recover.

But then, once in a while, you wait the needed 20 seconds; and it doesn't boot. The screen stays blank or frozen. We know that happens with the newest Celerons, and there's a <u>workaround</u> for that, but this might not be the issue.

Don't panic! For reasons we're not sure of just yet, after about 60 seconds, the board "wakes up" and should boot all the way to the UEFI shell.

Clearing the CMOS on the target has also been known to help when it still won't boot up. There's only one thing: it has gone back to the factory settings, so you'll need to reset the WDT timer, and perform the other steps, as per <u>BIOS Settings</u> section in this manual.

Then, you'll be back in business.



Conclusion

Thank you for getting this far! We hope that you have enjoyed the ride, and are using the power of SourcePoint successfully in your debugging and learning journeys.

Feel free to browse the SourcePoint Academy at <u>https://www.asset-</u> <u>intertech.com/sourcepoint-academy/</u> for helpful reference guides, help material and "how to" videos.

If you ever have any questions, please call, email or open a Support Case here: <u>https://www.asset-intertech.com/support/</u>. We'll be glad to help!

