Real Insight from Code to Silicon

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System-Level JTAG with ScanWorks Dispatcher

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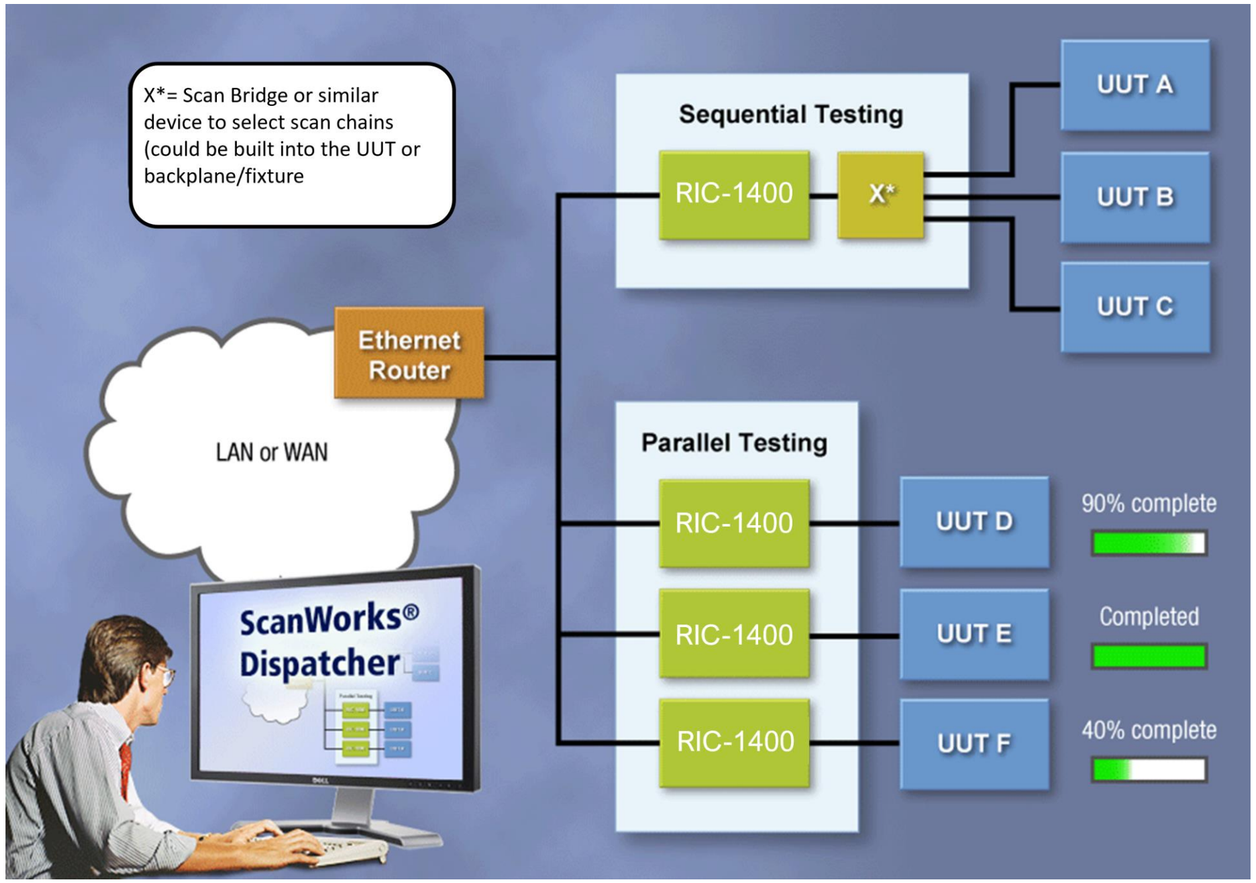
November 30, 2023

Agenda

- Guidelines for Board DFT based on Boundary Scan Webinars #1 & # 2
- Guidelines for System-Level JTAG Design Webinar #3
- ScanWorks Dispatcher
- Elements of a ScanWorks Dispatcher Deployment
- ScanWorks Dispatcher Demonstration
- ScanWorks Dispatcher Use Cases
- Summary



Board DFT based on Boundary Scan – Webinar #1

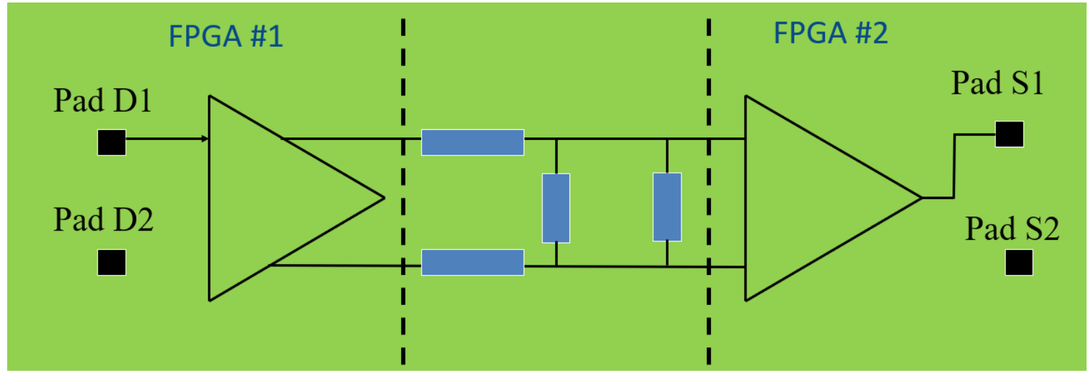
- Why do we test?
- Test challenges
- Boundary Scan overview
- Boundary Scan device selection
- Focus on the Scan Chain design
- Accessing to the TAP
- Buffering the TAP
- Direct control of the system clock
- TCK and TMS distribution
- Pull-up/pull-down on TAP signals
- Board TRST
- Handle troublesome devices / different voltages
- Connector test
- Allow defeatable tied-off pins / unused boundary scan pins
- Introduction to testing memory devices/flash programming
- Bypass watchdog circuits

Covered in [Board Design for Test (DFT) based on Boundary Scan Webinar #1]

Board DFT based on Boundary Scan – Webinar #2

- Interconnect Testing
  - Cluster modeling
  - Using Discrete I/O
  - Controlling clocks
- Memory Interconnect Testing
  - Chip Enables
  - Flash Programming
  - Cell Z/Cell Active Configurations
- Testing with FPGAs
  - Pros/cons of testing unconfigured and configured

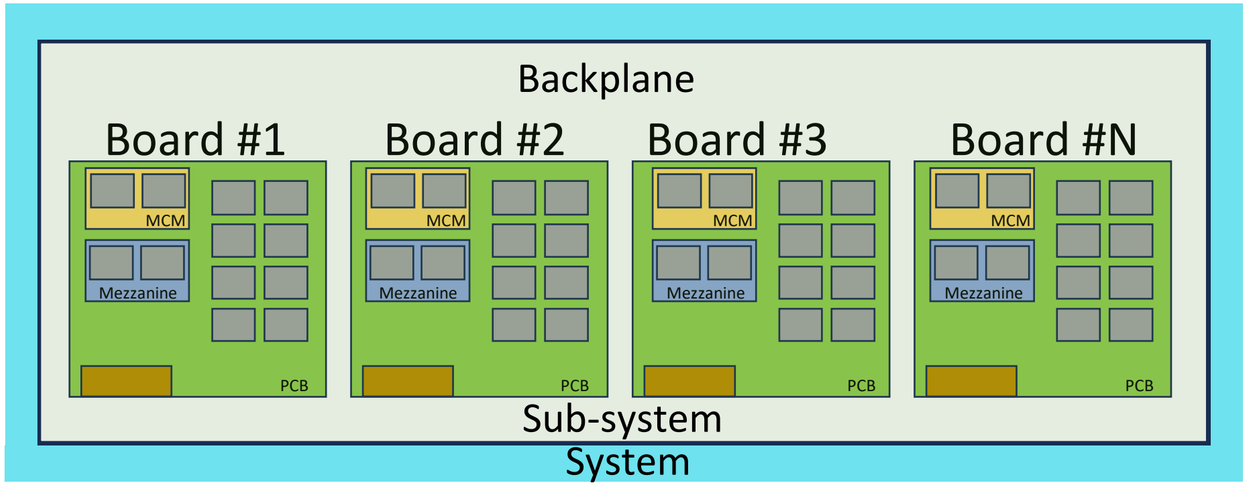
```
#VECTOR a1 47, 46, 44, 43
#VECTOR b1 2, 3, 5, 6
!-------------------------------------------------
#PART dis                ! whole device disabled
1     DRIVE  1           ! disable part1
48    DRIVE  1           ! disable part2
25    DRIVE  1           ! disable part3
24    DRIVE  1           ! disable part4
!-------------------------------------------------
#PART a2b                ! part1 transfer
1     DRIVE  0           ! enable part1
b1 EQUAL a1
```



Covered in [Board Design for Test (DFT) based on Boundary Scan Webinar #2]

System-Level JTAG Design – Webinar #3

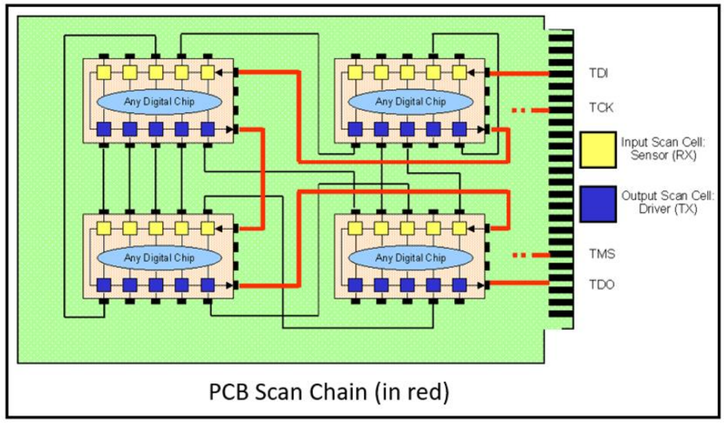
- Ring Architecture
- Star Architecture
- Multi-TAP Devices
  - SCANSTA112
- Multi-TAP Controllers
- ScanWorks Embedded Diagnostics
- SED for Test
- SED for Built-in Self-Test



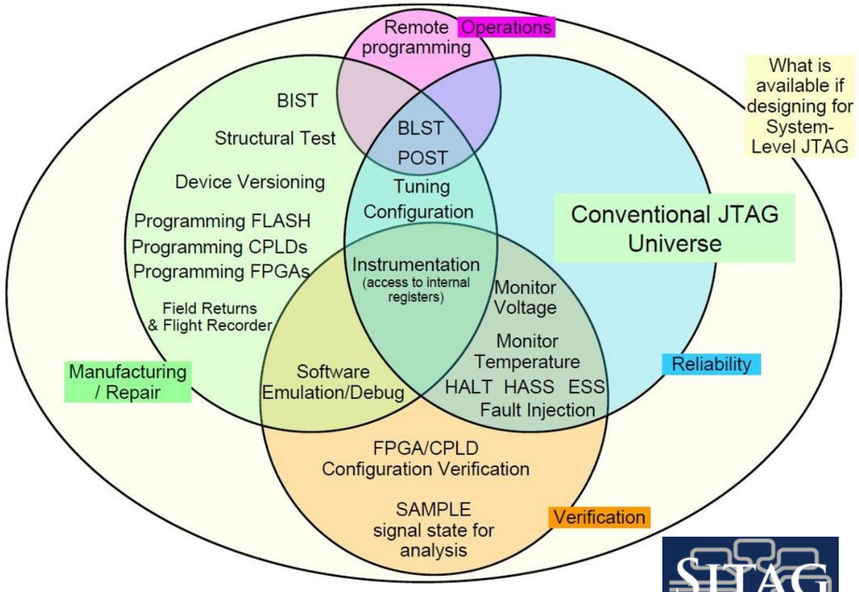
Covered in [Guidelines for System-Level JTAG Design Webinar #3]

System-Level JTAG Design – Webinar #3

- System-level JTAG (SJTAG) presumes that concept of applying JTAG to the individual boards of the target system has been embraced and implemented
- System-level creates a test access mechanism that extends the usefulness of JTAG throughout the entire product life-cycle
- System-level JTAG extends JTAG significantly beyond the traditional board-level scope of structural test and device programming
- The potential of SJTAG is illustrated by the Venn Diagram described as the SJTAG Universe

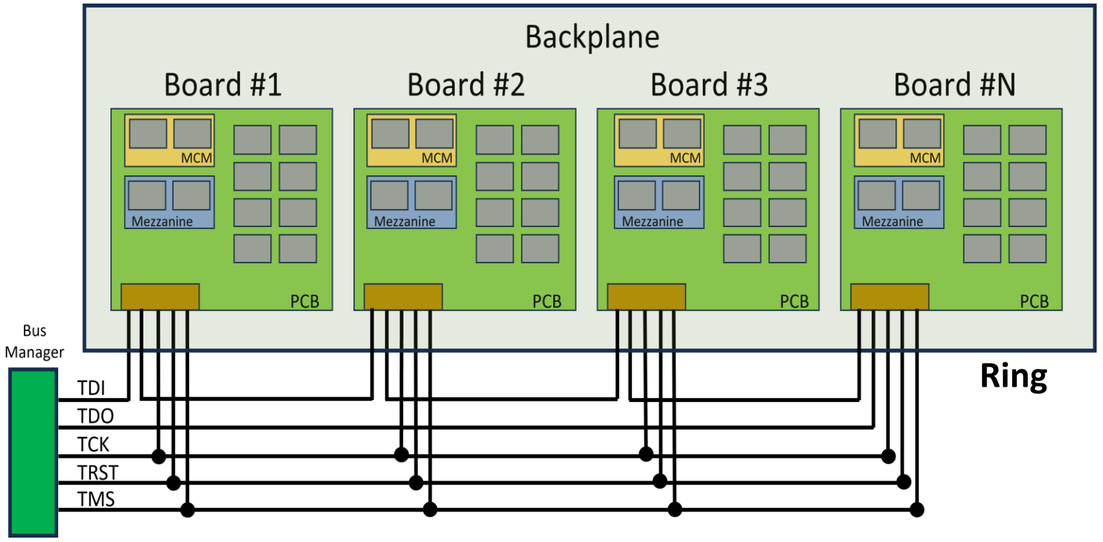


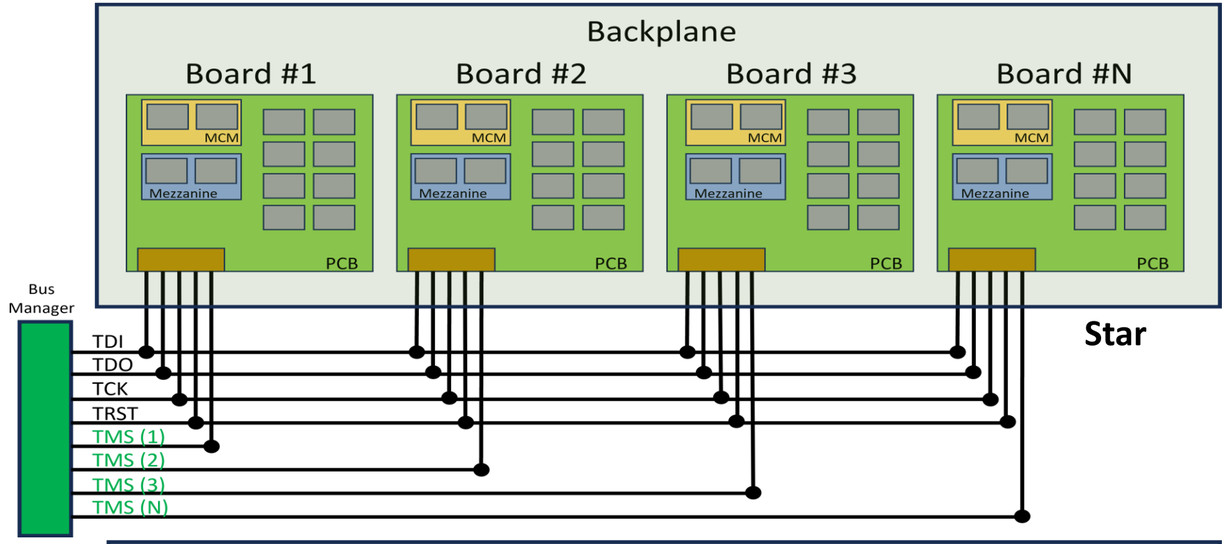
PCB Scan Chain (in red)

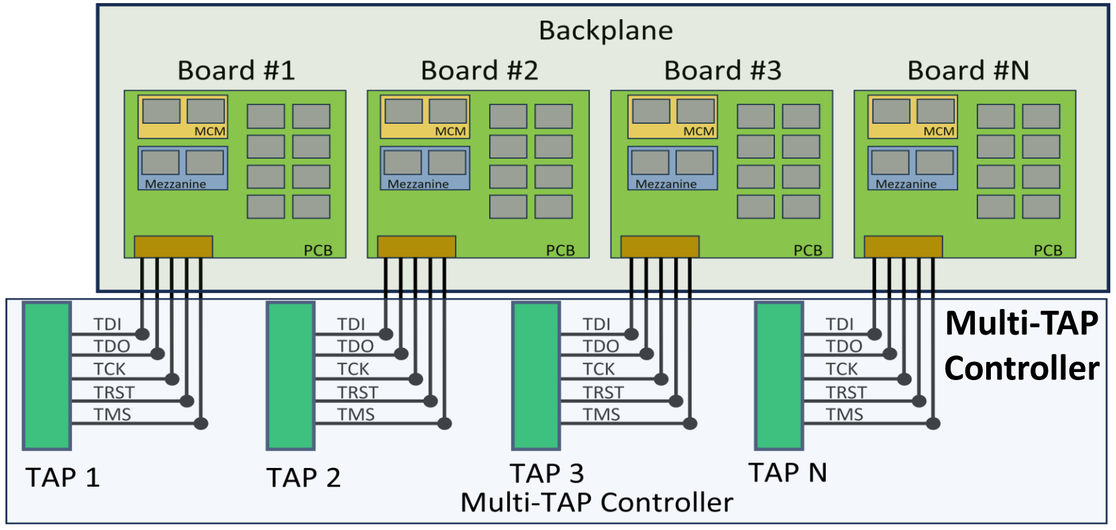


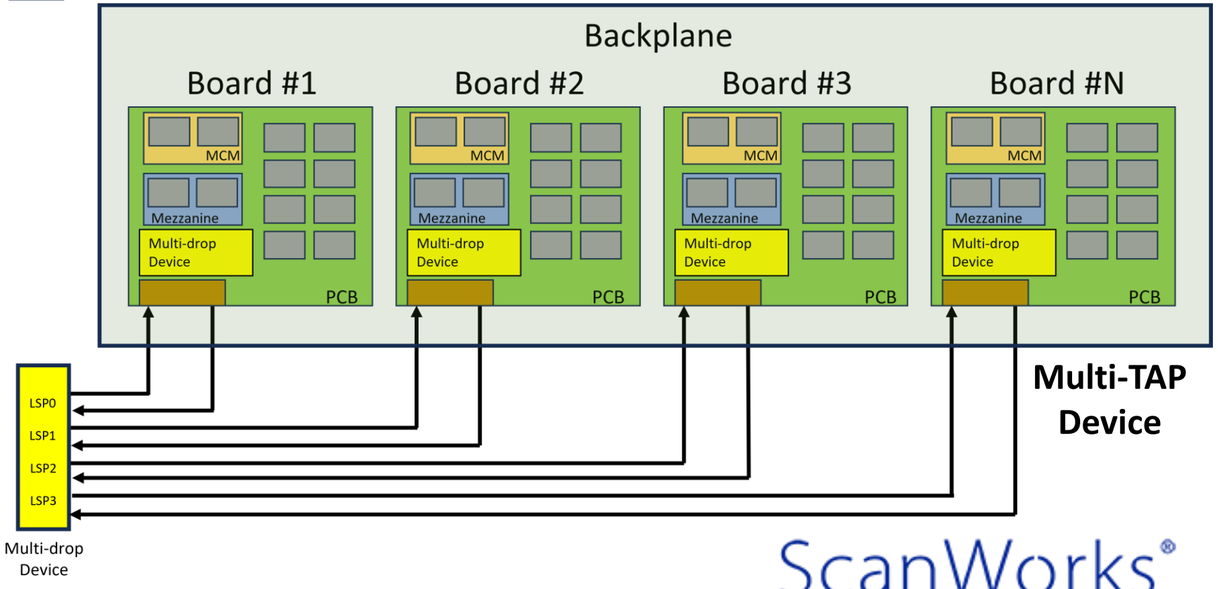
SJTAG Universe

System-Level JTAG Design – Webinar #3









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ScanWorks Dispatcher

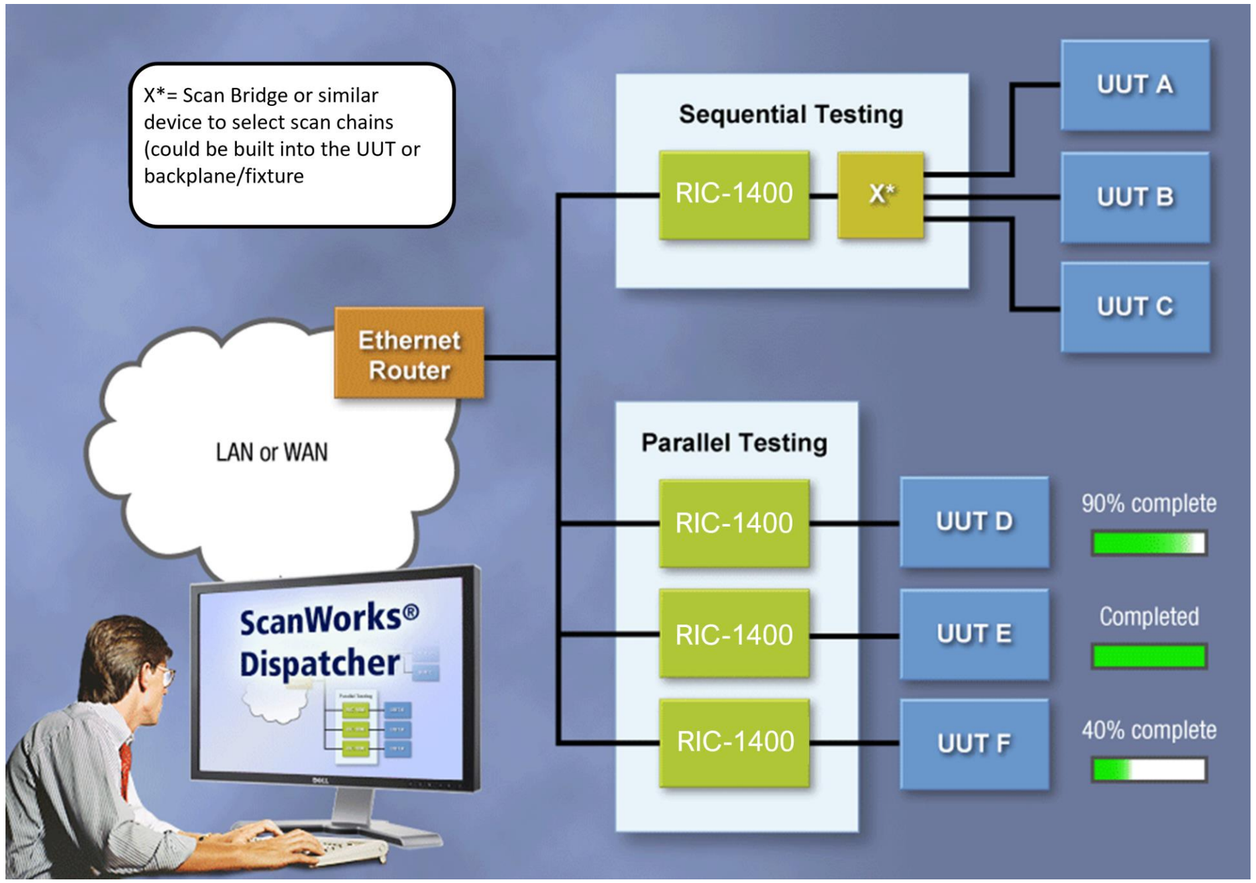
What Is ScanWorks Dispatcher?

- ScanWorks Dispatcher is a flexible, high-speed **parallel boundary-scan test** and in-system programming application system for high test throughput
- Example Use Cases:
  - High volume production test facilities
  - Programming multiple boards simultaneously
  - High-reliability HALT/HASS testing in environmental chambers

ScanWorks Dispatcher

What Can ScanWorks Dispatcher Do?

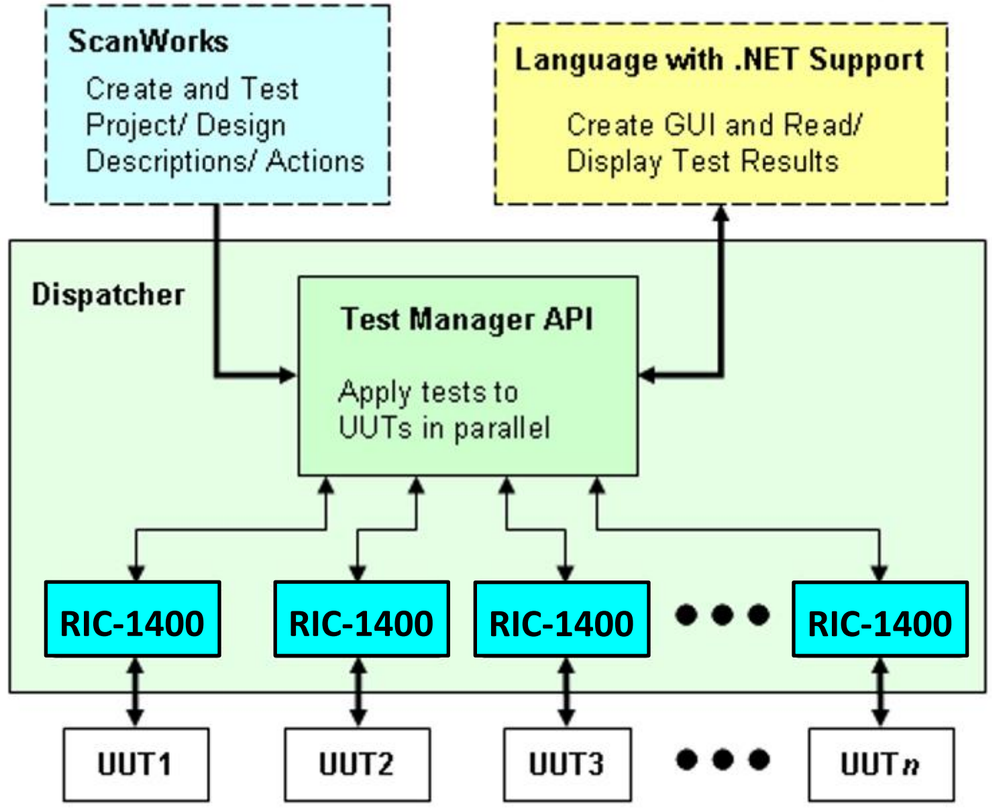
- Multiply production throughput by testing multiple UUTs in parallel
- UUTs may be identical or completely different
- Manage test results independently for each tester and each individual UUT
- Actions can be controlled individually or as a ScanWorks sequence
- Existing ScanWorks tests can be used with no modifications or special preparations
- Actions downloaded to on-board memory in specific RICs and are applied independently by processors in each RIC



ScanWorks Dispatcher

ScanWorks Dispatcher API

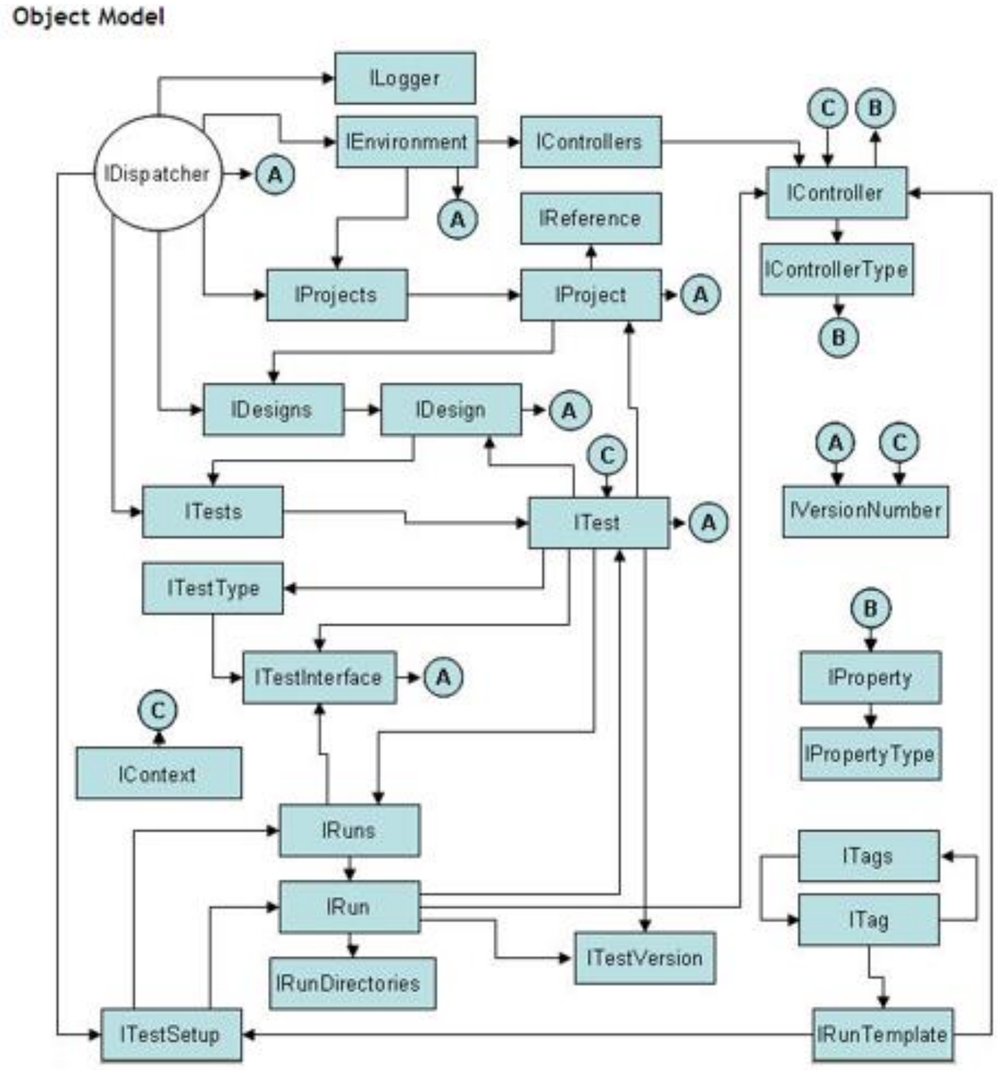
- Dispatcher provides an API designed to support custom test applications
- The API is a ".NET" API written in C# and compatible with most commonly used programming languages and with National Instruments LabVIEW and TestStand
- Dispatcher API includes complete documentation and example applications
- Dispatcher does not include an operator user interface, except for an authorization dialog and a hardware configuration dialog
- Dispatcher gives you the flexibility to test multiple UUTs simultaneously and asynchronously from your test executive



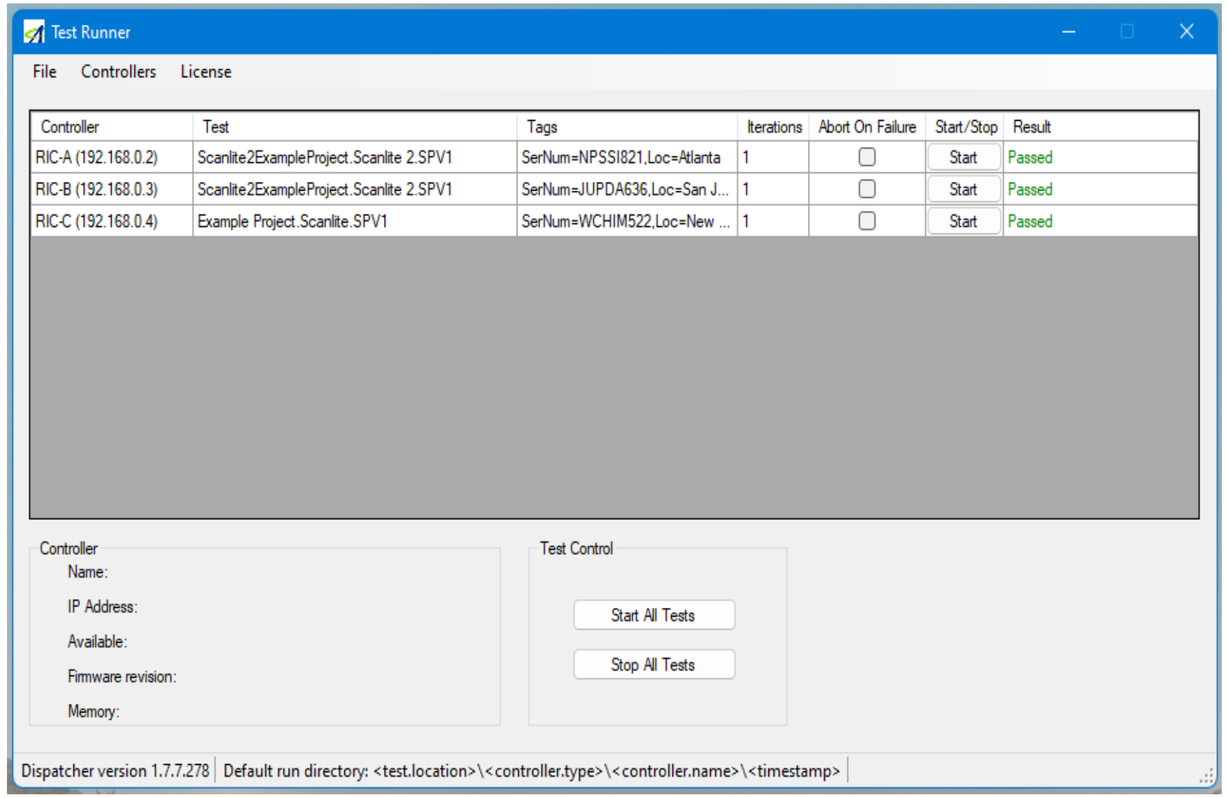
ScanWorks Dispatcher

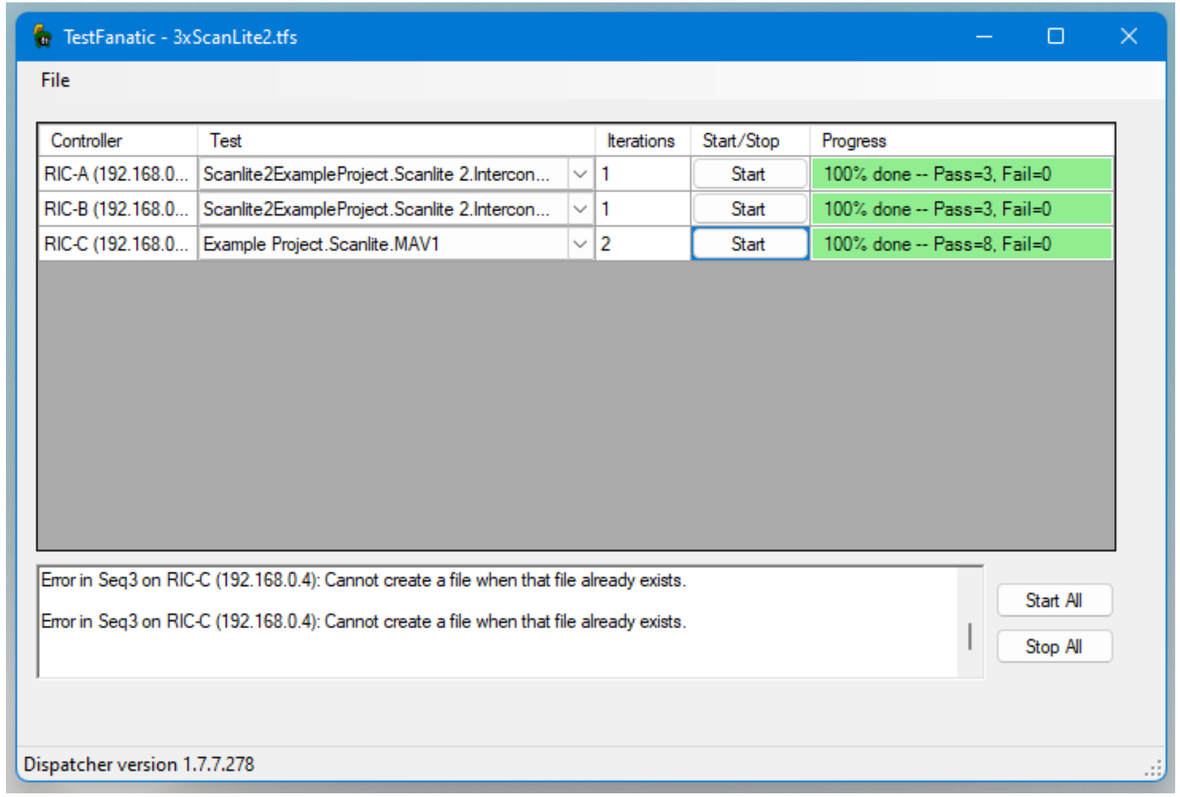
ScanWorks Dispatcher API Object Model

- The ScanWorks Dispatcher API provides access to everything you need for running and evaluating your boundary scan test



ScanWorks Dispatcher

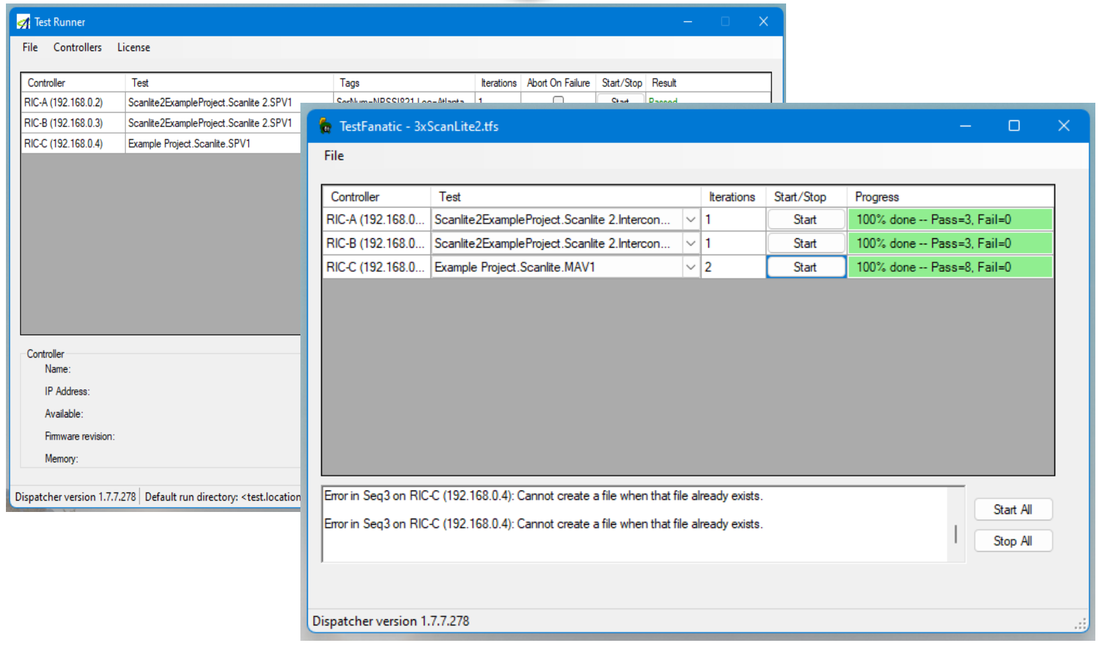




- Test Runner used to run single ScanWorks actions
- Test Fanatic used to run multiple ScanWorks actions in a sequence

Elements of a ScanWorks Dispatcher Deployment

- ScanWorks and Dispatcher software
- ScanWorks license with Dispatcher and Parallel Access addons
- Two or more Remote Instrumentation Controllers (RIC-1400)
- Test Runner, Test Fantic example application (supplied with Dispatcher), or other API created to apply test
- A previously created ScanWorks project compatible with the RIC-1400 as the controller



ScanWorks Dispatcher Demonstration

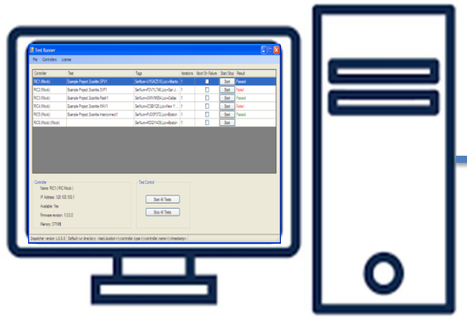
ScanLite2 – UUT A
192.168.0.2 – RIC A

ScanWorks 4.11.0
Dispatcher 1.7.7

Switch

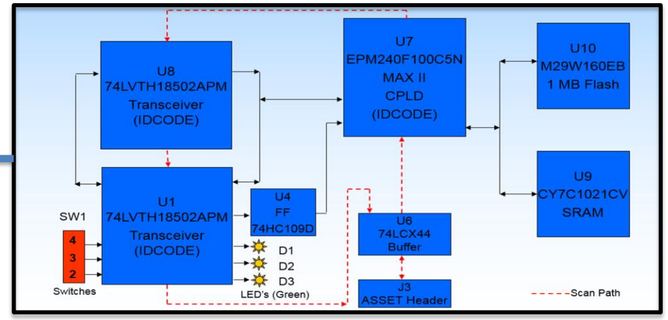
ScanLite2 – UUT B
192.168.0.3 – RIC B

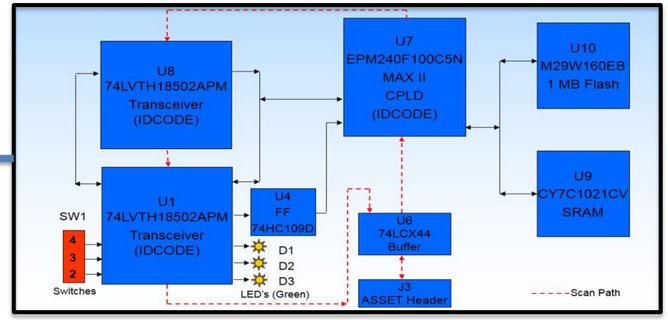
ScanLite – UUT C
192.168.0.4 – RIC C

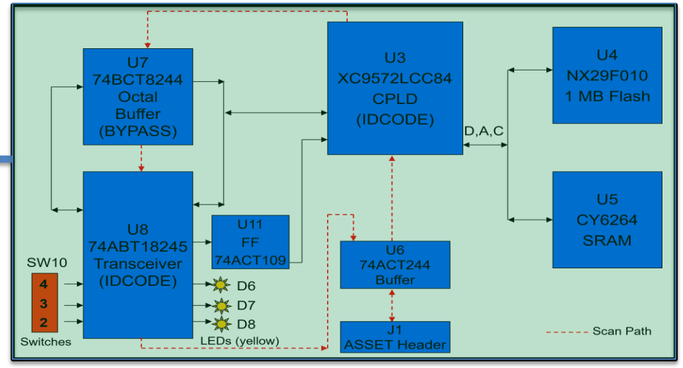


192.168.0.1

Test Runner
Test Fanatic







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ScanWorks Dispatcher Demonstration

UUT A & UUT B (Scanite2)

Fault Switch	Default Setting	Fault Setting	Fault Type
SW2	Norm	SA0	2 Drivers, 1 Receiver
SW3	Norm	SA0	1 Driver, 2 Receivers - Open
SW4	Norm	SA0	2 Drivers, 2 Receivers – 1 Pin Fail
SW5	Norm	SA0	TDO/TDI Error
SW6	Norm	SA1	Flip Flop Error
SW7	Norm	SA0	Memory – D0
SW8	Norm	Bridge	Flash Interconnect Fail
SW9	Norm	SA0	Memory – D1
SW10	Norm	Bridge	Address Fault
SW11	Norm	SA0	Short
SW12	Norm	Open	1 Driver, 1 Receiver
Data Switch	**Default Setting**		**Data Type**
SW1 (1-4)	Off	On	3- Bits of Test Stimulus Data for U1 and LED's

UUT C (ScanLite)

Fault Switch	Default Setting	Fault Setting	Fault Type
SW1	Norm	SA0	Address Fault
SW2 (1-4)	Norm	Open	Memory
SW4	Norm	SA1	2 Drivers, 2 Receivers
SW5	Norm	SA1	1 Driver, 2 Receivers
SW6	Norm	SA1	2 Drivers, 1 Receiver
SW7	Norm	Bridge	Open Fault
SW8	Norm	SA0	1 Driver, 1 Receiver
SW9	Norm	Bridge	Flip Flop Fault
SW11	Norm	Open	TDO/TDI Fault
Data Switch	**Default Setting**		**Data Type**
SW10 (1-4)	Logic O/Norm	Logic 1	3-Bits of Test Stimulus Data for U8 and for LEDs
Clock Switch	**Oscillator Disconnected**	**Oscillator Connected**	
SW3	On	Off	Clock

ScanWorks Dispatcher Demonstration

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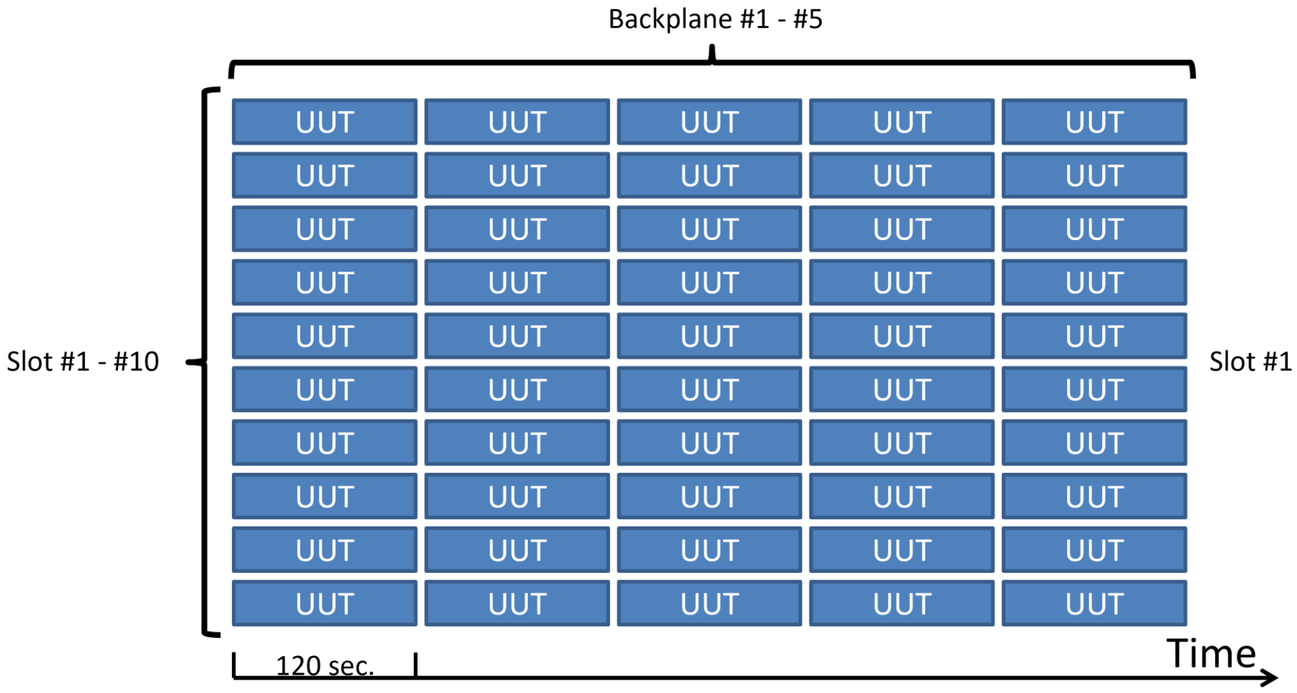
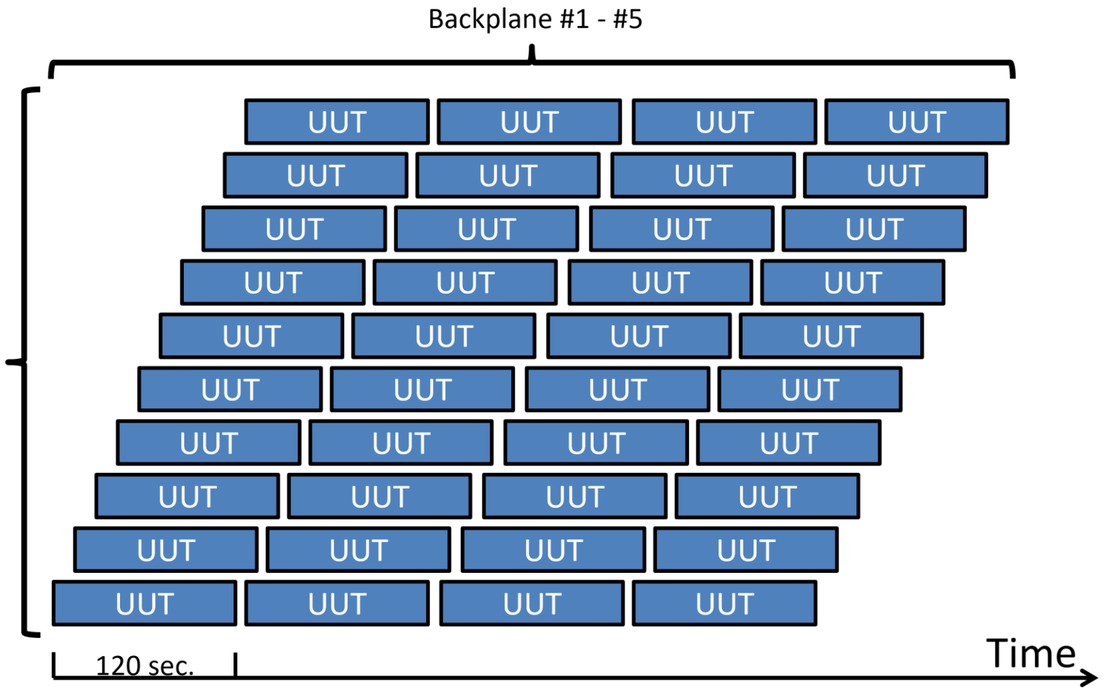
ScanWorks Dispatcher Use Cases

- Dispatcher manages the application of ScanWorks test and programming operations for many UUTs simultaneously
- Applications include high-throughput production and environmental test
- If Dispatcher is used with boards and backplanes implementing DFT guidelines and system-level JTAG designs, the test coverage and programming capabilities of ScanWorks Dispatcher expands tremendously

ScanWorks Dispatcher Use Cases





- High volume test and programming
- RIC-1400 per backplane
- Backplane designed with a JTAG system-level architecture (ex. Ring or Multi-TAP device)

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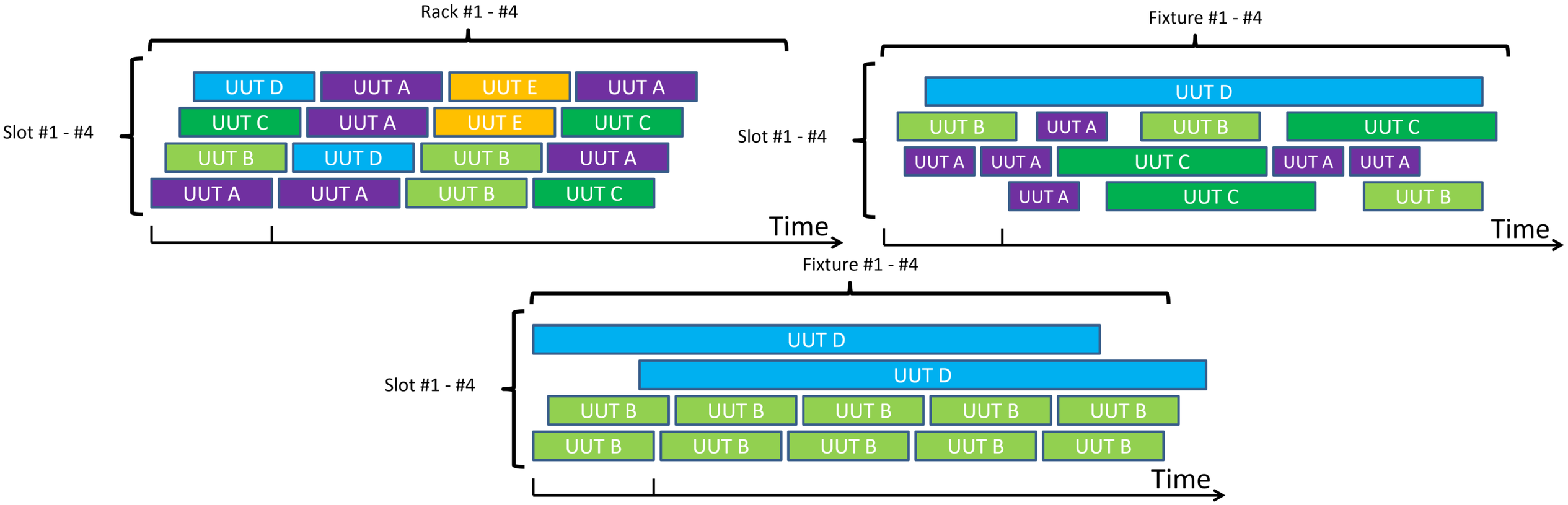
ScanWorks Dispatcher Use Cases



- Low volume-high mix test and programming/Mid-mix test and programming
- RIC-1400 per rack or fixture
- Backplane designed with a JTAG system-level architecture (ex. Ring or Multi-TAP device)

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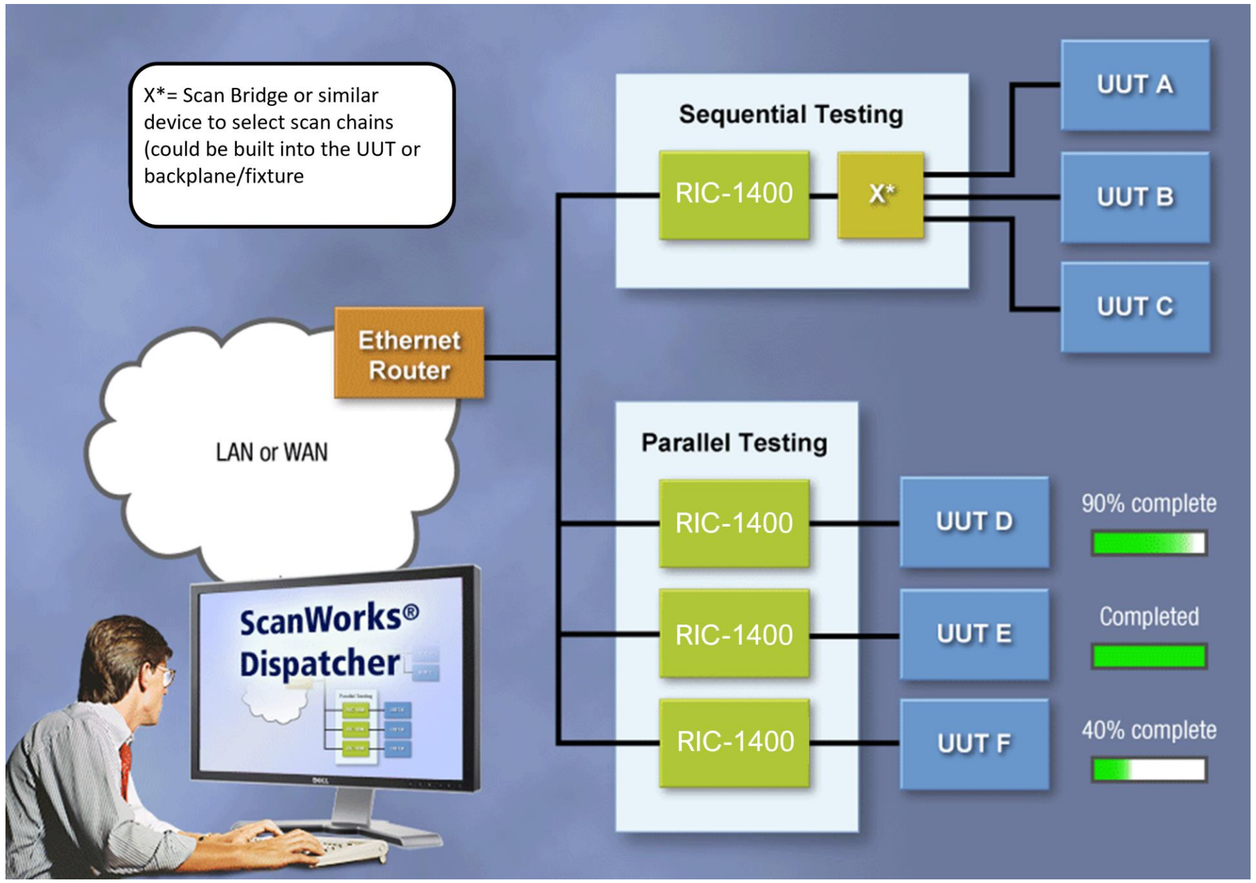
Summary

- ScanWorks Dispatcher is a solution for system-level parallel board test
- Multiply production throughput
- Remote test management
- Parallel test of different UUTs
- Parallel programming
- Remote diagnostics
- Backplane/Rack testing
- High-mix production
- High-volume Production
- Result files in XML
- Extensive .NET API



For More Information

- View the webinar, Guidelines for Board Design for Test (DFT) based on Boundary Scan Webinar #1, https://www.asset-intertech.com/wp-content/uploads/2022/12/Boundary-Scan-Design-for-Test.mp4
- View the webinar, Guidelines for Board Design for Test (DFT) based on Boundary Scan Webinar #2, https://www.asset-intertech.com/wp-content/uploads/2023/04/Boundary-Scan-Design-for-Test_-Part-2.mp4
- View the webinar, Guidelines for Board Design for Test (DFT) based on Boundary Scan Webinar #3, https://www.asset-intertech.com/wp-content/uploads/2023/08/System-level_JTAG_Webinar_v1.mp4
- Download the eBook, Testing DDR Memory with Boundary Scan/JTAG (Third Edition), https://www.asset-intertech.com/resources/eresources/ddr-memory-test-modern-tools-for-validation-test-and-debug/
- View the webinar, Squeezing Out More Test Coverage: Bridging the Gap Between Boundary Scan and Functional Test, https://www.asset-intertech.com/resources/videos/bridging-the-gap-between-boundary-scan-and-functional-test/

Questions and Contact Information

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