Real Insight from Code to Silicon

SourcePoint® ScanWorks®

Guidelines for System-level JTAG Design

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Guidelines for Board DFT based on Boundary Scan Webinar #1 & #2 recap

Guidelines for System-level JTAG Design

What is System-level JTAG Design?

System-level JTAG Design Architectures

System-level JTAG Design Multi-drop Devices

System-level JTAG Design Multi-TAP Controller

System-level JTAG Design Embedded Applications

Summary
Board DFT based on Boundary Scan - Webinar #1

- Why do we test?
- Test challenges
- Boundary Scan overview
- Boundary Scan device selection
- Focus on the Scan Chain design
- Accessing to the TAP
- Buffering the TAP
- Direct control of the system clock

- TCK and TMS distribution
- Pull-up/pull-down on TAP signals
- Board TRST
- Handle troublesome devices / different voltages
- Connector test
- Allow defeatable tied-off pins / unused boundary scan pins
- Introduction to testing memory devices/flash programming
- Bypass watchdog circuits

Covered in Board Design for Test (DFT) based on Boundary Scan Webinar #1
Board DFT based on Boundary Scan - Webinar #2

- Interconnect Testing
  - Cluster modeling
  - Using Discrete I/O
  - Controlling clocks
- Memory Interconnect Testing
  - Chip Enables
  - Flash Programming
  - Cell Z/Cell Active Configurations
- Testing with FPGAs
  - Pros/cons of testing unconfigured and configured

Covered in **Board Design for Test (DFT) based on Boundary Scan Webinar #2**
An electronic system is a group of interrelated devices, boards, and sub-assemblies that function together to accomplish a task.

At a fundamental level, testing a system’s structural integrity would involve verifying that each component is properly connected to all other components that require such connections.

System test is to verify the structural integrity and functionality at the level of the complex whole.
System-level JTAG (SJTAG) presumes that concept of applying JTAG to the individual boards of the target system has been embraced and implemented.

System-level creates a test access mechanism that extends the usefulness of JTAG throughout the entire product life-cycle.

System-level JTAG extends JTAG significantly beyond the traditional board-level scope of structural test and device programming.

The potential of SJTAG is illustrated by the Venn Diagram described as the SJTAG Universe.
System-level JTAG Design Architectures

Ring

- **Advantage**
  - Single Scan Chain per system with one access point
  - No special circuitry for the system boards themselves is required

- **Disadvantage**
  - One break in the Scan Chain will disable all Boundary Scan operations
    - Unless bypass circuitry is implemented
  - Slow access time for very long Scan Chain
  - Can only test as fast as the slowest board in the Scan Chain
Star

Advantage

- Allows boards to be tested independently
- A faulty board does not make the scan test for the other boards unusable

Disadvantage

- Can only test one board at a time
- Hardware must be designed to support Star architecture or additional devices are required to select TMS
- Cumbersome to implement in large multi-board systems
Multi-drop Device

- **Advantage**
  - Simple, single point of access on the backplane as Ring architecture
- **Disadvantage**
  - Requires additional devices placed on the board and/or backplane
Multi-drop Device

- SCANSTA112 7-Port Multi-drop 1149.1 (JTAG) Multiplexer
  - Create multiple Scan Paths (LSP0-LSP6)
  - Test individual boards and individual Scan Paths
  - Several types of multi-drop devices exist on the market for use
## System-level JTAG Design Architectures

### Multi-drop Devices

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Texas Instruments</td>
<td>Scan Path Linker (SPL) – SN54ACT8997</td>
</tr>
<tr>
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<td>Addressable Scan Port (ASP) – SN54ABT8996</td>
</tr>
<tr>
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<td>Linking Addressable Scan Port (LASP) – SN54LVT8986</td>
</tr>
<tr>
<td>National Semiconductor</td>
<td>Scan Bridge – SCANSTA111, SCANSTA112</td>
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<tr>
<td></td>
<td>Gateway – JTSO3, JTSO6</td>
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<tr>
<td>Lattice Semiconductor</td>
<td>BSCAN2 (Multiple Scan Port Linker)</td>
</tr>
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System-level JTAG Design Architectures

Multi-TAP Controller

- **Advantage**
  - Single point of access on the backplane for each board in the system

- **Disadvantage**
  - Requires multi-TAP controller and backplane design considerations
Multi-TAP Controller

- **PCle-410**
  - ScanWorks supports up to 3 PCIe-410 cards installed within a desktop PC
  - Each 410 pod connects to a PCIe card and has 4 TAPs
  - 12 TAPs for system-level JTAG testing
## System-level JTAG Design Architectures Summary

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ScanWorks Embedded Diagnostics (SED) for Test

- JTAG is typically used “locally” for board test development, production and system debug with a dedicated bus manager
- Since JTAG is software that leverages on-chip embedded logic, it is possible to port that application directly onto the board itself (SoC)
- SED for Test eliminates the need for bus manager, cables, and fixturing for JTAG testing
- SED for Test creates a “remote” JTAG/boundary-scan test and programming application
- Embedded Boundary Scan directly on the board/system
System-level JTAG Design Embedded Applications

SED for Test

- Test vectors are stored locally on the system
- Expands the universe of testing (ex. in-system structural testing, in-system programming, in-situ diagnostics, etc.)
- Addresses intermittent faults and “No Fault Found” (NFF) issues
- Creates a powerful BIST without external hardware that can be used throughout the entire lifecycle of the board/system
SED for Test

- The resources required for the TAP Controller IP are small when compared to today’s FPGAs
  - Uses < 4,000 Lookup Tables (LUTs)
  - Uses less than < 75kb memory
- Action players run on the CPU
  - Occupies < 2MB flash footprint
- Action data
  - Occupies ~ 300kB (typical) to >~1MB (for large designs)
SED for Debug

- Remote Host – running Intel® Customer Scripts (Cscripts)

- On-Target Diagnostics (OTD) – applications on Baseboard Management Controller (BMC) invoking debug/run-control autonomously:
  - Speed
  - Scalability
  - Security
SED for Built-in Self Test

- In the most general case, system-level access to BIST can be mediated via any on-chip or off-chip processor
- Provides test, debug, and validation support at-scale
- Industry standard IEEE 1687 (IJTAG) for access and control of embedded instruments (MBIST, Logic Test, IO BIST, Scan Test, Array Freeze & Dump, etc.)
- Unparalleled insight into IC, board and system internals and their impacts on planetary-scale computing
Guidelines for System-level JTAG Design

**Summary**

- Guidelines for System-level JTAG Design
  - What is System-level JTAG Design?
    - System-level JTAG, or SJTAG, expands the application potential of JTAG significantly beyond the traditional board-level scope of structural test and device programming
  - System-level JTAG Design Architectures
    - Ring and Star
  - System-level JTAG Design Devices and Controller
    - Multi-drop devices – Scan Path Linkers
    - Multi-TAP Controller – PCIe-410
  - System-level JTAG Design Embedded Applications
    - SED for Test, SED for Debug, SED for Built-in Self-Test
View the webinar, Guidelines for Board Design for Test (DFT) based on Boundary Scan Webinar #1, https://www.asset-intertech.com/wp-content/uploads/2022/12/Boundary-Scan-Design-for-Test.mp4

View the webinar, Guidelines for Board Design for Test (DFT) based on Boundary Scan Webinar #2, https://www.asset-intertech.com/wp-content/uploads/2023/04/Boundary-Scan-Design-for-Test_Part-2.mp4

Go to the blog series, Everything You Need to Know About ScanWorks Interconnect Blog Series, https://www.asset-intertech.com/resources/blog/2022/09/everything-you-need-to-know-about-scanworks-interconnect-part-1/


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