Agenda

- Guidelines for Board DFT based on Boundary Scan Webinar #1 Recap
- Guidelines for Board DFT based on Boundary Scan Webinar #2
  - Interconnect Testing
  - Memory Interconnect Testing
  - Flash Programming
  - Testing with FPGAs
Board DFT based on Boundary Scan - Webinar #1

- Why do we test?
- Test challenges
- Boundary Scan overview
- Boundary Scan device selection
- Focus on the Scan Chain design
- Accessing to the TAP
- Buffering the TAP
- Direct control of the system clock

- TCK and TMS distribution
- Pull-up/pull-down on TAP signals
- Board TRST
- Handle troublesome devices / different voltages
- Connector test
- Allow defeatable tied-off pins / unused boundary scan pins
- Introduction to testing memory devices/flash programming
- Bypass watchdog circuits

Covered in Board Design for Test (DFT) based on Boundary Scan Webinar #1
Interconnect testing identifies shorts and opens on printed circuit boards

Utilizes the embedded instrumentation Boundary Scan cell capability to drive and receive test stimulus on the board nets

Goal is to maximize test coverage between Boundary Scan to Boundary Scan devices and between Boundary Scan and non-Boundary Scan devices
Connect Boundary Scan pins to Chip Enables of non-Boundary Scan devices as a method of control.
ScanWorks Interconnect test coverage is increased by adding ASSET Cluster Models.

Language created by ASSET

Describes the I/O characteristics of non-Boundary Scan devices

Consist of simple keywords such as DRIVE, SENSE, JOIN, EQUAL...more

Consist of PART sections which multiple functions of the non-Boundary Scan device

Cluster models are assigned to non-Boundary Scan devices through the Model Device Browser

Cluster models describe how to test through non-Boundary Scan devices or disable the outputs of non-Boundary Scan devices

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Cluster Model Example

```plaintext
#VECTOR a1 47, 46, 44, 43
#VECTOR b1 2, 3, 5, 6
!-----------------------------------------------------

#PART dis ! whole device disabled
1    DRIVE 1 ! disable part1
48   DRIVE 1 ! disable part2
25   DRIVE 1 ! disable part3
24   DRIVE 1 ! disable part4
!-----------------------------------------------------

#PART a2b ! part1 transfer
1    DRIVE 0 ! enable part1
b1   EQUAL a1
```

Cluster Model (partial) for 16-Bit Line Driver
Where Boundary Scan access to a non-Boundary Scan device hasn’t been designed in, an alternative is to provide access via a discrete I/O signal.
Interconnect Testing with Boundary Scan

- Design access to all Chip Selects and Output Enables of non-Boundary Scan Devices

Employ Unassigned FPGA Boundary Scan Pins

Boundary Scan Device

Non-Boundary Scan Devices

<table>
<thead>
<tr>
<th>Spare Boundary Scan Pins</th>
<th>Outputs OZ to be driven by other Boundary Scan devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS, OE</td>
<td>Memory banks</td>
</tr>
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</tr>
<tr>
<td>CS, OE</td>
<td>I/O Interfaces</td>
</tr>
<tr>
<td>EN, DIR</td>
<td>Buffers</td>
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<tr>
<td>CS</td>
<td>Other digital</td>
</tr>
<tr>
<td>CS, PwrDwn</td>
<td>Telecommunications</td>
</tr>
<tr>
<td>CS, PwrDwn</td>
<td>Mixed signal</td>
</tr>
</tbody>
</table>
Controlling clocks reduces noise on the board and prevents false fails.
Connectors are opens – use loopback connectors

- Build a connector loopback or a mating plug/socket that wires nets together
- Add an ASSET CIOM-100 for better shorts and opens testing
Memory Interconnect Testing with Boundary Scan

- Boundary Scan device or devices connected to memory control, address and data signals
- Test vectors are shifted into Boundary Scan devices connected to memory devices that create read/write cycles
- Test for shorts and opens on control, address, and data signals of memory devices
Provide access to all memory signals

- Design in access to Chip Enables of memory devices
Following proper DFT can reduce the number of cycles needed to program flash devices which decreases the programming time.

No external programmers are needed when using Boundary Scan.
To program flash you must have access to all address, data and control signals.
Provide access to all flash signals

External, Cell Active Configuration: Use an ASSET hardware controller to toggle WE with the Boundary Scan pin held high
Provide access to all flash signals

- External, Cell Z Configuration: Use an ASSET hardware controller to toggle WE with the Boundary Scan pin held at HI-Z
Testing FPGAs with Boundary Scan

- Unconfigured vs. configured
- Differential circuits

What does the FPGA drive or sense?
- FPGA outputs may damage the surrounding circuitry
- FPGA inputs may not meet the expected thresholds leading to false fails

Unconfigured FPGA
Technology mismatch problem

Wrong output voltage causes damage
Wrong input threshold causes test fails
FPGAs Support Many I/O Technologies

- Technology
  - LVTTTL
  - LVCMOS
  - HSTL
  - LVPECL
  - LVDS

- Voltages
  - 3.3
  - 3.3, 2.5, 1.8, 1.5
  - 1.5
  - Current
  - Current
Check the datasheet for the default technology of unconfigured FPGAs
In an unconfigured FPGA, Boundary Scan has access to all 4 pads: D1, D2, S1 and S2
In an unconfigured FPGA, D1 can be driven and sensed on D2
In an unconfigured FPGA, D2 can be driven and sensed on D1
Testing FPGAs with Boundary Scan

Access to dangling differential pair

- In an unconfigured FPGA, S1 can be driven and sensed on S2
- In an unconfigured FPGA, S2 can be driven and sensed on S1
Considerations when conducting Boundary Scan testing with unconfigured FPGAs

- Assess risk to surrounding devices
- Access to differential pairs
- Access to dangling differentials
Testing FPGAs with Boundary Scan

- How do you conduct Boundary Scan testing with a configured FPGA?
- The FPGA vendor should have tools to generate a post-configuration BSDL file
Many designs have multiple configurations for the same FPGA
Testing FPGAs with Boundary Scan

- Boundary Scan testers can interrogate the User Code before testing to ensure that the expected configuration is the one actually in place.
Testing FPGAs with Boundary Scan

- Patterns can be driven into D1 and sensed at S1 so the pair can be tested.
- If the test fails we cannot diagnose the fault to the pin level.
No test of dangling differential driver

- Patterns can be driven into D1 but there is no way to sense them

Configured FPGA
No test of dangling differential sensor

- Patterns can be sensed out of S1, but there is no way to drive them
- Testing with configured FPGAs can reduce test coverage
Issues to consider when conducting Boundary Scan testing with configured FPGAs

- Vendor BSDL is no longer valid after configuration
- Which configuration is present in the FPGA?
- No access to differential pairs
- No test of dangling differentials
Should you test FPGAs configured or unconfigured?

- There is no clear answer
- Consider configured for pass/fail and unconfigured for diagnosing fails
- If testing unconfigured consider the issues discussed (e.g. potential damage to surrounding devices)
Summary of Board DFT based on Boundary Scan

- Interconnect Testing
  - Maximizing coverage with cluster models
  - Maximizing coverage with discrete I/O
  - Employing unassigned Boundary Scan pins for control of non-Boundary Scan devices
  - Controlling clocks to minimize noise
  - Loopbacks for extended Boundary Scan testing

- Memory Interconnect Testing
  - Provide access to all Control, Address, and Data pins

- Flash Programming
  - Provide access to all Control, Address, and Data pins
  - Use external access methods to reduce programming time

- Testing with FPGAs
  - Considerations for testing FPGAs unconfigured or configured
  - Technology mismatch
  - Differential drivers and receivers
For More Information

- View the webinar, Guidelines for Board Design for Test (DFT) based on Boundary Scan Webinar #1, [https://www.asset-intertech.com/wp-content/uploads/2022/12/Boundary-Scan-Design-for-Test.mp4](https://www.asset-intertech.com/wp-content/uploads/2022/12/Boundary-Scan-Design-for-Test.mp4)
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