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Guidelines for Board Design for Test (DFT) based on Boundary Scan

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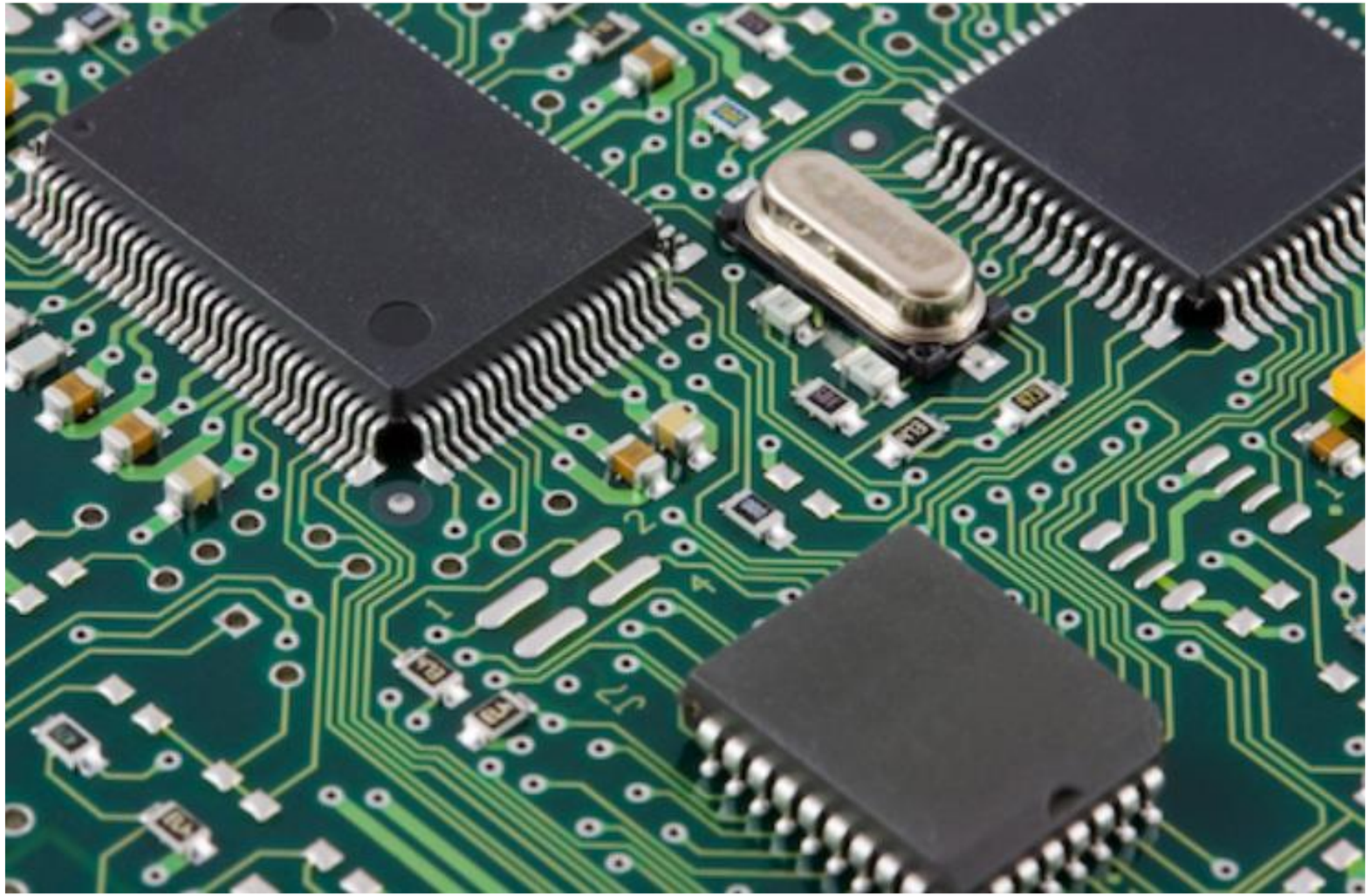
November 09, 2022

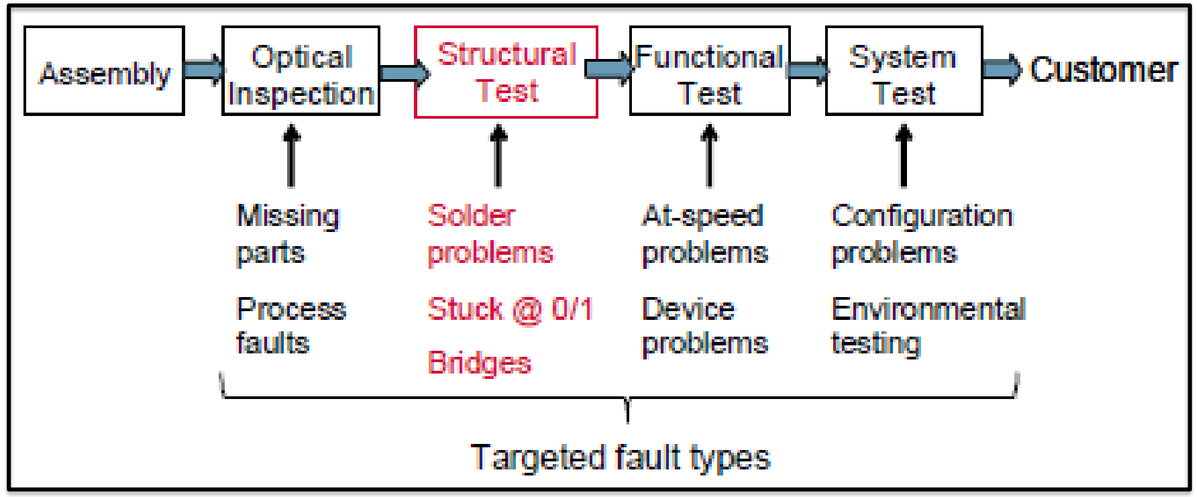
Agenda

- Why Do We Test?
- Board Test Challenges
- Boundary Scan Overview
- Board DFT based on Boundary Scan Guidelines



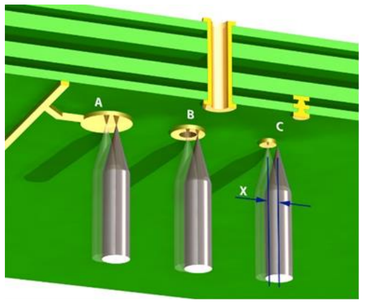
Why Do We Test?

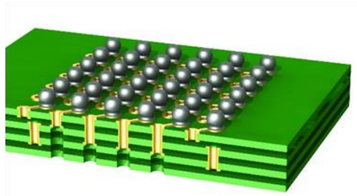
- Ensure the final product works as expected
- Identify problems (early) during the manufacturing process
- Problems are more expensive to correct later in manufacturing process
- Implementing design for test (DFT) based on boundary scan guidelines during board design increases boundary scan testability during the manufacturing step

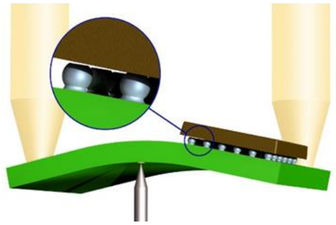


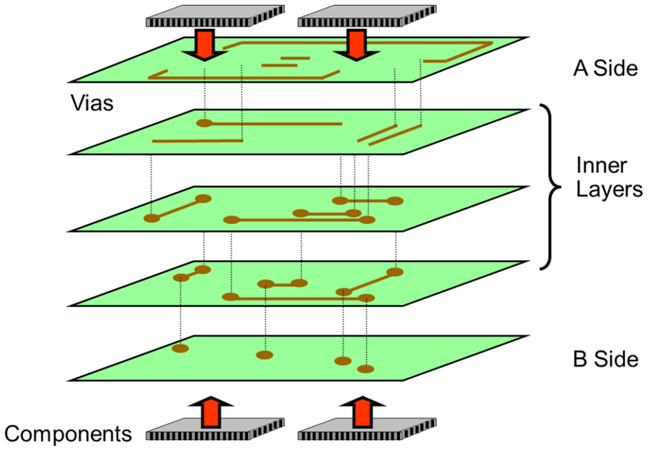
Board Test Challenges

- PCB issues
  - Fine pitch packages
  - High density interconnects
  - Blind and buried vias
  - BGAs
  - Heat sinks
  - Conformal coating
  - AC-coupled nets
  - High-speed serial I/Os
  - Inaccessible nodes
- Cost issues
  - High-priced test equipment and machinery
  - Substantial machinery life-cycle cost
  - Expensive bed-of-nail fixtures



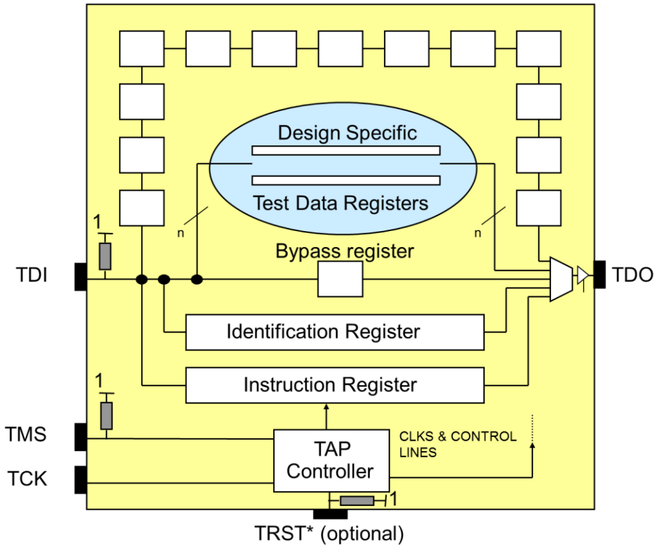


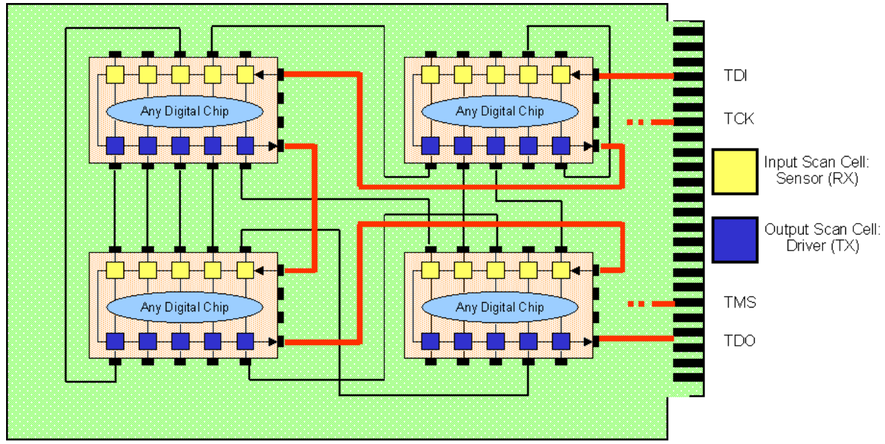




Boundary Scan Overview

- Boundary scan is a static, vector-based test technology implemented through on-chip embedded instruments within commercial silicon
- Utilizes embedded cells and registers to drive/receive stimulus data across the PCB
- Detects shorts/opens/stuck-at faults with diagnostics to the device and net/pin level
- A proven and mature structural test and programming technology





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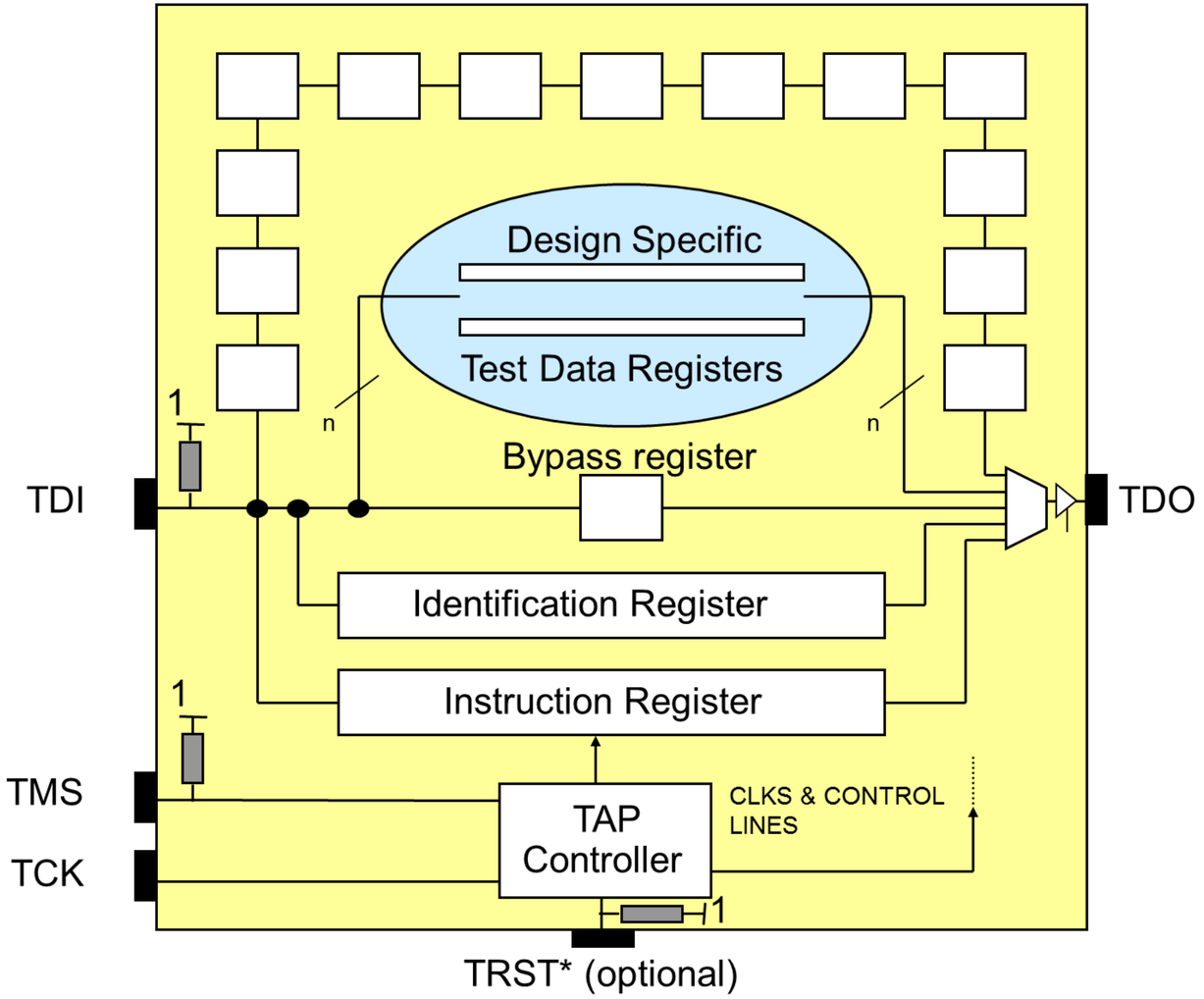
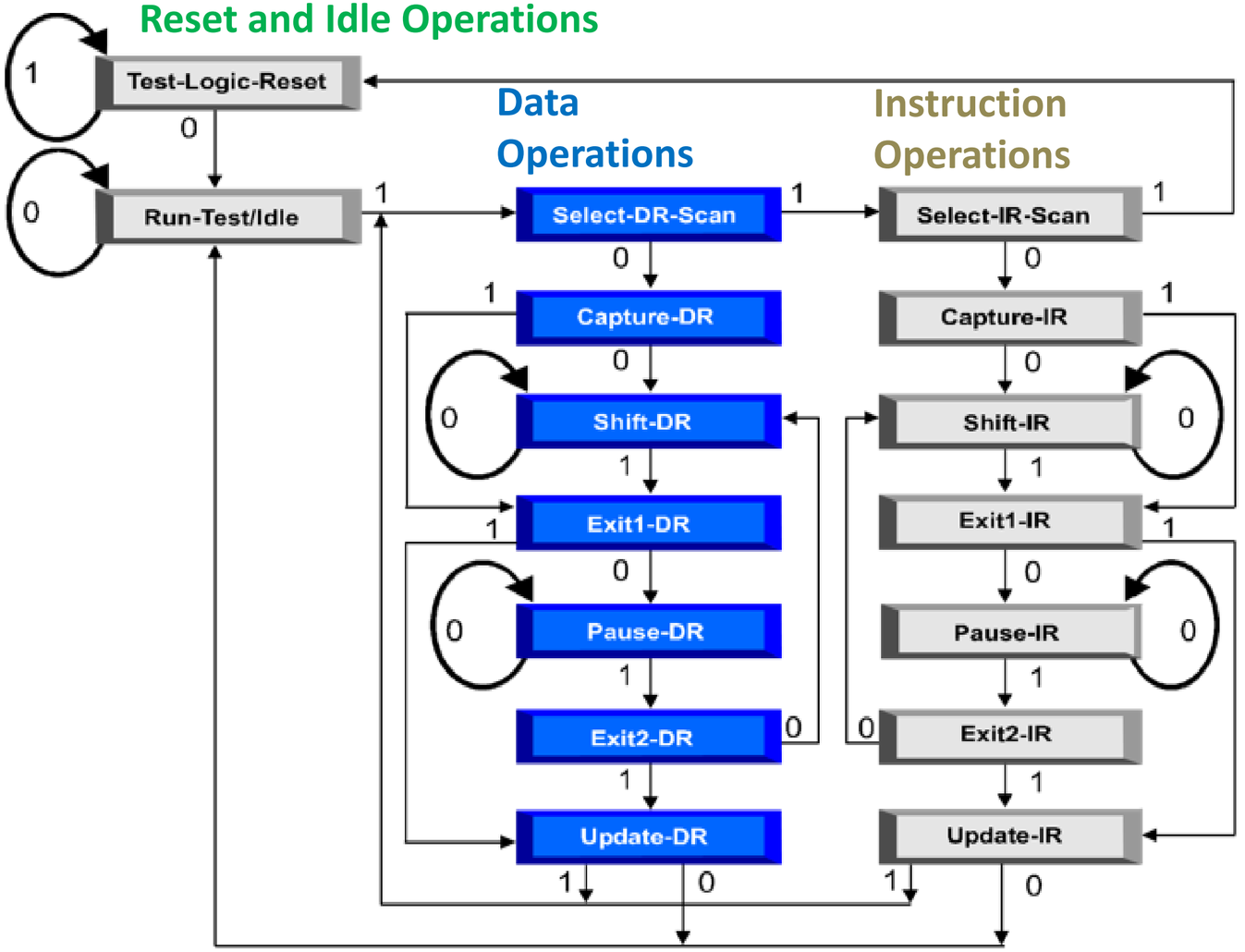
Boundary Scan Overview

- Test Data In (TDI)
  - Serial data in sampled on rising edge (Default =1)
- Test Data Out (TDO)
  - Serial data out sampled on falling edge (Default =Z)
- Test Mode Select (TMS)
  - Input control sampled on rising edge (Default =1)
- Test Clock (TCK)
  - Any frequency
- TRST Reset (TRST*)
  - Optional async reset active low (Default =1)



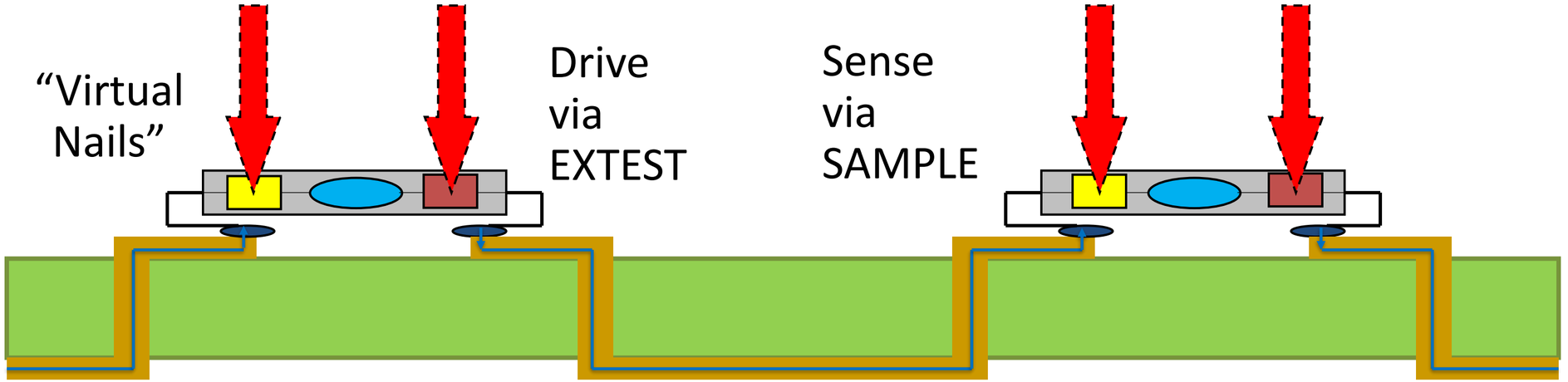
Boundary Scan Overview

- The TAP Controller is synchronous finite state machine that responds to TMS and TCK signals
- Provides four major operations
  - Reset
  - Run Test/Idle
  - Scan-DR
  - Scan-IR
- Scans consist of
  - Capture
  - Shift
  - Update



Boundary Scan Overview

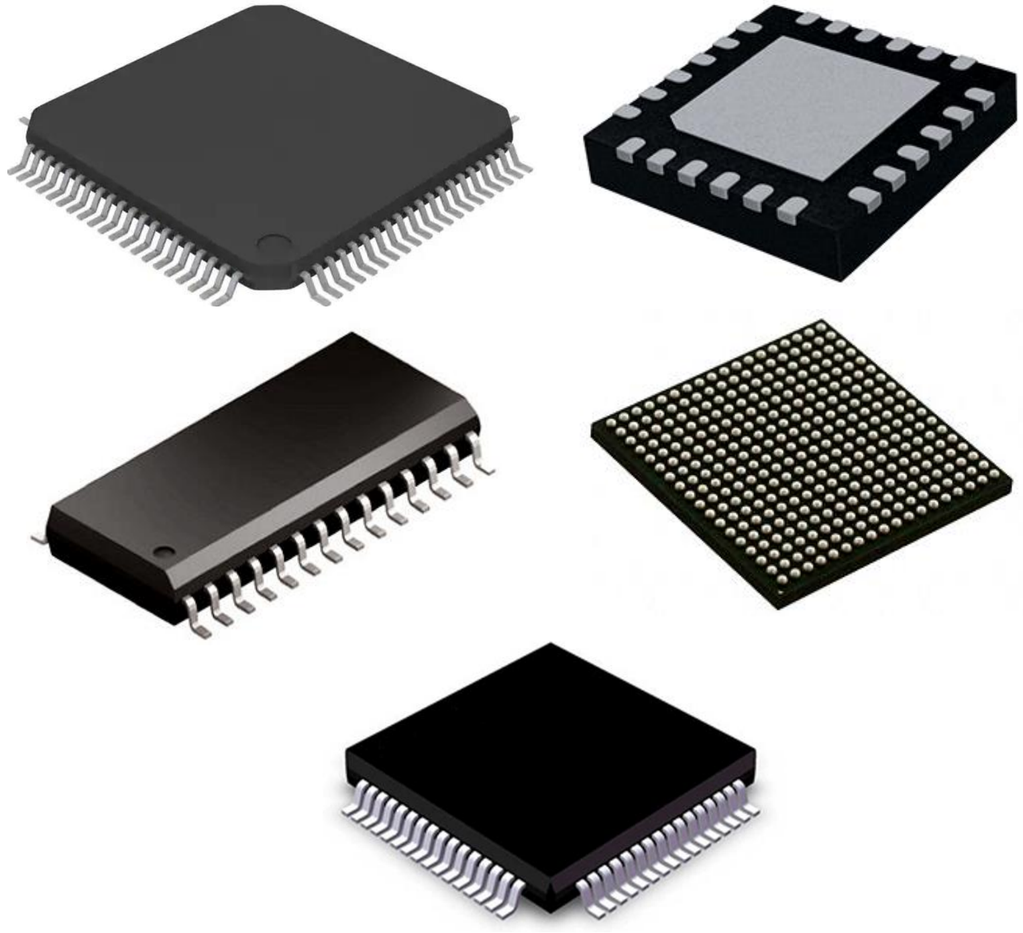
- Boundary Scan provides virtual electronic probing with fault detection/reporting to the net and pin level



In this mode (EXTEST), defects covered:
driver (TX) scan cell → driver amp → bond wire → leg → solder interconnect
solder → leg → bond wire → sensor amp → sensor (RX) scan cell

Boundary Scan Device Selection

- Select as many IEEE 1149.1 **compliant** devices for the board as possible
- Consider putting logic (combinatorial and sequential) into PLDs/FPGAs
- Obtain accurate BSDL files from the device manufacturer
- Validate BSDL files (use ASSET's online BSDL Validation Service)
- Check state of Compliance Pins in the Boundary Scan Description Language (BSDL) file



Boundary Scan Device Selection

- Mandatory Instructions
  - BYPASS
  - EXTEST
  - SAMPLE
  - PRELOAD
- Optional Instructions
  - INTEST
  - RUNBIST
  - CLAMP
  - HIGHZ
  - IDCODE
  - USERCODE

Mandatory Instructions	Description
BYPASS	Places the single-bit data register to be connected between TDI and TDO. Serial data bypasses the Boundary Scan Register.
EXTEST	Places the Boundary Scan Register to be connected between TDI and TDO. Test interconnects between Boundary Scan devices.
SAMPLE	Places the Boundary Scan Register to be connected between TDI and TDO. Allows the device to remain in functional mode. Samples device I/O signals.
PRELOAD	Places the Boundary Scan Register to be connected between TDI and TDO. Allows the device to remain in functional mode. Shifts patterns to Boundary Scan devices while in functional mode.
Optional Instructions	**Description**
INTEST	Places the device in an internal boundary test mode and selects the boundary scan register to be connected between TDI and TDO.
RUNBIST	Places the device in self-test mode, enable a comprehensive self-test of its core logic and selects a user-specified data register to be connected between TDI and TDO.
CLAMP	Sets the outputs of the device to logic levels determined by the contents of the boundary scan register and selects the bypass register to be connected between TDI and TDO.
HIGHZ	Sets all of the device outputs to a disabled (high-impedance) state and selects the bypass register to be connected between TDI and TDO.
IDCODE	Allows the device to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO.
USERCODE	Allows the device to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. Captures user-defined information about the device.

Boundary Scan Device Selection

- Allow direct access to Compliance Pins of Boundary Scan devices
  - These pins must be kept in a specified state for the device to meet the IEEE 1149.1 standard

```
attribute COMPLIANCE_PATTERNS of XA7A35T_CPG236: entity is --
"(PROGRAM_B) (1)";
```

Boundary Scan Device Selection

- Choose Boundary Scan devices which support Identification Code

```
attribute IDCODE_REGISTER of EPM240F100 : entity is
 "0000"&                --4-bit Version
  "0010000010100001"&   --16-bit Part Number (hex 20A1)
"00001101110"&          --11-bit Manufacturer's Identity
 "1";                   --Mandatory LSB
```

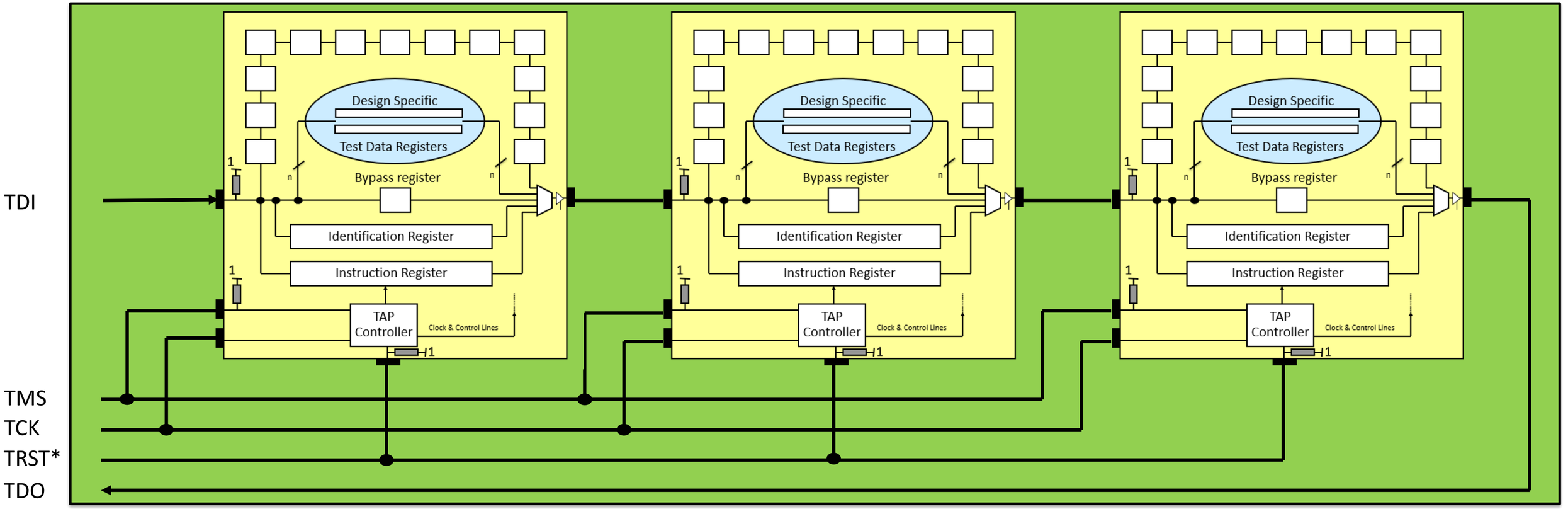
Boundary Scan Device Selection

- Examine the BSDL for TCK speed of each device
  - Device 1
    - attribute TAP_SCAN_CLOCK of TCK :
    - signal is (33.0e6, BOTH);
  - Device 2
    - attribute TAP_SCAN_CLOCK of TCK :
    - signal is (2.0e6, BOTH);
  - Device 3
    - attribute TAP_SCAN_CLOCK of TCK :
    - signal is (20.0e6, BOTH);
- Maximum TCK rate for this scan chain will be 2MHz

Boundary Scan Device Selection

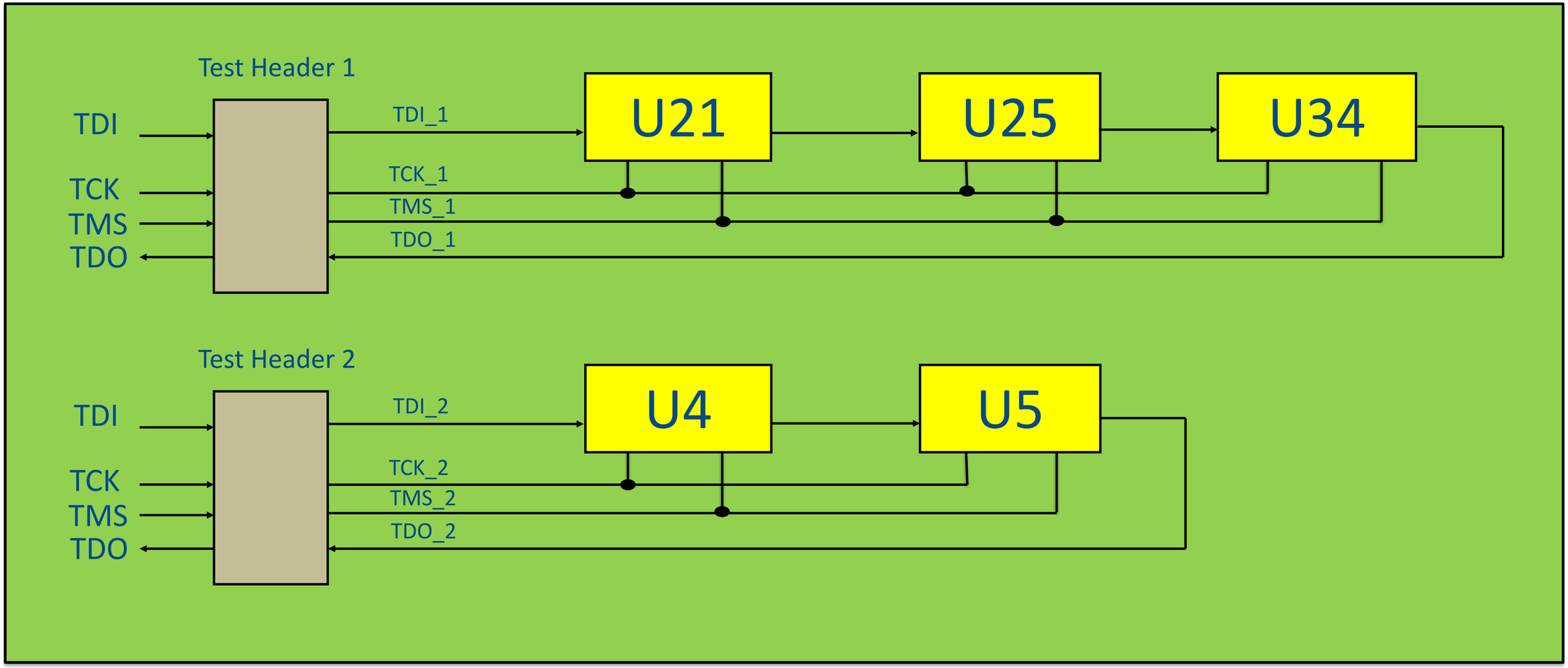
```
-- BSDL file for device XCR3032A, package PC44
-- Xilinx, Inc. $State: ADVANCED $ $Date: 2000-07-27 10:00:39-07 $
--
-- IMPORTANT NOTE  WARNING !!
-- ************************************************************
--     Boundary registers as called out by this file do not exist!
--     They must be described for  BSDL Compliance. Extest and
--     Preload commands do not exist nor function.  If either of
--     those commands are selected, the bypass register will be
--     used.
--
```

Simple Scan Chain Design



- Check that all boundary scan devices are connected in a scan chain
- Check that the scan path is unbroken from TDI to TDO

Complex Scan Path Design



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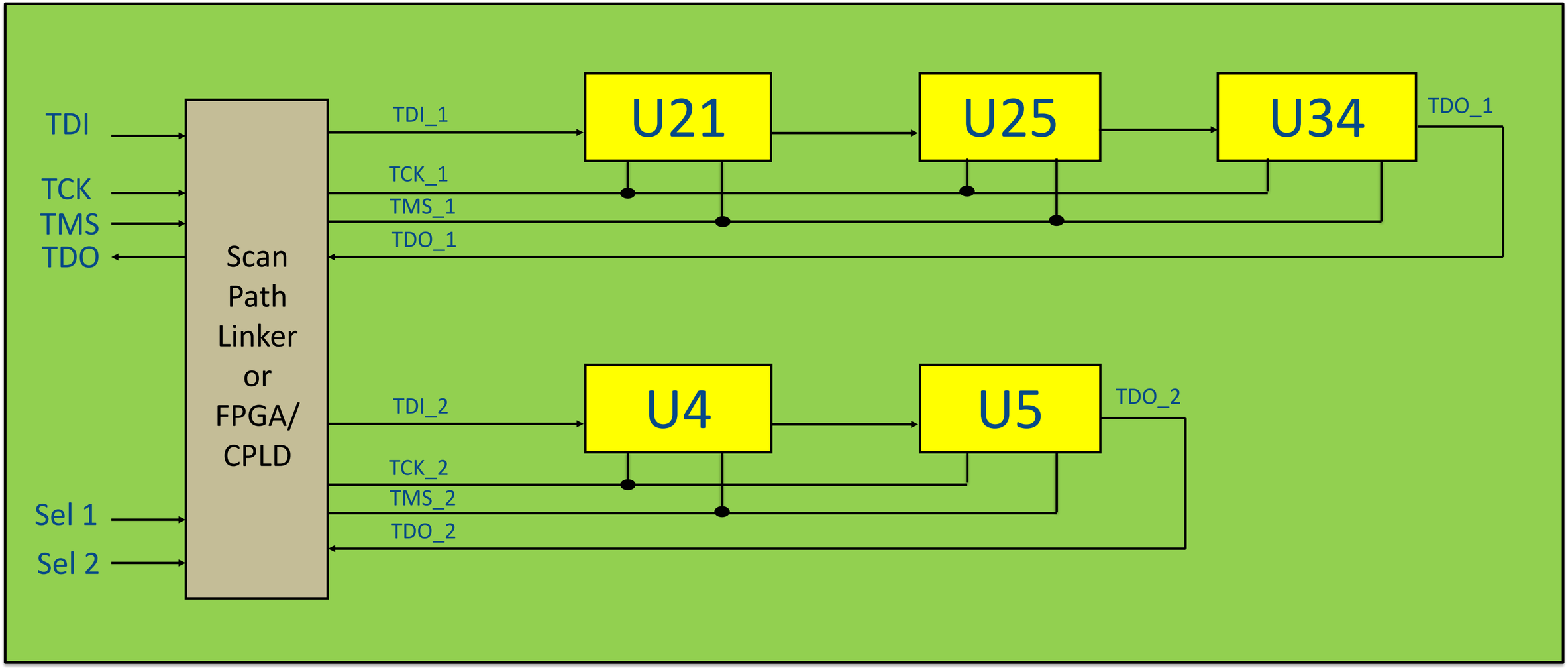
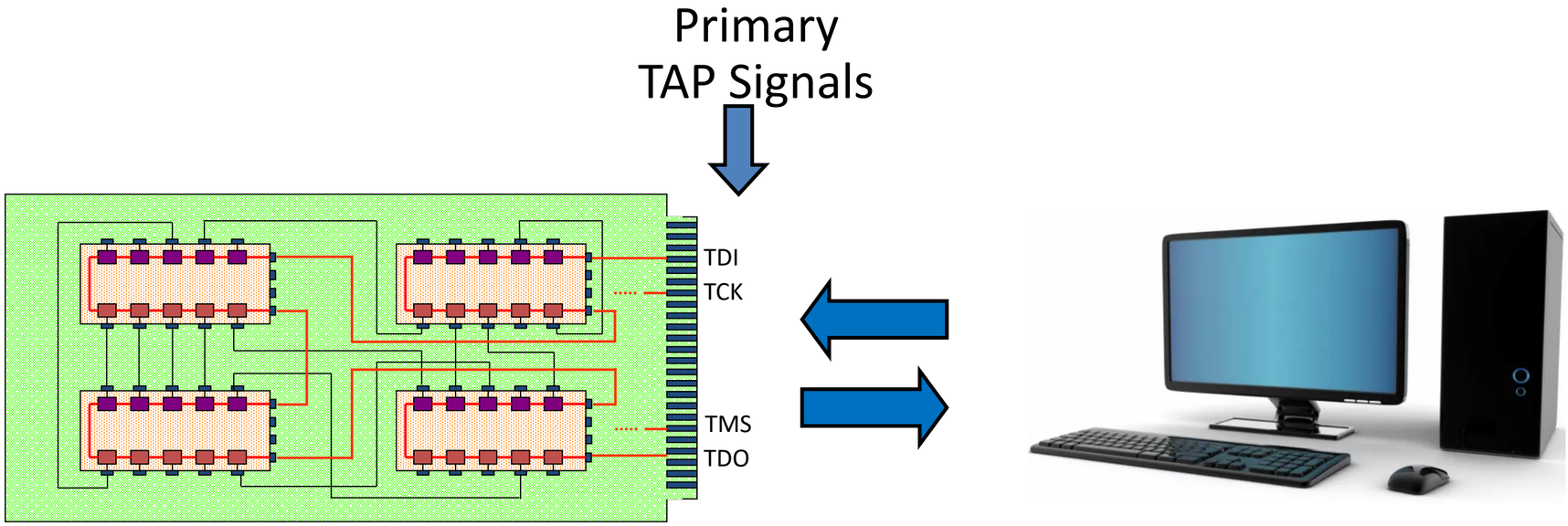
Complex Scan Path Design



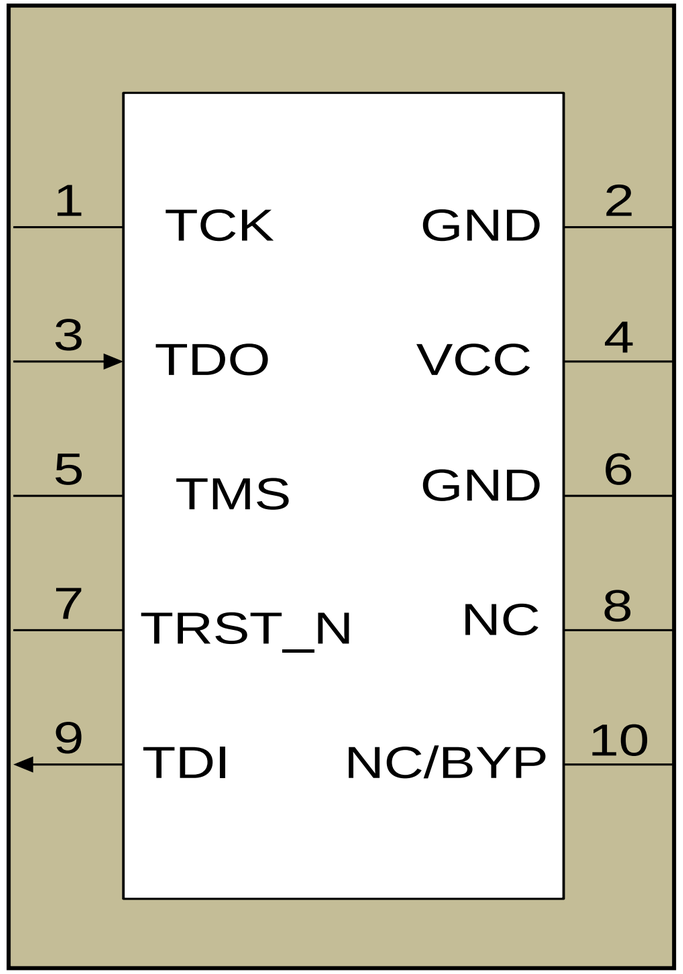
Access to TAP Signals



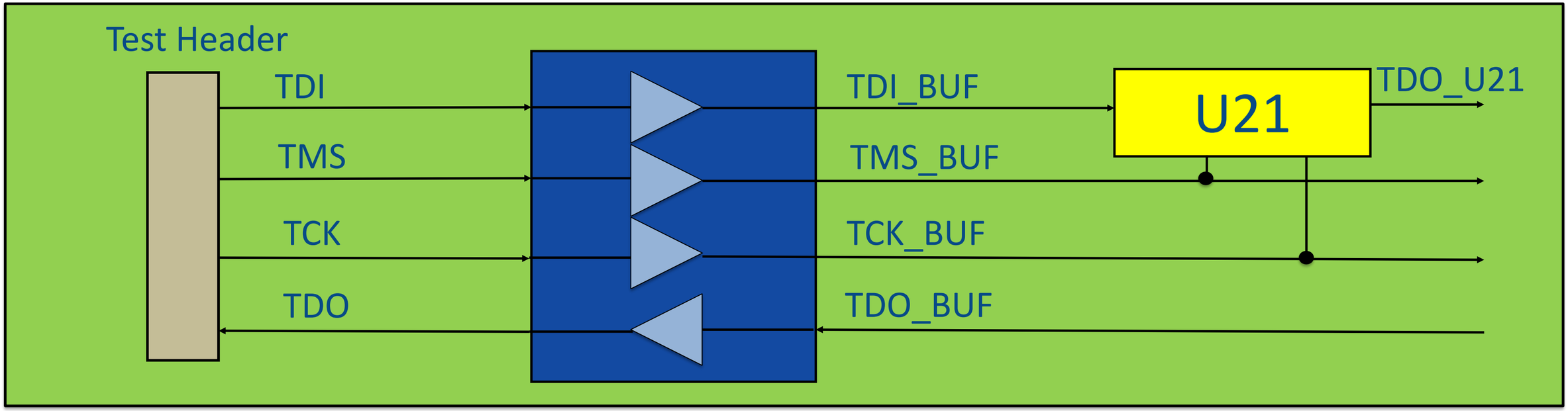
- Allow direct primary access from the tester to all board top-level TAP signals: TDI, TDO, TMS, TCK and TRST*

Access to TAP Signals

- Use a common test header
  - minimum 10-pin header
- Use vendor or boundary scan tool provider footprint
- Key the header
  - Cable can only be plugged in one way
  - Prevents damage to test equipment



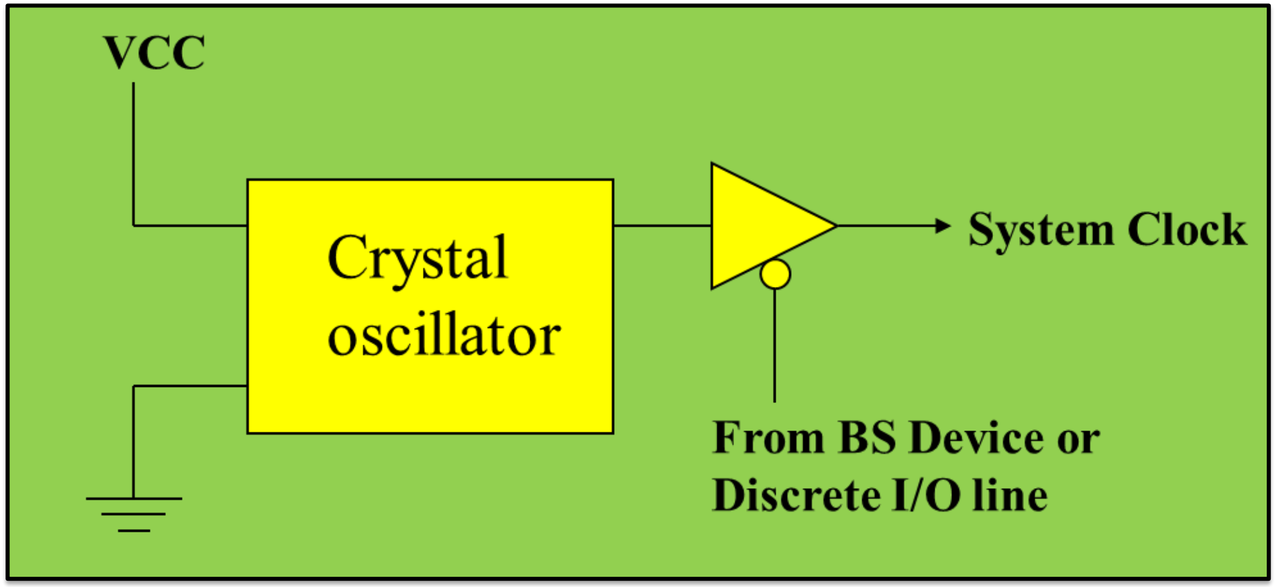
Buffering TAP Signals



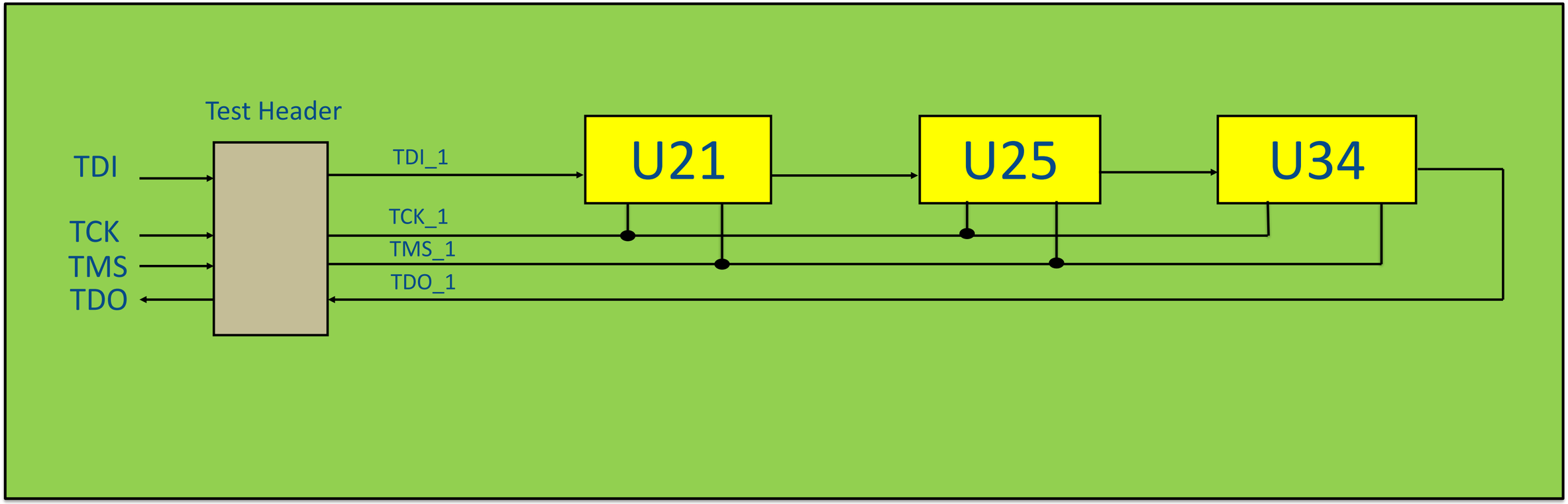
- At the primary TAP connector use buffer devices to reduce noise, minimize skew and impedance match
- Use FPGAs as buffers if existing devices are too slow or supply incorrect voltage

Direct Control of System Clock

- Allow boundary scan or direct tester control of the system clock
  - Elimination of noise
  - Ensure UUT is non-functional so boundary scan operations can take place safely



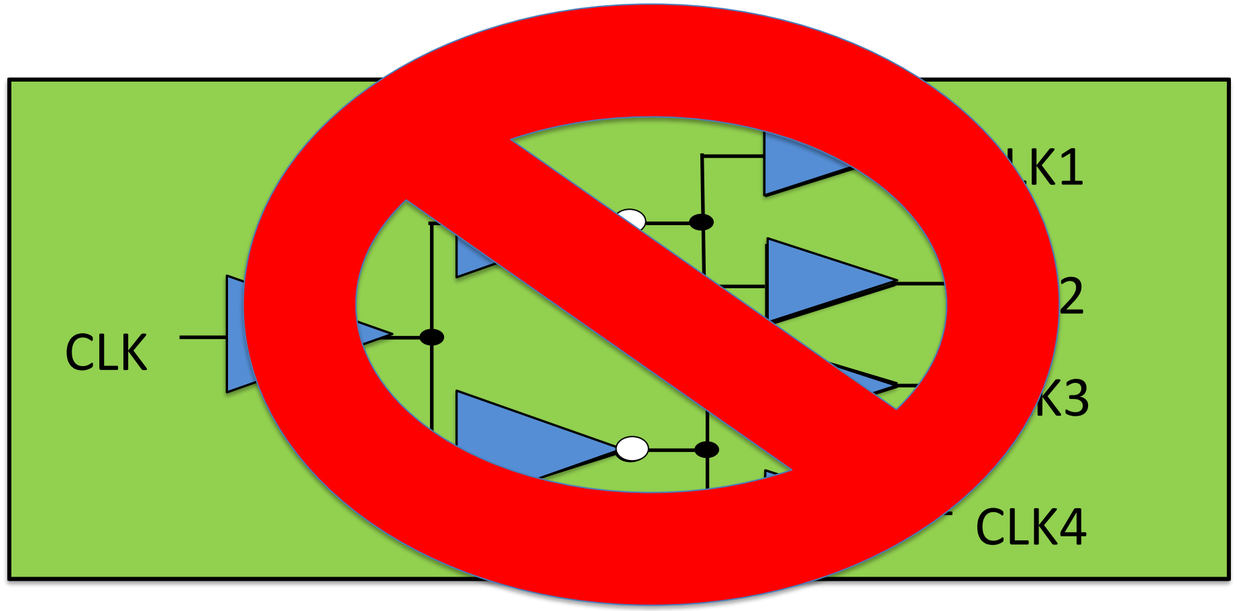
TCK and TMS Distribution



- Design TCK and TMS board distribution with care
- Specify TCK as critical signal during layout
- Design TMS to have no skew relative to TCK

TCK and TMS Distribution

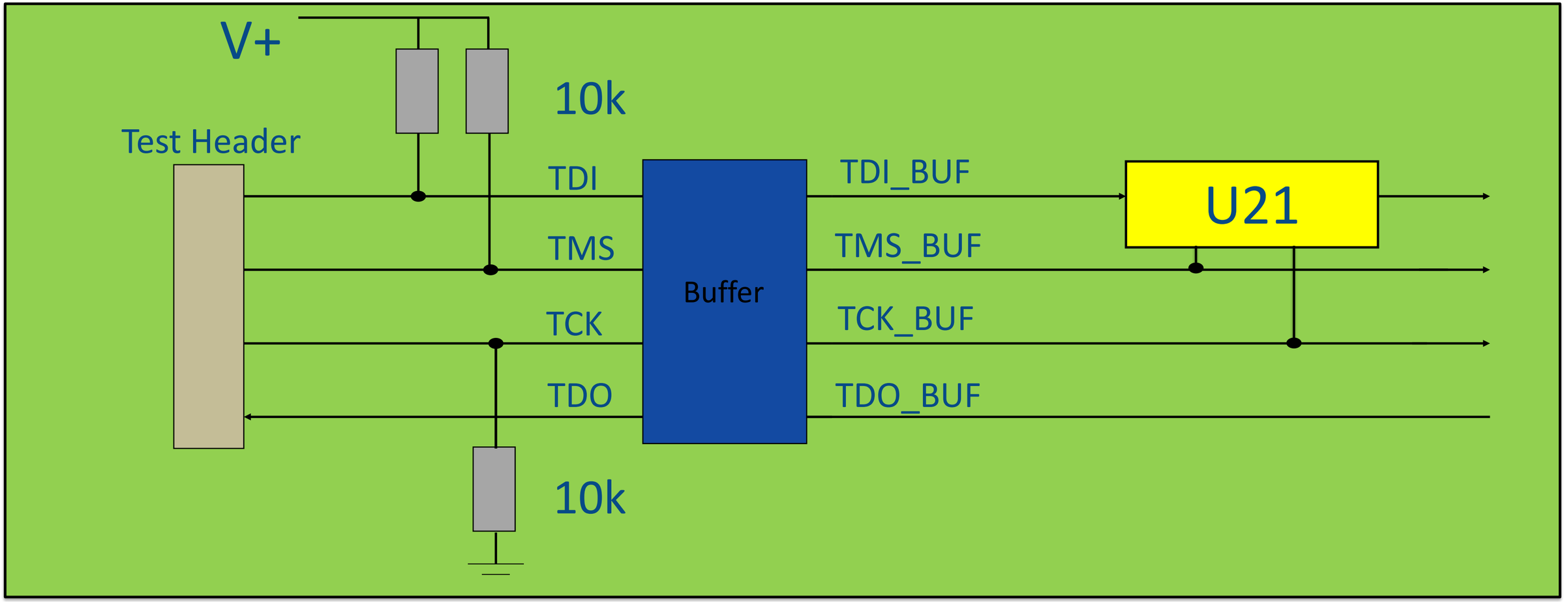
- Be careful with the type of buffer used for TCK and TMS distribution



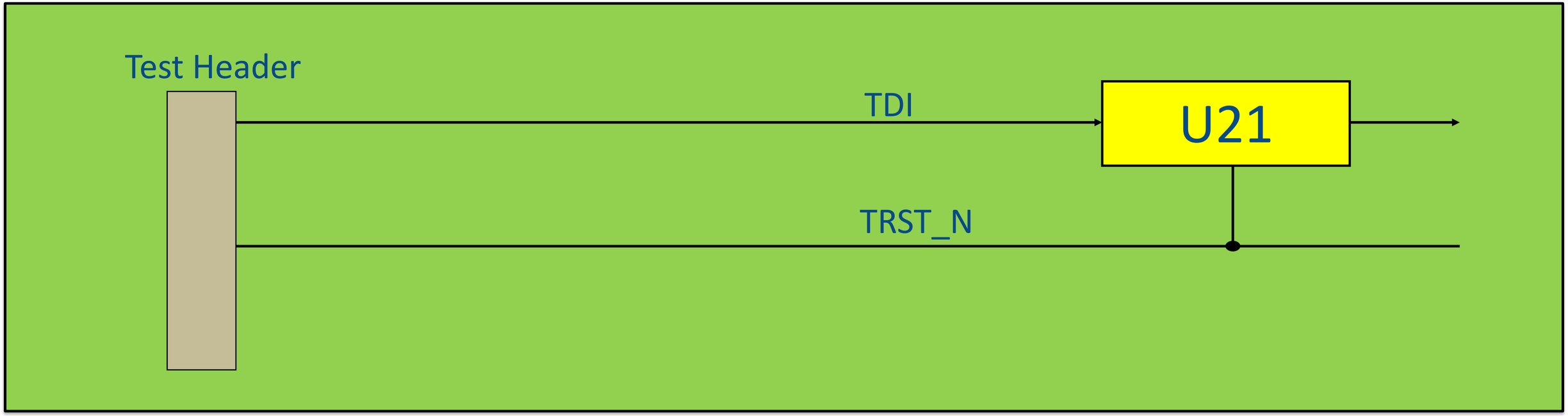
- Inverting clock buffers are used to help maintain a 50-50 duty cycle on a system clock
- Do not use inverting buffers for TCK and/or TMS - logical inversion is not allowed

Pull-up / Pull-down on TAP Signals

- TAP signals should be pulled to safe states



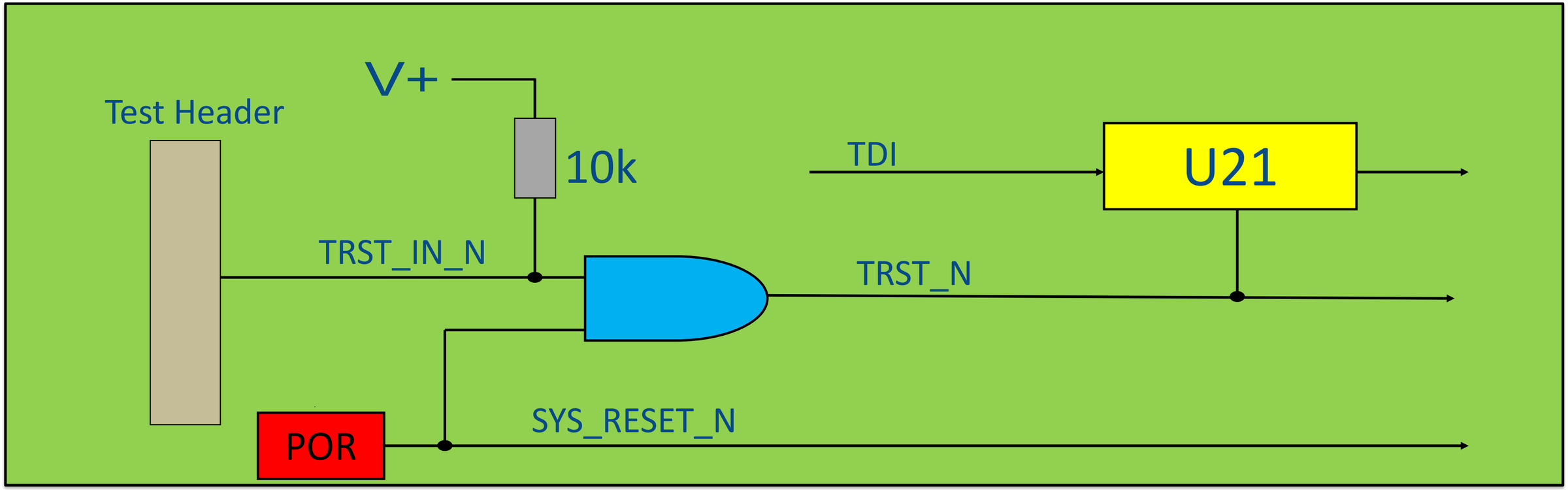
Board TRST



- 1149.1 requires TRST internal to go high (logic-1) when left open-circuit
- This is accomplished with a pull-up resistor internal to the device
- If the board TRST_N signal is floating during normal operation and there is no internal power-up reset in the boundary scan device (not mandated when the device has a TRST), the TAP controller can power up in any state

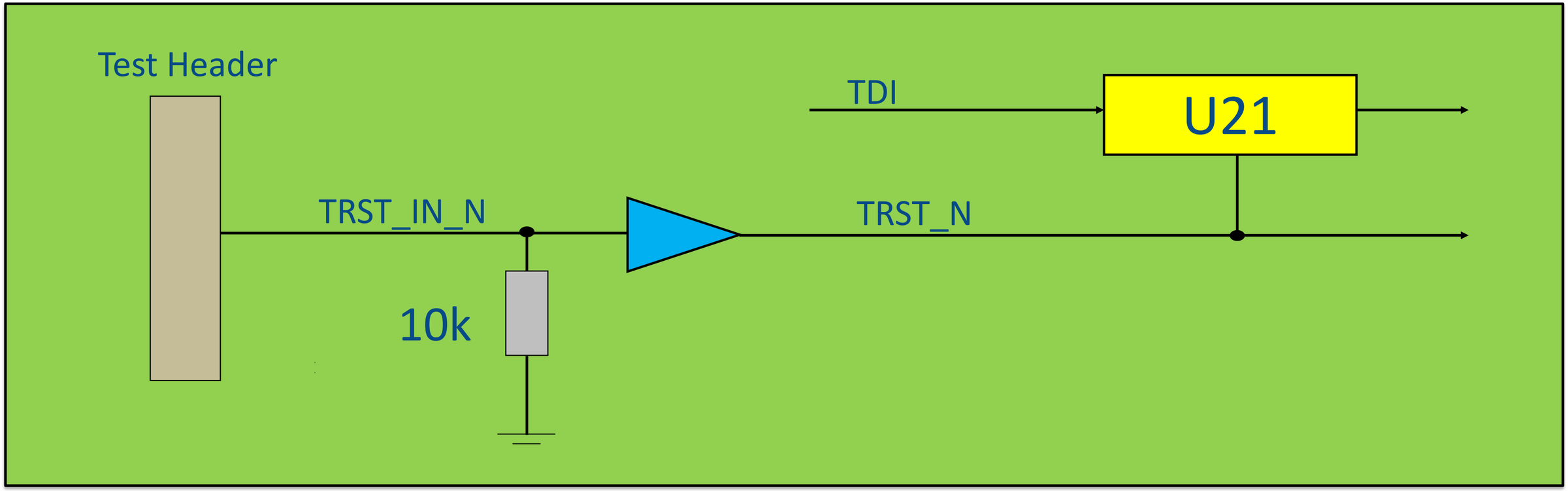
Board TRST – Power-on Reset Solution #1

- Add a Power-Up Reset circuitry to reset TRST

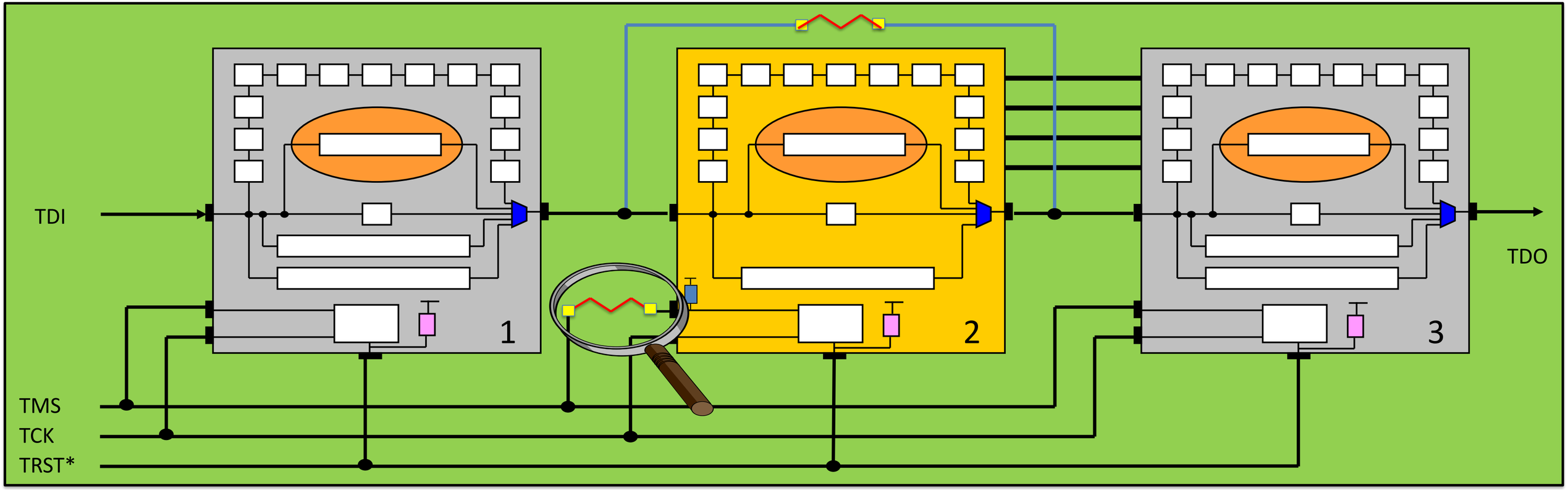


Board TRST – Power-on Reset Solution #2

- Place pull-down resistor before buffer

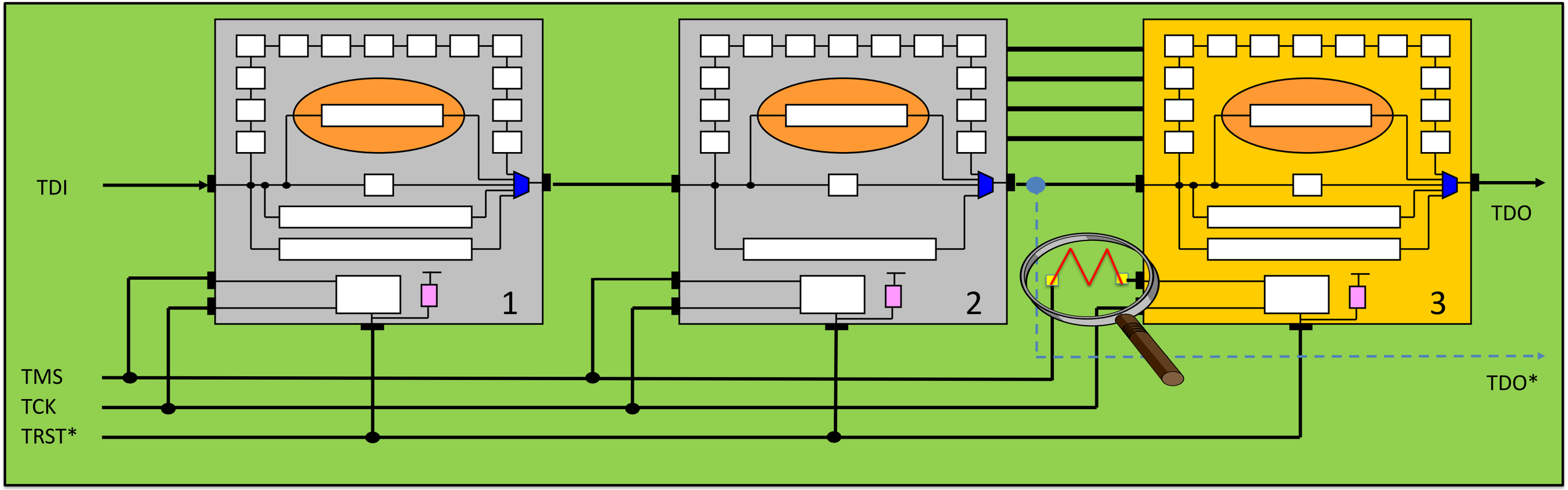


Handling Non-Compliant Devices



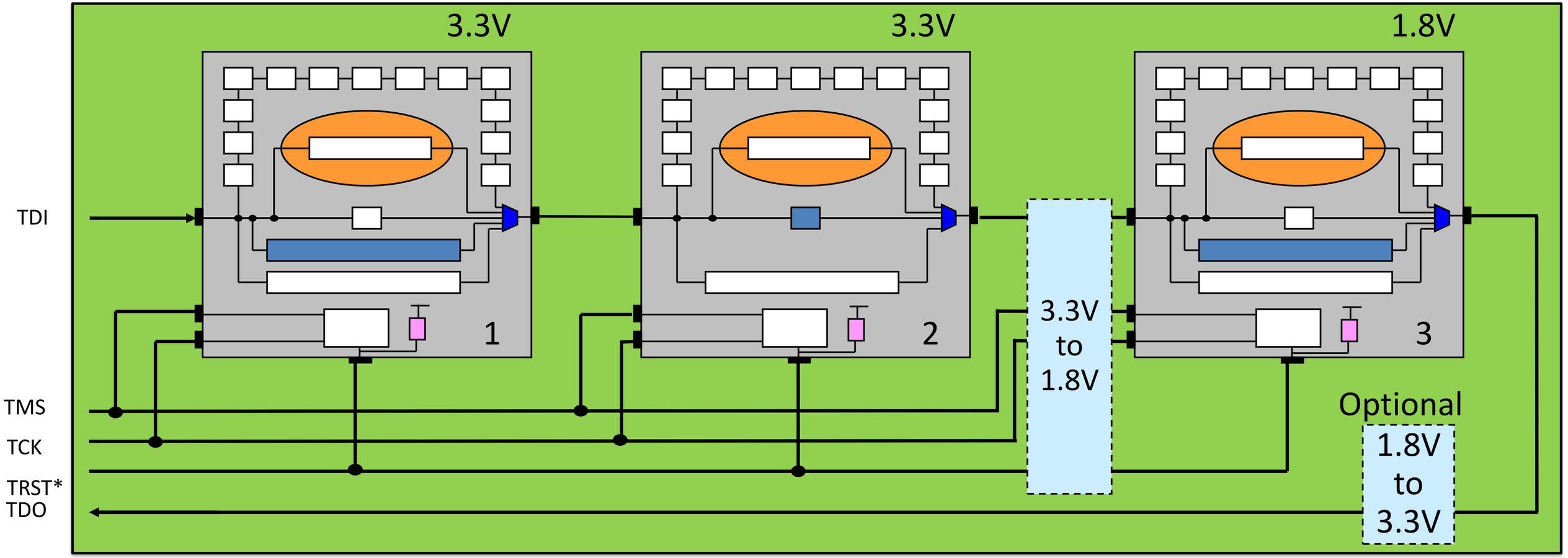
- Place a zero-ohm jumper between TDI and TDO of suspected non-compliant or non-operational boundary scan devices in order to bypass them if necessary
- Make sure TMS is disconnected to ensure that the non-compliant device is held in its Test-Logic-Reset state (TMS = 1 when open circuit)

Handling Non-Compliant Devices



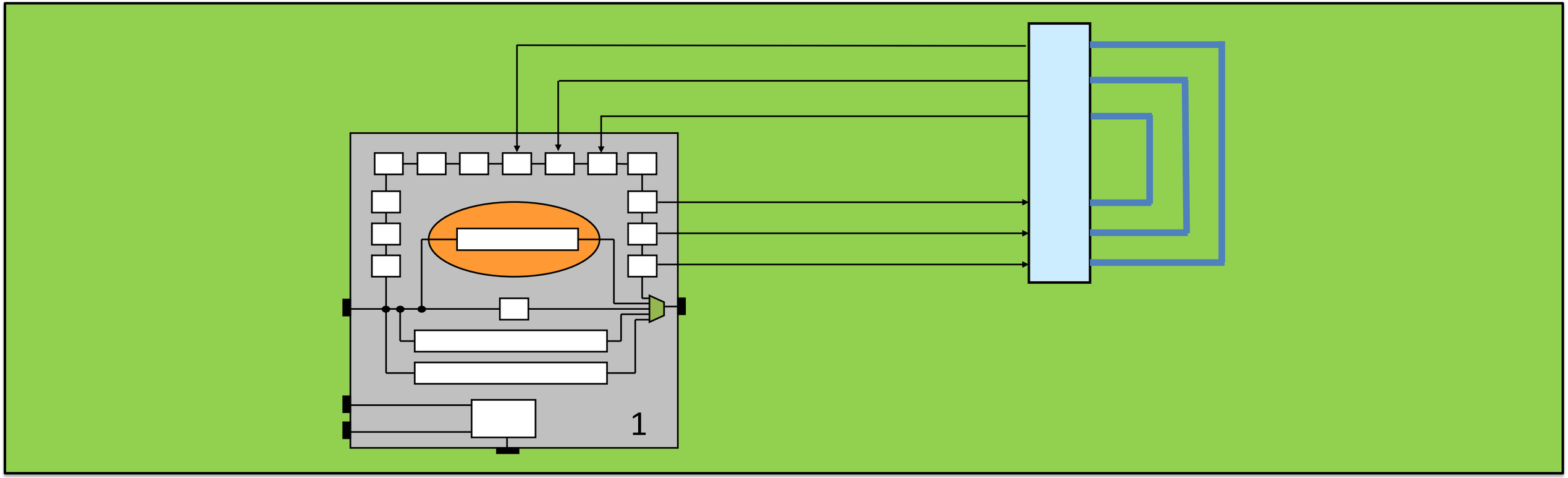
- Place a potentially troublesome device at the end of the chain and provide an alternate TDO exit off the board

Handling Different Voltage Levels



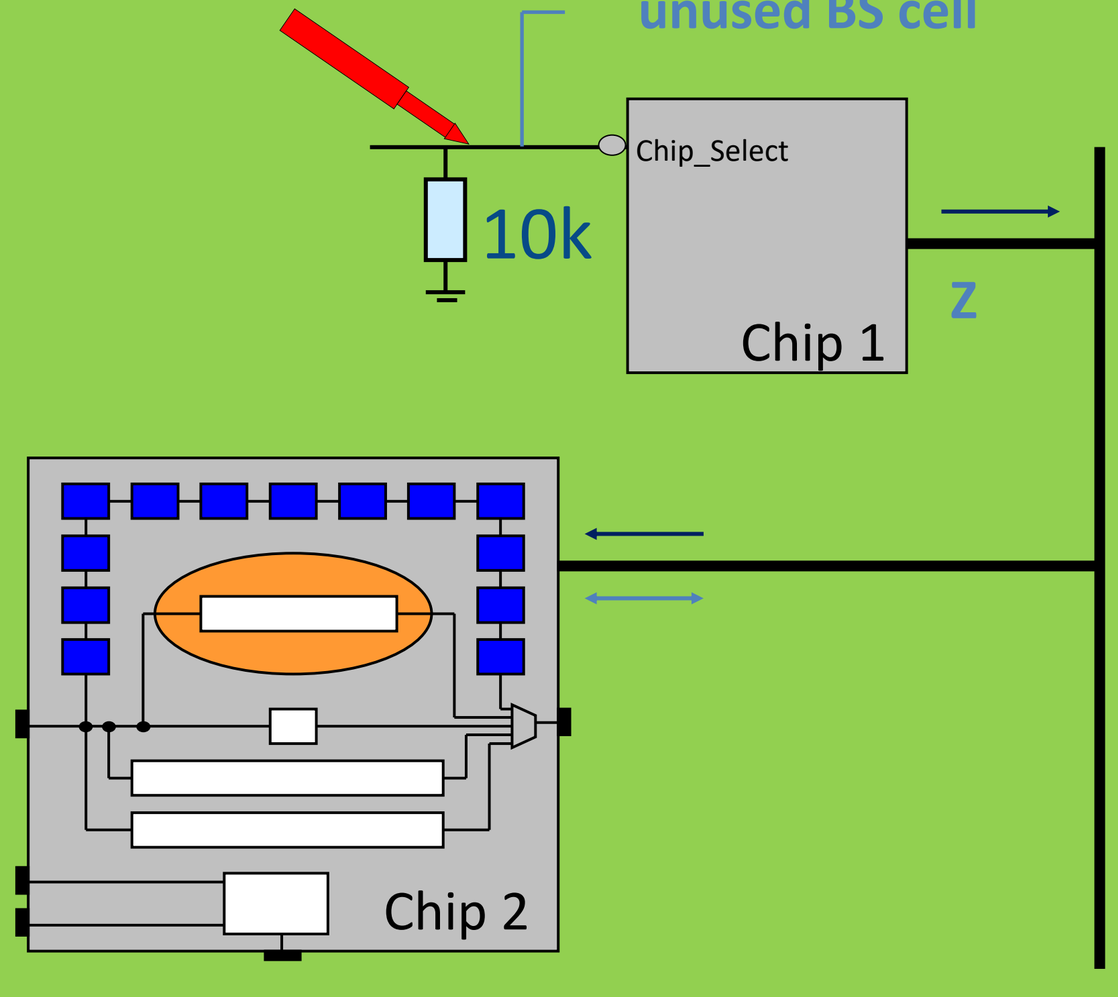
- Ideally, group devices with the same voltage levels into the same scan chain
- Or provide voltage converters between different parts of the scan chain

Connector Test



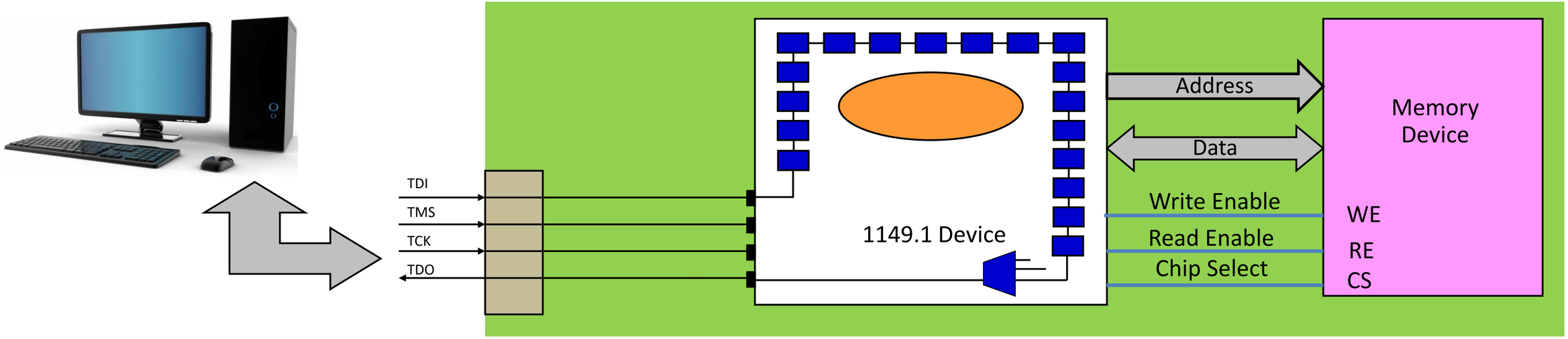
- Nets to a board connector can be tested for shorts
- Use a connector loopback fixture or an external board to add opens testing for the connector pins and boundary scan pins

Allow Defeatable Tied-off Control Pins



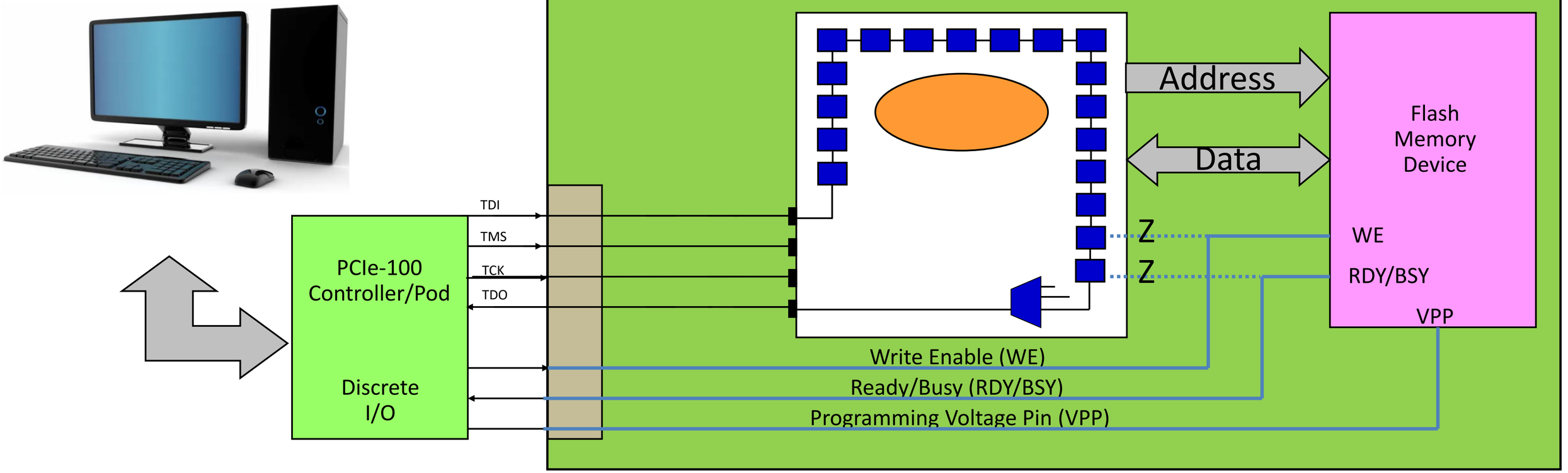
- **Functional mode:**
  - Chip 1: outputs active
  - Chip 2: bidirectional pins are always inputs
- **Test Mode:**
  - Chip 1: outputs are HighZ
  - Chip 2: bidirectional pins can be either outputs or inputs

Testing Memory Devices

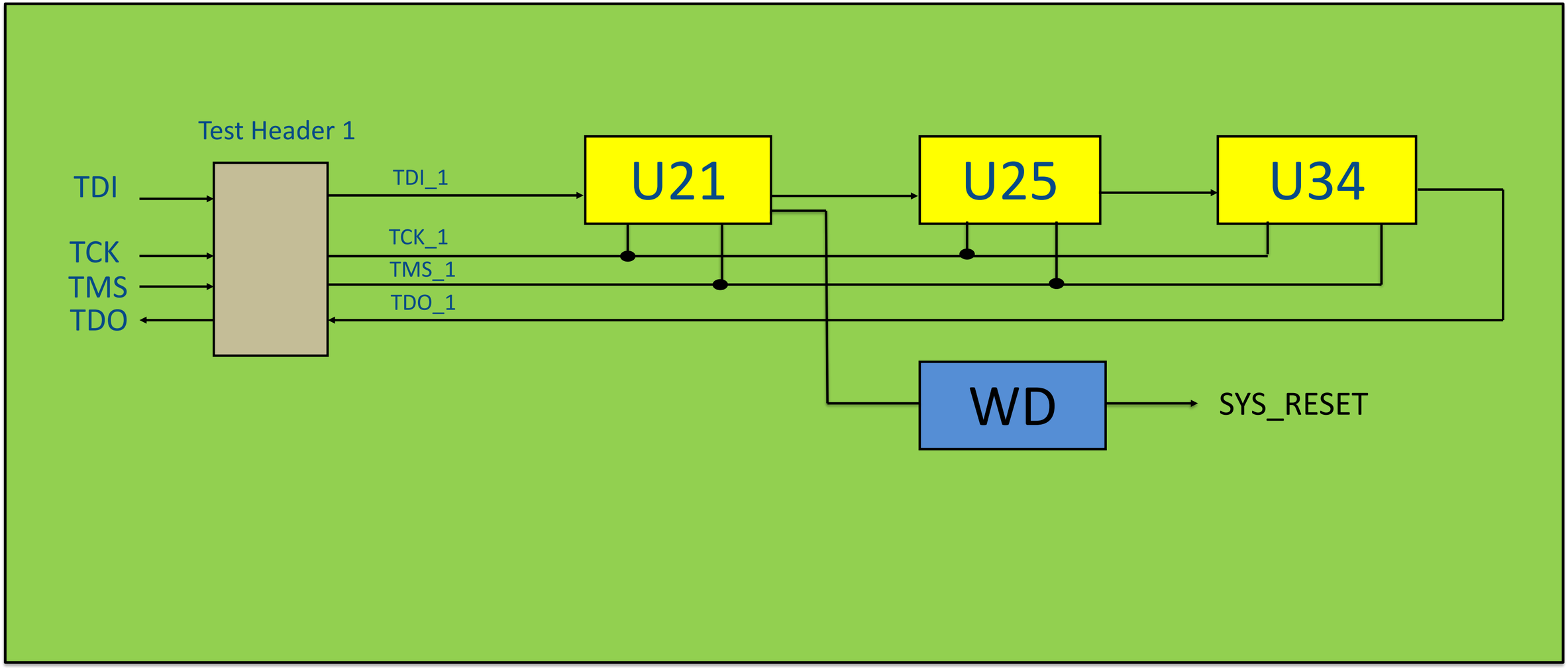


- Allow presence, orientation and bonding tests to be applied to the memory devices from the boundary-scan interface. Requires:
  - Boundary scan access to address and data busses
  - Direct or boundary scan access to the memory control signals
  - Make sure there is no risk of contention during memory test, check for cluster models of any non boundary scan devices on the data bus
  - Need model of memory device that describes at minimum the pins of the memory device that require boundary scan access

Programming Flash Devices



Bypass Watchdog Circuits



Summary of Board DFT based on Boundary Scan

- Boundary scan device selection
- Focus on the scan chain design
- Access to the TAP
- Buffering the TAP
- Direct control of the system clock
- TCK and TMS distribution
- Pull-up / pull-down on TAP signals
- Board TRST
- Handle troublesome devices / different voltages
- Connector test
- Allow defeatable tied-off pins / unused boundary scan pins
- Testing memory devices / flash programming
- Bypass watchdog circuits

For More Information

- Use ASSET's Online BSDL Validation site for syntax and semantics error checking, http://bsdl.asset-intertech.com/
- Go to our blog, Everything You Need to Know About ScanWorks Interconnect (Part 1), https://www.asset-intertech.com/resources/blog/2022/09/everything-you-need-to-know-about-scanworks-interconnect-part-1/
- Download our eBook, Testing DDR Memory with Boundary Scan/JTAG (Third Edition), https://www.asset-intertech.com/resources/eresources/ddr-memory-test-modern-tools-for-validation-test-and-debug/
- View our webinar, Squeezing Out More Test Coverage: Bridging the Gap Between Boundary Scan and Functional Test, https://www.asset-intertech.com/resources/videos/bridging-the-gap-between-boundary-scan-and-functional-test/

Questions and Contact Information

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