ScanWorks Test Technologies

Larry Osborn

Project Manager for:

ScanWorks FPGA-Flash Programming

ScanWorks Processor-based Fast Programming

ScanWorks IJTAG

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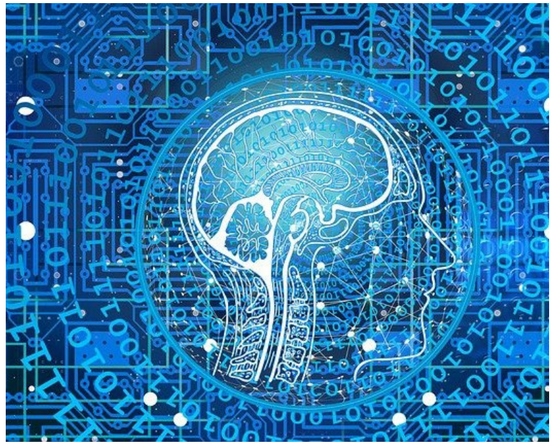
Agenda

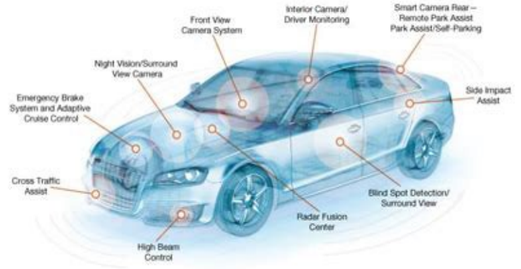
- Technology Trends
  - Device Complexity
    - Stacked Die
    - Chiplet
    - Tiles
  - Impact of Component Shortages
    - Replacement vs re-design
    - Dealing with Counterfeit Components
- ScanWorks Addressing the Trends
  - Technology Trends
    - Stacked Die
    - Chiplet
    - Tiles
- ScanWorks Platform
  - BST
    - Interconnect Test
    - Component Test
    - DDR4 Test
- ScanWorks Platform
  - Functional Test
    - QSPI
    - SDMMC
- Demo
  - UltraZed
    - Memory Test
      - Structural Test - BST
      - Functional Test -PFx
- Questions

Technology Trends

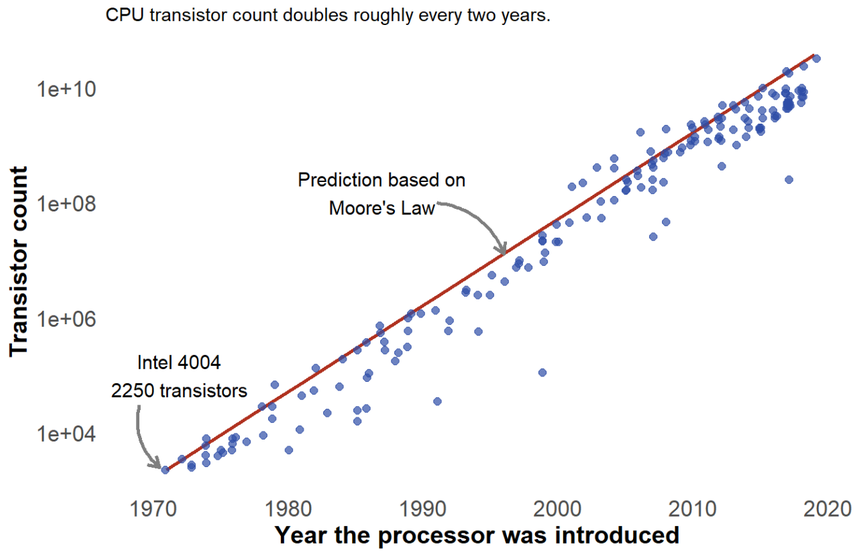
- Market Trends
  - Design starts
    - Artificial Intelligence
    - 5G
    - Defense - towards FPGAs for Cyber Security issues
    - Automated Driving Solutions (ADS)
    - Hyperscale Data Centers (HDC)

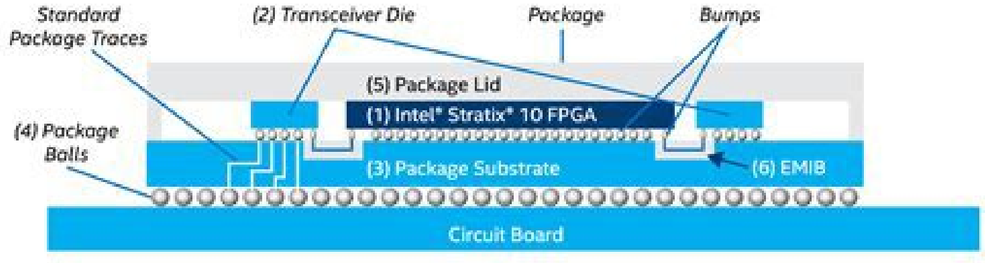


Advanced Driver Assistance System Applications



Device Complexity



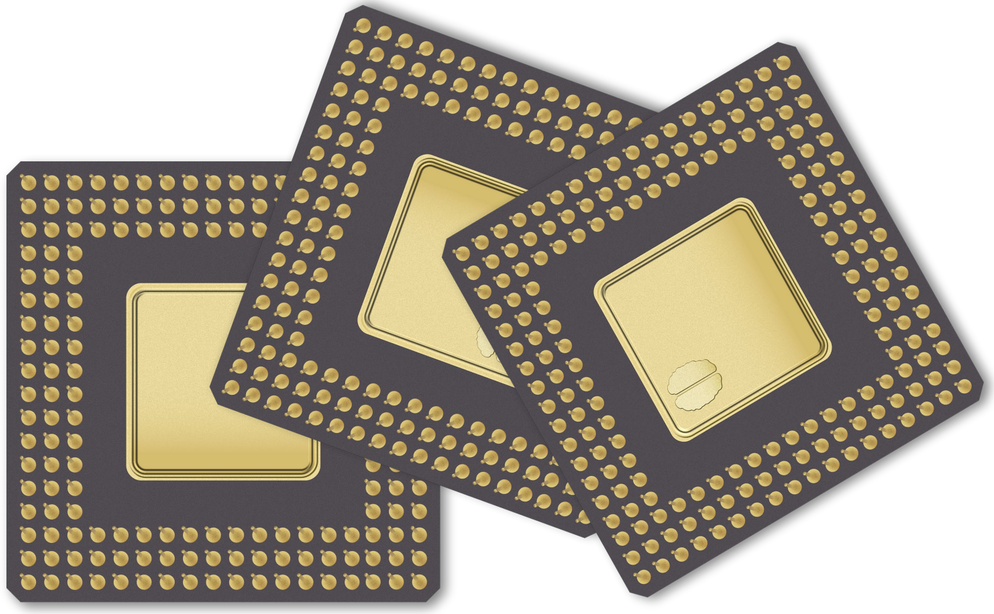


- Stacked Die Chiplets/Tiles
- New IP
- New IEEE standards

Component Shortage Impacts

- Redesign Decisions
  - Is the component available?
  - What is the current cost?
- IEEE Spectrum articles on Chip Shortages
  - How and When the Chip Shortage Will End
  - 5 Ways the Chip Shortage is Rewiring Tech

Component Shortage – Dynamic Test Tools a Must



- Robust library selection
  - Memories
  - FPGA
  - Logic component
- Test development responsiveness
  - Easy test modifications
- Smart Tests
  - Device ID driven test flow

Counterfeit Components

- Counterfeiters are getting creative
  - How are you managing the risk?

- IEEE article on counterfeit components

ScanWorks®

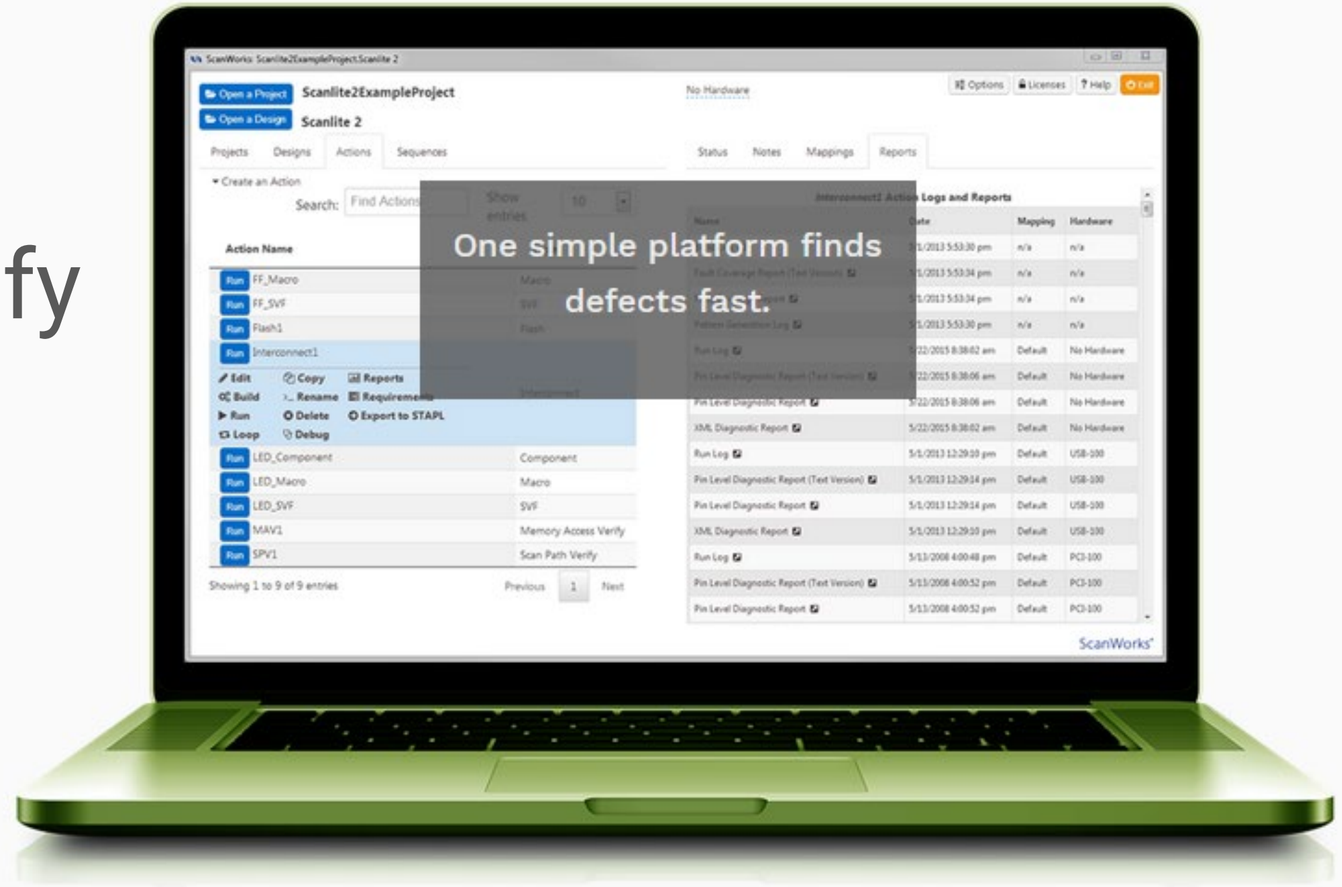
Platform for Embedded Instruments

ScanWorks Platform

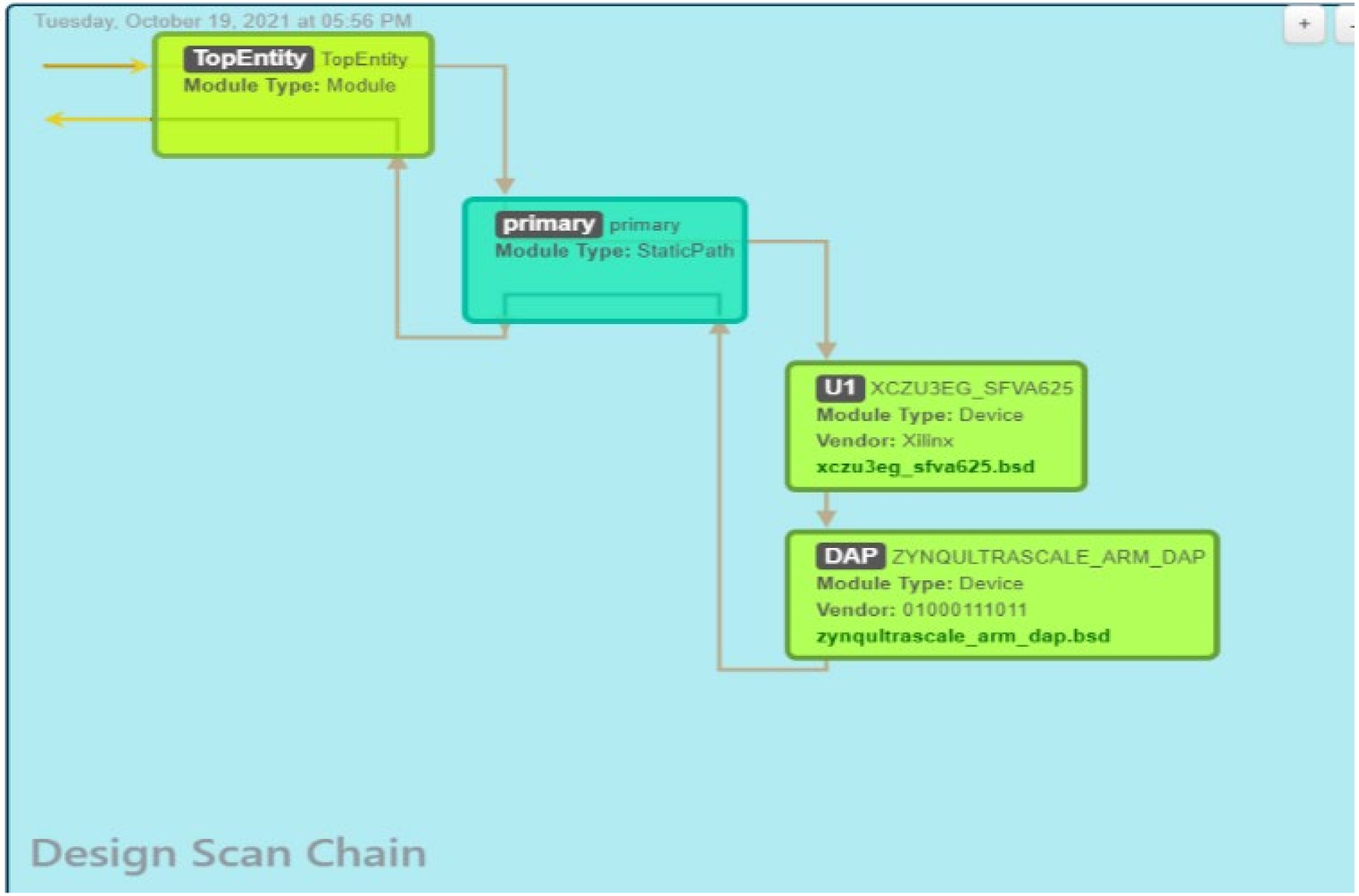
- ScanWorks Products
  - Boundary-Scan Test
  - Board Functional Test
    - Processor-based (Xilinx and NXP SoCs)
  - Fast Programming
    - FPGA-based (Intel (Altera), AMD-Xilinx, Microchip (Microsemi))
    - Processor-based (Xilinx and NXP SoCs)
  - Embedded Diagnostics
    - Custom fielded diagnostics via Baseboard Management Controller
  - IJTAG Test

ScanWorks Platform

- BST
  - Interconnect
  - Memory Access Verify
  - Component Action

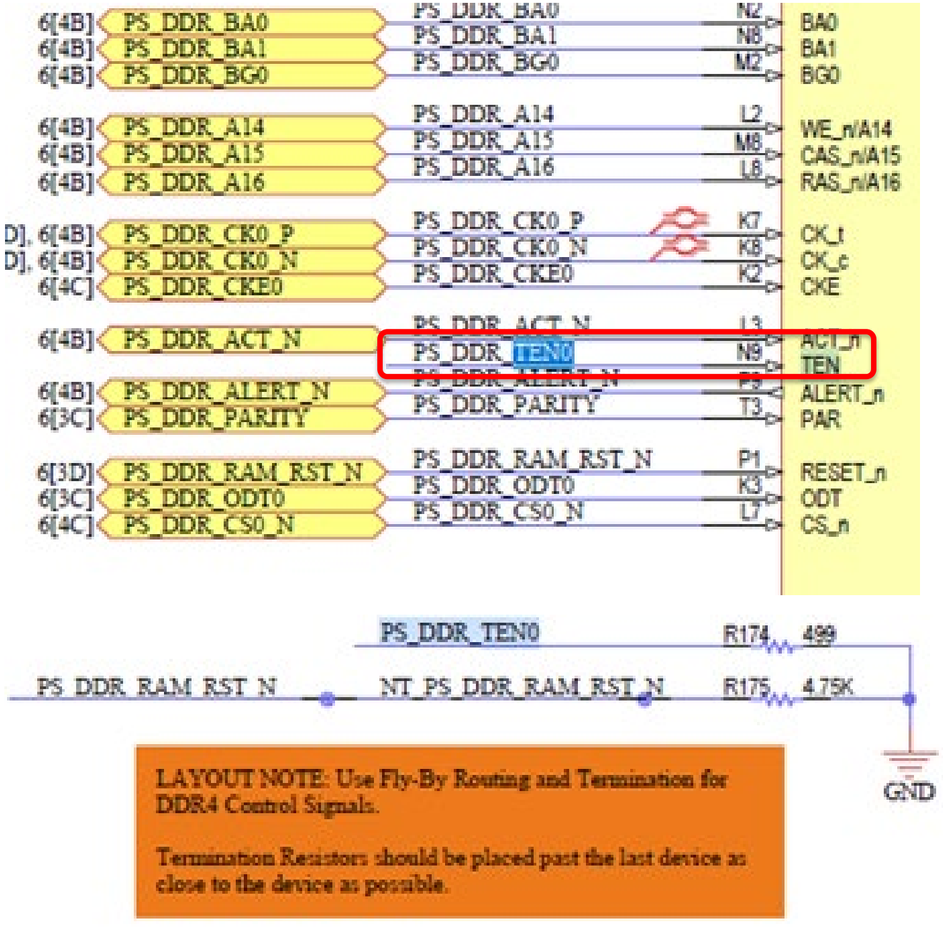


ScanWorks Test Development



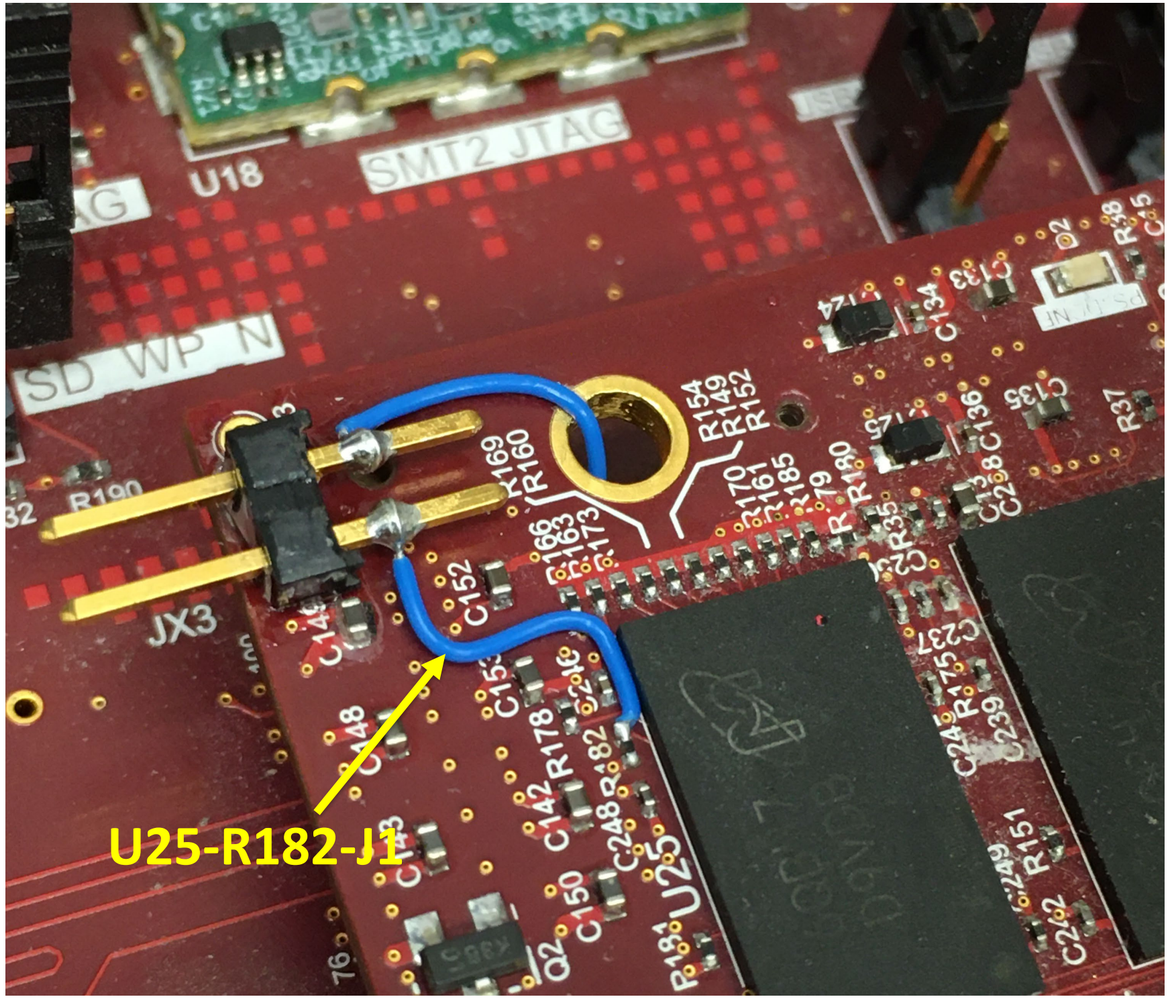
- Define the device(s) in the JTAG chain
- Add the actions
  - Enable the Arm_DAP via SVF
  - Interconnect Test
  - MAV Test

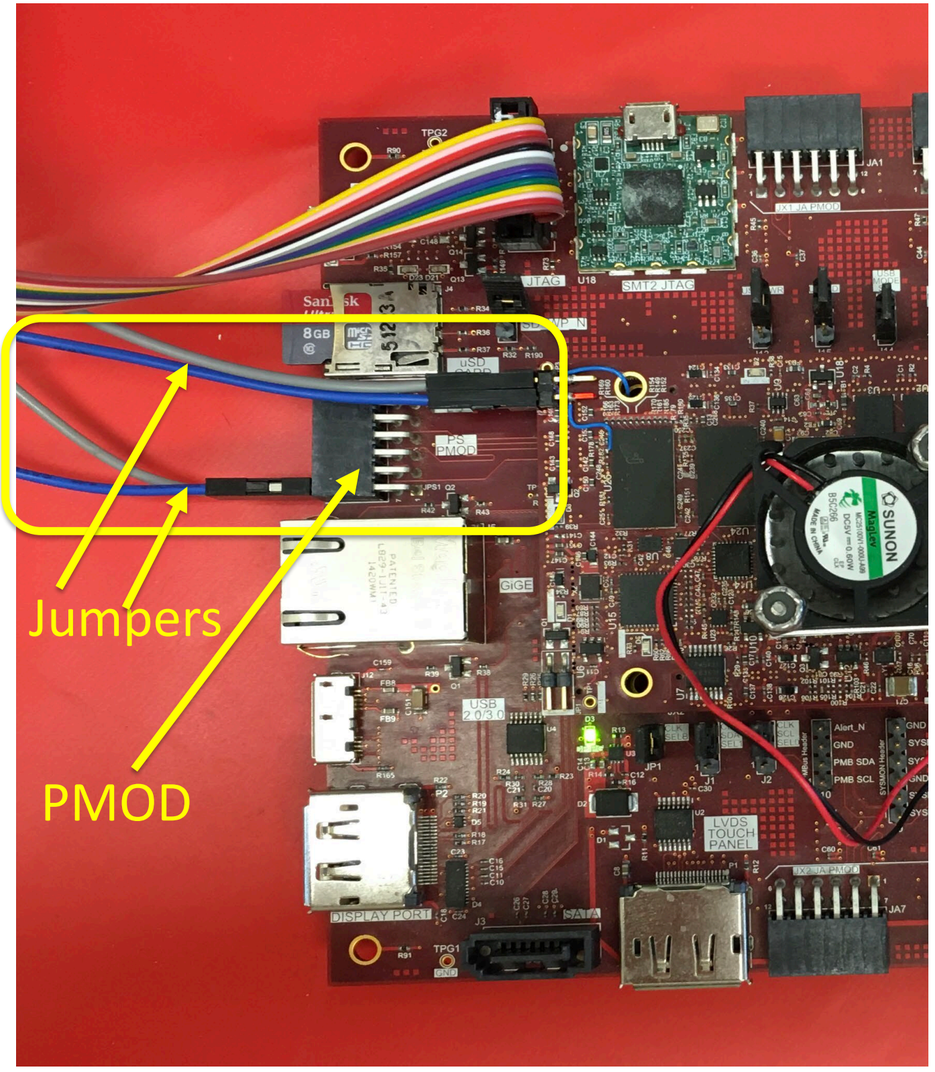
ScanWorks Test Development Continued



- Component Action
  - Provide control access to Test Enable (TEN) Connect PS_DDR_TEN0 to memory devices

Component Action

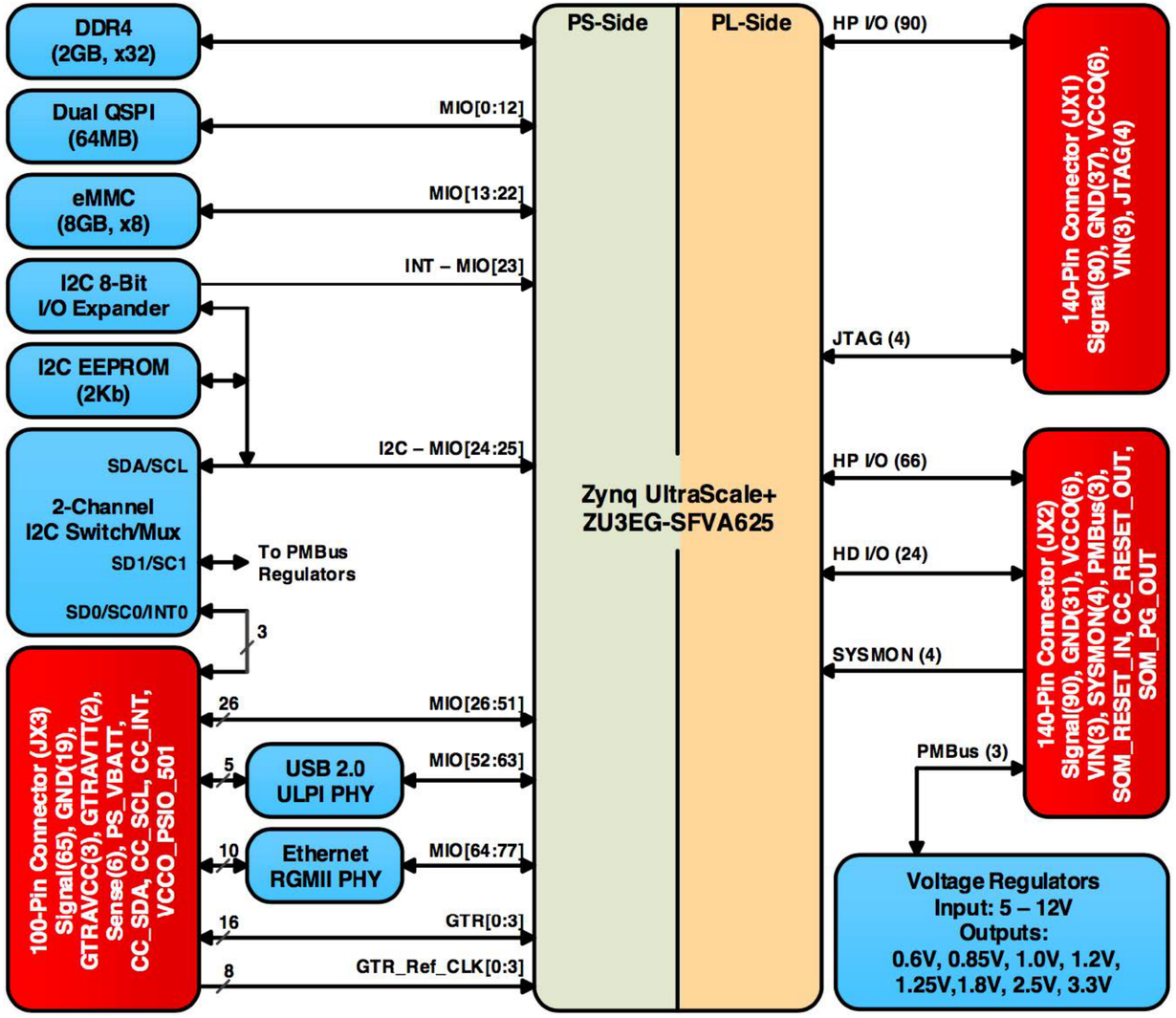




SourcePoint®
Platform for Software Debug and Trace

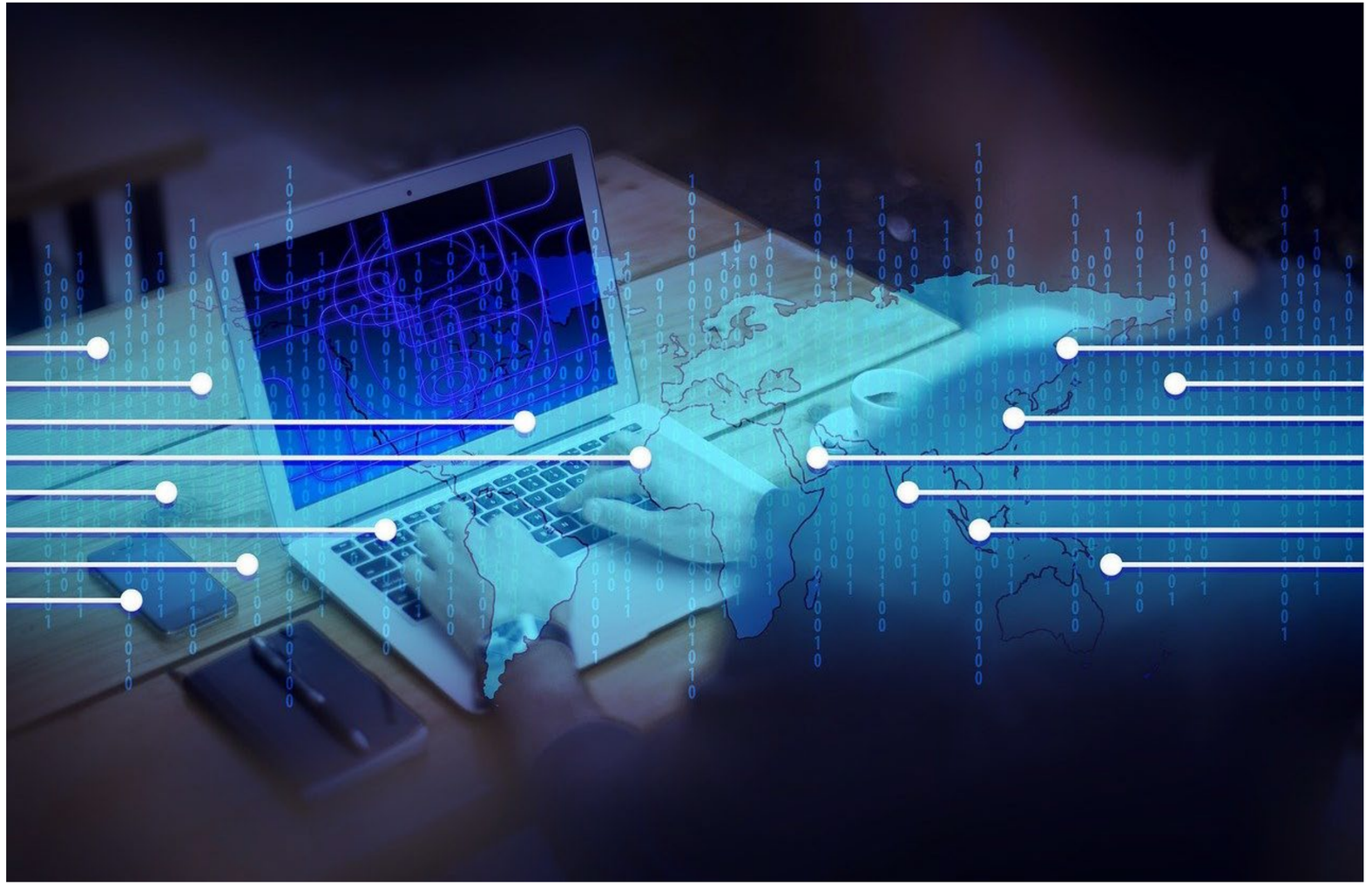
ScanWorks®
Platform for Embedded Instruments

Xilinx Zynq UltraScale+ MPSoC



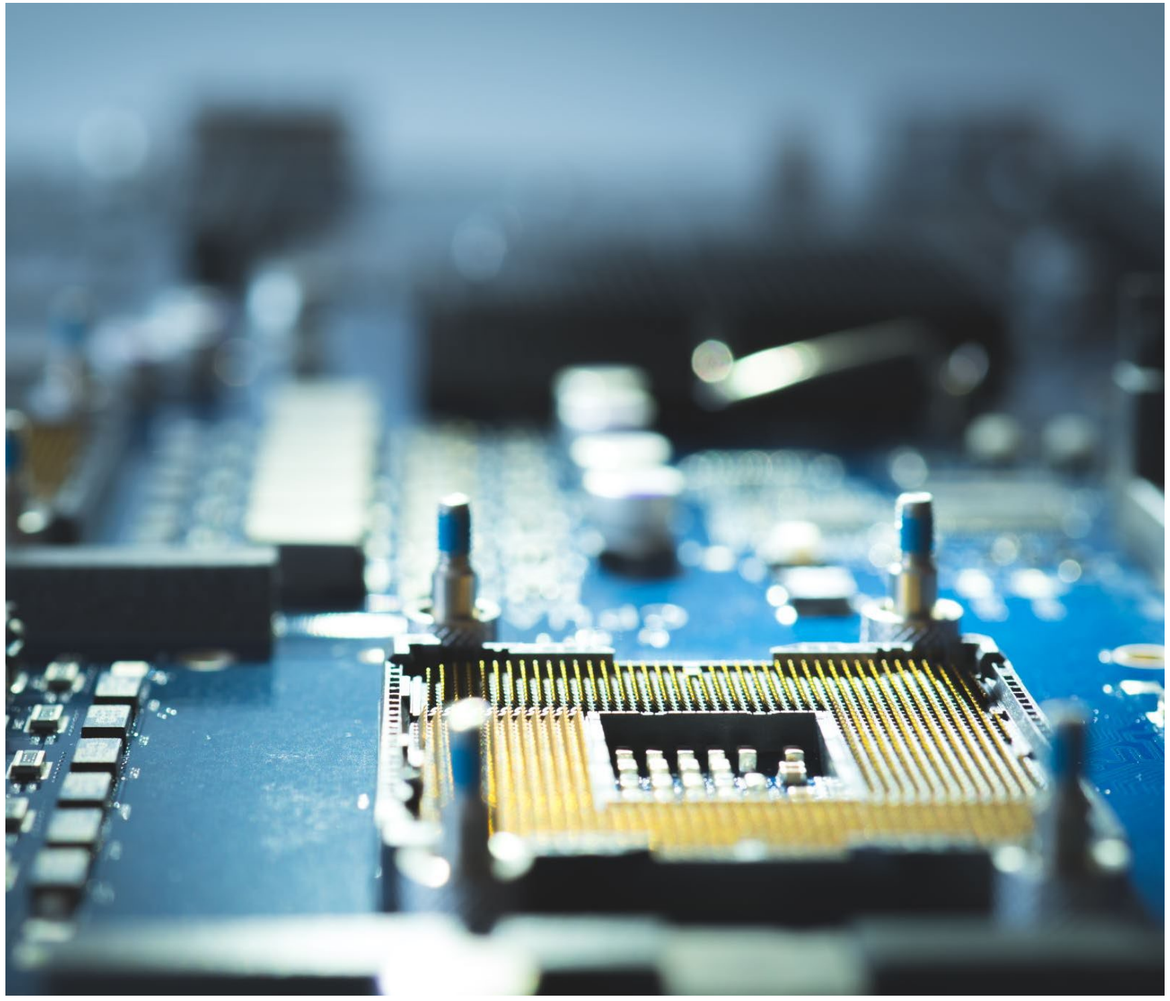
- PS connections
  - QSPI
  - DDR4
  - eMMC
  - I2C
  - Ethernet PHY

ScanWorks Platform



- Functional Test
  - DDR4
  - Device Presence
  - Ethernet PHY
- Programming
  - NAND/NOR
  - SPI/QSPI
  - SDMMC/eMMC

Programming Methods Consideration

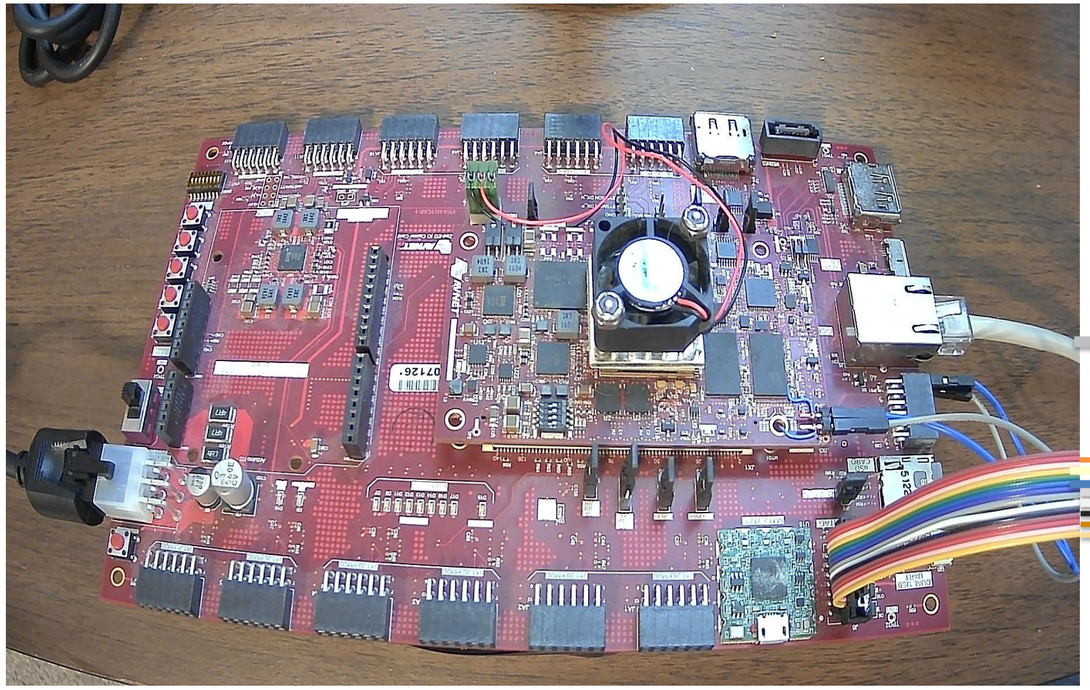


- BST
  - SoC boundary scan
    - NAND, NOR, SPI, QSPI, eMMC
  - Connected to JTAG enable device
- SPI DIO
  - GPIO control
- SoC – Processor System or FPGA Fabric
  - If Processor – PFP
    - NAND, NOR, SPI, QSPI, SD/MMC, eMMC
    - Ethernet data download
  - If Programmable Logic – FFP
- FPGA Standalone
  - FFP
- SPI Direct – RIC-1400
  - Flash Header access

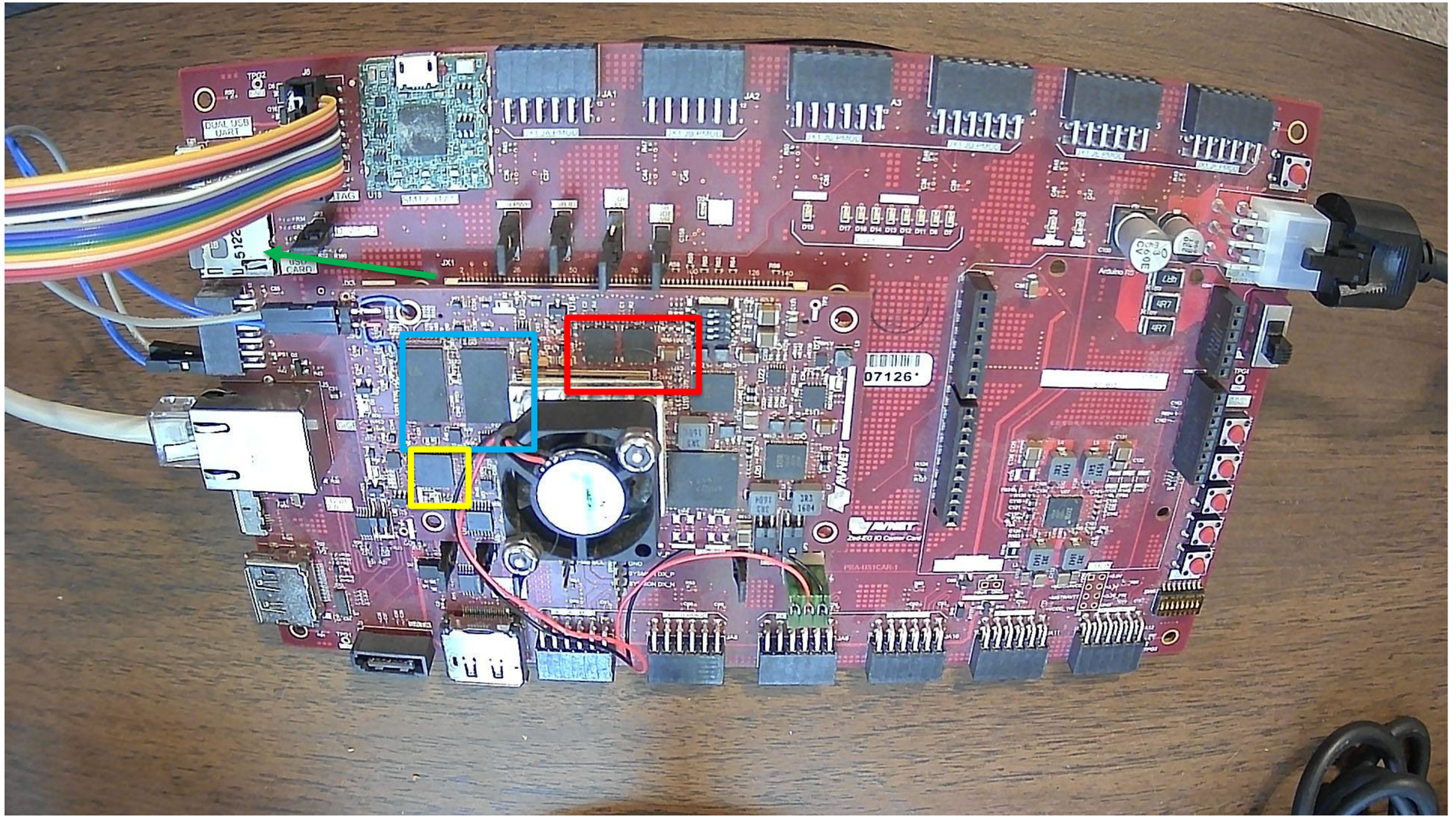
ScanWorks Programming Speed Technology Comparison

Access Method	TCK	SoC Clock	FPGA Clock	Programming File Size	Erase/Program/ Verify Time	Improvement	Constraints
Boundary-Scan Chain	12 MHz	NA	NA	1 MB	35 minutes (2100 seconds)	-	UUT JTAG Clock Rate /BST Register
Short Chain	12 MHz	NA		1 MB	4 minutes (240 seconds)	~9x	Supported FPGA Families
SPI DIO	45 MHz	NA	NA	1 MB	2 minutes 5 seconds	17x	SPI Header
PFx Programming	30Mhz	800 MHz	NA	1MB	11 seconds	190x	UUT JTAG Clock Rate
PFx Programming Via Ethernet	30Mz	800 MHz	NA	1 MB	2.4 seconds	78x	Supported SoC Only
FPGA-based SPI Flash Programming	30 MHZ	100 MHz	100 MHz	1 MB	2.3 seconds	91x	Supported FPGA Families
SPI Direct	10 MHz	100 MHz	100 MHz	1 MB	2.3 seconds	91x	RIC-1400 and SPI Header

ScanWorks Demo Configuration



Avnet UltraZed



QSPI

DDR4

eNet PHY

SD Card

ScanWorks Demo

Recap

ScanWorks Addressing Technology Trends

- We demonstrated how ScanWorks can address both structural and functional testing during this era of chip shortages and redesign impacts that occur when moving from one silicon provider to another. The demonstration showed the various ways of attacking various problems that can be manifested in device complexity as you move to newer more powerful and sophisticated silicon.

Conclusion

- You or your competitor will be the leader by the tool choices made during these time of component shortages.

Resources

- BST
  - https://www.asset-intertech.com/products/scanworks/scanworks-boundary-scan-test/
- PFT
  - https://www.asset-intertech.com/products/scanworks/scanworks-board-functional-test-device-programming/
- FFP
  - https://www.asset-intertech.com/products/scanworks/scanworks-fpga-based-fast-programming/
- PFP
  - https://www.asset-intertech.com/products/scanworks/scanworks-fast-flash-programming/
- eResouces
  - eBooks
  - Videos

Questions and Contact Informaion

Contact Information:

Larry Osborn

7161 Bishop Rd. Ste. 250

Plano, TX 75024

Larry.Osborn@asset-intertech.com

www.asset-intertech.com

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