Real Insight from Code to Silicon

ScanWorks Test Technologies

Larry Osborn

Project Manager for:
ScanWorks FPGA-Flash Programming
ScanWorks Processor-based Fast Programming
ScanWorks JTAG
August 2022
Agenda

- Technology Trends
  - Device Complexity
    - Stacked Die
    - Chiplet
    - Tiles
  - Impact of Component Shortages
    - Replacement vs re-design
    - Dealing with Counterfeit Components

- ScanWorks Addressing the Trends
  - Technology Trends
    - Stacked Die
    - Chiplet
    - Tiles

- ScanWorks Platform
  - BST
    - Interconnect Test
    - Component Test
    - DDR4 Test

- ScanWorks Platform
  - Functional Test
    - QSPI
    - SDMMC

- Demo
  - UltraZed
    - Memory Test
      - Structural Test - BST
      - Functional Test - PFx

- Questions
Technology Trends

- Market Trends
  - Design starts
  - Artificial Intelligence
  - 5G
  - Defense - towards FPGAs for Cyber Security issues
  - Automated Driving Solutions (ADS)
  - Hyperscale Data Centers (HDC)
Device Complexity

- Stacked Die Chiplets/Tiles
- New IP
- New IEEE standards
Component Shortage Impacts

- Redesign Decisions
  - Is the component available?
  - What is the current cost?
- IEEE Spectrum articles on Chip Shortages
  - How and When the Chip Shortage Will End
  - 5 Ways the Chip Shortage is Rewiring Tech
Component Shortage – Dynamic Test Tools a Must

- Robust library selection
  - Memories
  - FPGA
  - Logic component
- Test development responsiveness
  - Easy test modifications
- Smart Tests
  - Device ID driven test flow
Counterfeit Components

- Counterfeiters are getting creative
  - How are you managing the risk?

- IEEE article on counterfeit components
ScanWorks Platform

- ScanWorks Products
  - Boundary-Scan Test
  - Board Functional Test
    - Processor-based (Xilinx and NXP SoCs)
  - Fast Programming
    - FPGA-based (Intel (Altera), AMD-Xilinx, Microchip (Microsemi))
    - Processor-based (Xilinx and NXP SoCs)
  - Embedded Diagnostics
    - Custom fielded diagnostics via Baseboard Management Controller
  - IJTAG Test
ScanWorks Platform

- BST
- Interconnect
- Memory Access Verify
- Component Action
- Define the device(s) in the JTAG chain
- Add the actions
  - Enable the Arm_DAP via SVF
  - Interconnect Test
  - MAV Test
Component Action

- Provide control access to Test Enable (TEN)
- Connect PS_DDR_TEN0 to memory devices
Xilinx Zynq UltraScale+ MPSoC

- PS connections
  - QSPI
  - DDR4
  - eMMC
  - I2C
  - Ethernet PHY
ScanWorks Platform

- Functional Test
  - DDR4
  - Device Presence
  - Ethernet PHY
- Programming
  - NAND/NOR
  - SPI/QSPI
  - SDMMC/eMMC
### Programming Methods Consideration

- **BST**
  - SoC boundary scan
    - NAND, NOR, SPI, QSPI, eMMC
    - Connected to JTAG enable device
  - SPI DIO
    - GPIO control
  - SoC – Processor System or FPGA Fabric
    - If Processor – PFP
      - NAND, NOR, SPI, QSPI, SD/MMC, eMMC
      - Ethernet data download
    - If Programmable Logic – FFP
  - FPGA Standalone
    - FFP
  - SPI Direct – RIC-1400
    - Flash Header access
## ScanWorks Programming Speed Technology Comparison

<table>
<thead>
<tr>
<th>Access Method</th>
<th>TCK</th>
<th>SoC Clock</th>
<th>FPGA Clock</th>
<th>Programming File Size</th>
<th>Erase/Program/Verify Time</th>
<th>Improvement</th>
<th>Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boundary-Scan Chain</td>
<td>12 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td><strong>35 minutes</strong> (2100 seconds)</td>
<td></td>
<td>UUT JTAG Clock Rate /BST Register</td>
</tr>
<tr>
<td>Short Chain</td>
<td>12 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td><strong>4 minutes</strong> (240 seconds)</td>
<td>~9x</td>
<td>Supported FPGA Families</td>
</tr>
<tr>
<td>SPI DIO</td>
<td>45 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td>2 minutes 5 seconds</td>
<td>17x</td>
<td>SPI Header</td>
</tr>
<tr>
<td>PFx Programming</td>
<td>30Mhz</td>
<td>800 MHz</td>
<td>NA</td>
<td>1MB</td>
<td>11 seconds</td>
<td>190x</td>
<td>UUT JTAG Clock Rate</td>
</tr>
<tr>
<td>PFx Programming Via Ethernet</td>
<td>30Mhz</td>
<td>800 MHz</td>
<td>NA</td>
<td>1 MB</td>
<td>2.4 seconds</td>
<td>78x</td>
<td>Supported SoC Only</td>
</tr>
<tr>
<td>FPGA-based SPI Flash Programming</td>
<td>30 MHZ</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>1 MB</td>
<td>2.3 seconds</td>
<td>91x</td>
<td>Supported FPGA Families</td>
</tr>
<tr>
<td>SPI Direct</td>
<td>10 MHz</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>1 MB</td>
<td>2.3 seconds</td>
<td>91x</td>
<td>RIC-1400 and SPI Header</td>
</tr>
</tbody>
</table>
ScanWorks Demo Configuration

SourcePoint®
Platform for Software Debug and Trace

© 2022, ASSET InterTech, Inc.
ScanWorks Demo
ScanWorks Addressing Technology Trends

- We demonstrated how ScanWorks can address both structural and functional testing during this era of chip shortages and redesign impacts that occur when moving from one silicon provider to another. The demonstration showed the various ways of attacking various problems that can be manifested in device complexity as you move to newer more powerful and sophisticated silicon.
You or your competitor will be the leader by the tool choices made during these time of component shortages.
- BST
- PFT
- FFP
- PFP
- eResources
  - eBooks
  - Videos
Questions and Contact Information

Contact Information:
Larry Osborn
7161 Bishop Rd. Ste. 250
Plano, TX 75024
Larry.Osborn@asset-intertech.com
www.asset-intertech.com
Real Insight from Code to Silicon