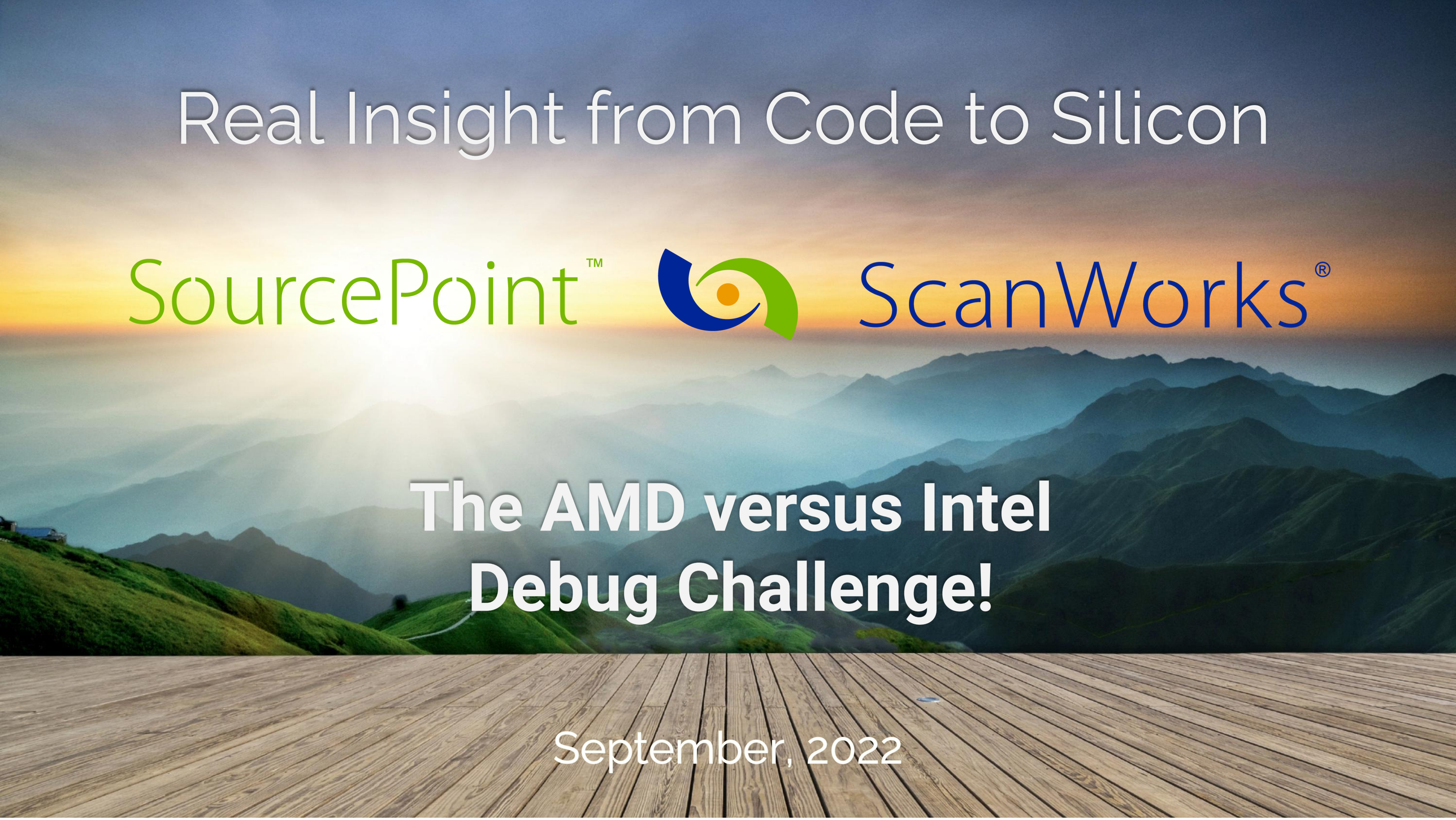

Real Insight from Code to Silicon
SourcePoint™
ScanWorks®
The AMD versus Intel
Debug Challenge!
September, 2022

Agenda

- Setup
- Basics of Run-Control and Trace
- Intel Advantage:
  - Intel Processor Trace
  - Trace Hub Message Trace
  - Architectural Event Trace
- AMD Advantage:
  - Advanced Breakpoints
- Demos
- And the winner is….

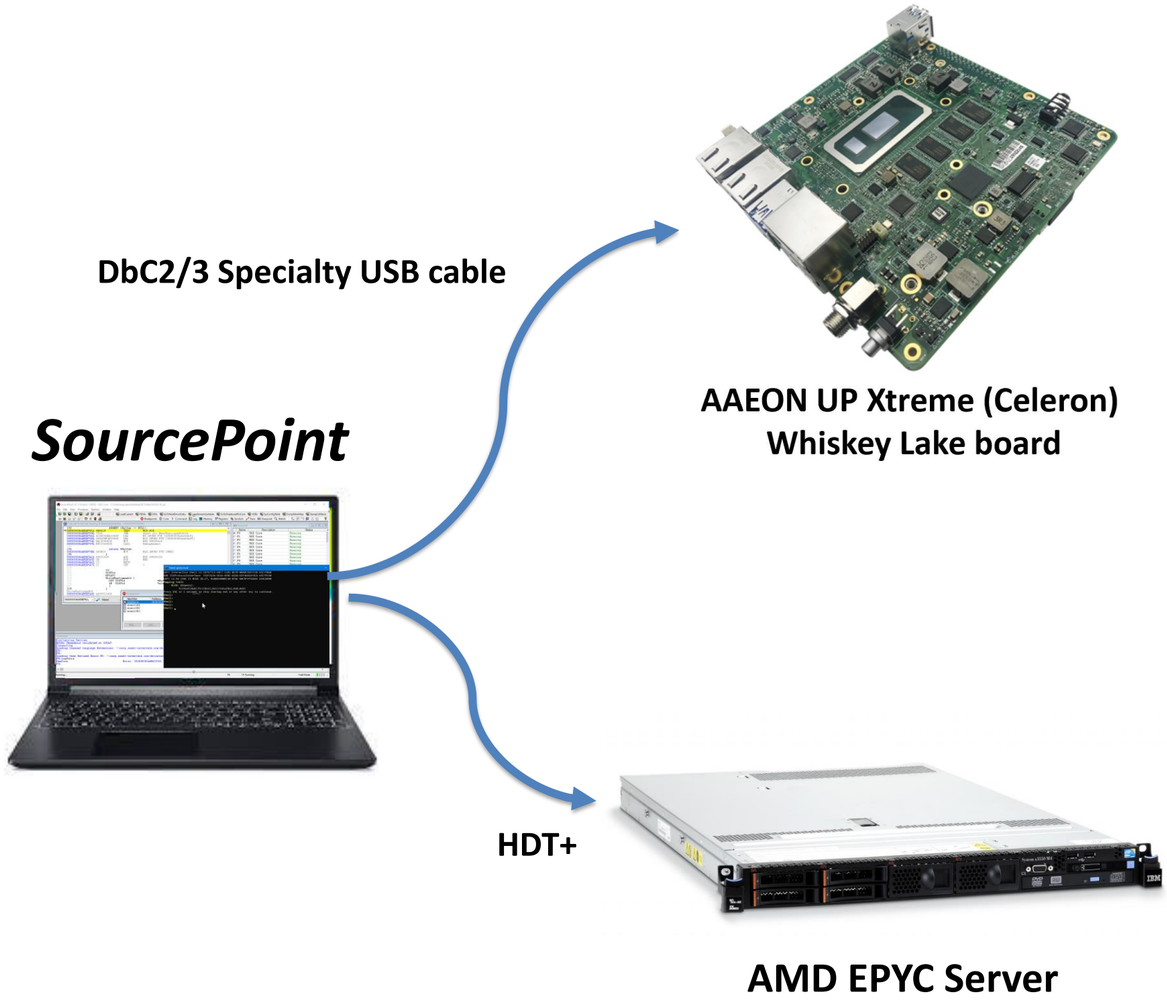
Setup

Intel target configuration

- AAEON UP Xtreme Whiskey Lake board via DCI

AMD target configuration

- Server (EPYC) via HDT+ interface



Basics of Run-Control

- Halt / Go
- Single-step
- Breakpoints
  - Hardware; Software; Data Access; Data Write; SMM; Reset; Power Cycle; etc.
- Symbols
- Watch Windows
- etc.

Basics of Trace

- Last Branch Record (LBR)
  - Instruction trace
  - Use MSR pairs for To/From branches
  - Limited number of pairs; a couple of hundred instructions

Advantage Intel: Trace

- Intel Processor Trace
  - Instruction trace
  - Requires DRAM on target; lots of trace
- Trace Hub Message Trace
  - ME trace; SVEN; At-Speed Printf; etc.
- Architectural Event Trace (AET)
  - Event trace
  - MSR reads/writes; Port In/Out; Code breakpoints; Data breakpoints; etc.

Advantage AMD: Advanced Breakpoints

- An address range can be specified for data breakpoints. Any Data Access or Data Write will cause a break, independent of data value
- A specific data value can be targeted for a Data Access or Data Write, for a single address
- Don’t Cares can be specified in addresses for hardware breakpoints (Execute, Data Access, Data Write, and I/O Access). For the latter three, specific data values or masked data values can be specified.

Advantages

Intel

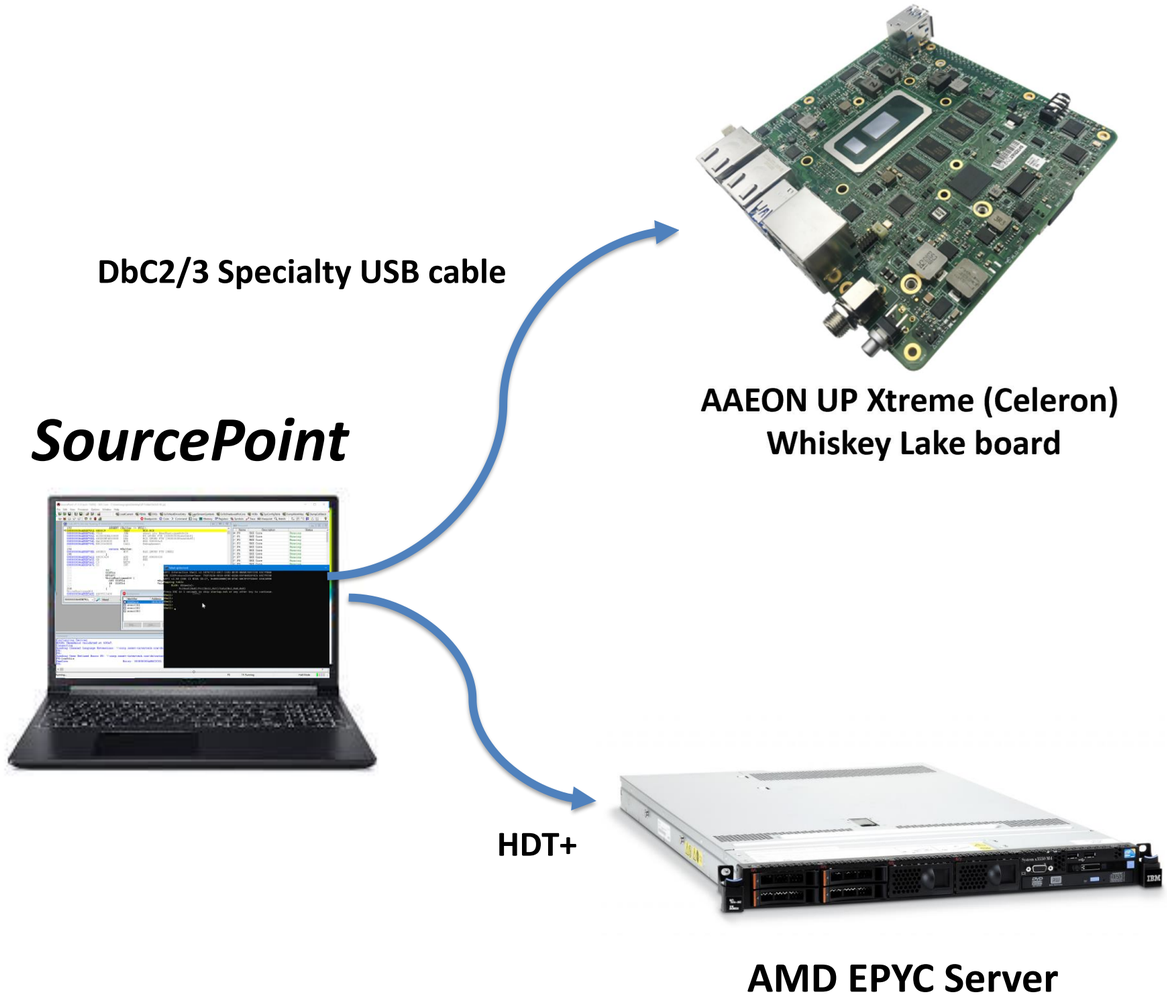
+ DCI
+ Intel Processor Trace
+ Trace Hub Message Trace
+ Architectural Event Trace

AMD

+ Data breakpoint address range
+ HW breakpoint address mask
+ Data value breakpoint

Demo

- The demo will last ~ 20 – 25 minutes
- The vote for best debug will come immediately after!



Compare and Contrast

	AMD	Intel
Run-Control	✓	✓
LBR Trace	✓	✓
Processor Trace	✘	✓
Trace Hub	✘	✓
Event Trace	✘	✓
Data BP address range	✓	✘
Data value BP	✓	✘
HW BP Don’t Cares	✓	✘

And the Winner is…

References

- **SourcePoint Academy**:
  https://www.asset-intertech.com/resources/academy/sourcepoint-academy/
  “How To” Guides and all our technical documentation online

- **Blogs**:
  https://www.asset-intertech.com/resources/blog/category/arium-probes-sourcepoint/
  Tons of articles on timely debugging and JTAG topics

- **Videos**:
  https://www.asset-intertech.com/resources/videos/
  Our recorded webinars: DCI debug of UEFI and hypervisor technologies on the AAEON UP Whiskey Lake and Tiger Lake boards, JTAG-based debugging of AMD EPYC servers, etc.

- **Webinars**:
  https://www.youtube.com/c/UEFIForum/videos
  Beyond Printf – Real-Time Firmware Debugging
  UEFI Debug with Intel Architectural Event Trace
  JTAG-based Debug & Trace

Wrap-Up

- Questions?

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