SourcePoint® 7.12 Release Notes

Content

Contact Us

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Requirements

Host Operating Systems Supported
Windows 10, 11

Note: You may need to contact your systems administrator to gain administrator privileges on your host computer to properly install SourcePoint. The Installation wizard may give false errors of other uninstall programs running when administrator privileges are not enabled.

New Features and Errata

Version 7.12 Build 22 – July, 2022

Our latest build has the following major enhancements:

- UEFI macro enhancements for GCC compiler
- Sapphire Rapids-HBM support
- Sapphire Rapids R0, L0, L0 support
- VMExit and VMLaunch hypervisor breakpoint support

- Full Alder Lake support of all Core/Atom configurations, with Trace
- Enhancement to bitfield display for structures with union
- Rocket Lake DCI support
- Raptor Lake support
- Enhanced support for AET with LBR
- CScripts support for Python 3.6.x rather than Python 2.7.
- Peek Memory: allows the reading of 32 bits of data using a register as the memory address
- Find MSR feature: search the Register view for an MSR by number.

There are still open errata that will be addressed in an upcoming release. “TT” is short for “Trouble Ticket”:

TT-16540	**SPR**: DbC support needed (workaround is to use ECM-XDP3e instead)
TT-16414	**RKL**: No AET trace with DbC
TT-16407	**RKL**: LBR and BTS trace not working with DCI
TT-16399	**ALL**: No DCI support for CScripts (NO FIX)
TT-16386	**JSL**: DCI gets wrong register values in Code window
TT-16375	**RKL**: Reset target not functional
TT-16353	**EHL**: Power cycle and reset are not supported
TT-16352	**JSL**: Power cycle and reset are not supported
TT-16330	**JSL**: Soft breaks do not work. Workaround: use hardware (processor) breakpoints
TT-16318	**ADL**: Trace hub based trace (AET and SW/FW trace) has not been validated yet
TT-16310	**ADL**: DbC has not been validated yet
TT-16253	**APL**: DbC reset and power cycle support not functional
TT-16229	**ICX**: DbC reset and power cycle support not functional
TT-16183	**TGL-U**: When restore hardware breaks on reset is enabled, SourcePoint not able to stop the target
TT-16124	**ICX**: Power cycle support not functional
TT-TBD	**WHL and earlier**: DCI Trace to System Memory not functional (workaround: use Trace to DbC/MTB where available)
TT-TBD	**RPL**: Trace to System Memory not functional, DCI and ECM-XDP3e
TT-TBD	AAEON **WHL** board supports Trace Hub trace to MTB only out of reset. For DCI streaming trace, works only after DXEMAIN.

For SPR, note that the first reset of a Sapphire Rapids target after loading the SourcePoint project does not stop the target at the reset vector. To stop the target at the reset vector, power cycle it after loading the SP project. The Reset button should then work for the remainder of the debug session. Here are the steps:

1) Power on XDP3e
2) Power on Sapphire Rapids target
3) Start SP and load project
4) Turn off target

5) Turn on target
6) Click on the Reset button
7) Verify that the target halts at the reset vector

For ICX-D:
1. We have noted that, on some targets, it is necessary to increase the stability time after reset to successfully stop at the reset vector. In the Options menu, go to Emulator Configuration, select the Target Reset tab, and increase the "After target reset, emulator will wait…." from what may be the default of 100 milliseconds to 400 milliseconds.
2. With reset break set, the target does halt but with some slip, after issuing a reset from the target UEFI console (looks like a cold reset).
3. With init break or power cycle break set, the target resets but continues to boot (all the way to the UEFI console), after issuing a reset from the target UEFI console (looks again like a cold reset).
4. Setting power cycle break and power cycling the target locks up both SourcePoint and the target (i.e. no JTAG at all). The only way out of this is to quit the emulator, power cycle the target, wait for it to begin booting and then bring back up the emulator again, at which point you can then turn the power cycle break off again.

A key erratum for JSL is the inability to halt the target at the Reset Vector via either a Power Breakpoint or a Reset Breakpoint.

To see the current status and differences between current offerings of open chassis (ECM-XDP3e) debug and closed chassis (DCI/DbC) debug, please refer to the following tables:

ECM-XDP3e:

	Run-Control	LBR	BTS (to system memory	Intel PT (to system memory)	UEFI and ME message trace (thru Trace Hub) to memory and MTB	AET (thru Trace Hub) to memory, MTB
SERVER & WORKSTATION						
Skylake Server	√	√	√	√	√	√
Cascade Lake Server	√	√	√	√	√	√
Ice Lake Server	√	√	√	√	√	√
Sapphire Rapids	√	√	√	√	√	√ (no LBR)
Fish Hawk Falls	√	√	√	√	√	√
ICX-D	√	√	√	√	O	O
CLIENT						
Skylake Client	√	√	√	√	√	√
Kaby Lake Client	√	√	√	√	√	√

Amber Lake Client	√	√	√	√	√	√
Coffee Lake Client	√	√	√	√	√	√
Whiskey Lake Client	√	√	√	√	√	√
Cannon Lake Client	√	√	√	√	√	√
Ice Lake Client	√	√	√	√	√	√
Comet Lake Client	√	√	√	√	√	√
Tiger Lake Client	√	√	√	√	√	√
Jasper Lake	√	√	√	√	O	O
Elkhart Lake	√	√	√	√	O	O
Rocket Lake	√	√	√	√	√	√
Alder Lake	√	√	√	√	√	√
Raptor Lake	√	√	√	√	O	O

√ In current release
O In Upcoming release
X Not supported

DCI/DbC:

	Run-Control	LBR	BTS (to system memory	Intel PT (to system memory)	UEFI and ME message trace (thru Trace Hub) to memory and MTB	AET (thru Trace Hub) to memory, MTB	UEFI and ME message Trace (thru Trace Hub) to DCI/ DbC Streaming Trace	AET (thru Trace Hub) to DCI/ DbC Streaming Trace
SERVER & WORKSTATION								
Skylake Server	X	X	X	X	X	X	X	X
Cascade Lake Server	X	X	X	X	X	X	X	X
Ice Lake Server	√	√	√	√	√	√	X	X
Sapphire Rapids	√	O	O	O	O	O	O	O
Fish Hawk Falls	√	O	O	O	O	O	O	O
ICX-D	√	√	√	√	X	X	X	X
CLIENT								
Skylake Client	X	X	X	X	X	X	X	X
Kaby Lake Client	X	X	X	X	X	X	X	X
Amber Lake Client	X	X	X	X	X	X	X	X

Coffee Lake Client	√	√	√	√	√	√	√	√
Whiskey Lake Client	√	√	√	√	√	√	X	X
Cannon Lake Client	X	X	X	X	X	X	X	X
Ice Lake Client	√	√	√	√	√	√	√	√
Comet Lake Client	√	√	√	√	√	√	√	√
Tiger Lake Client	√	√	√	√	√	√	√	√
Jasper Lake	O	O	O	O	O	O	O	O
Elkhart Lake	O	O	O	O	O	O	O	O
Rocket Lake	√	√	√	√	√	√	√	X
Alder Lake	√	√	O	√	√	√ (no LBR)	√	√ (no LBR)
Raptor Lake	√	√	√	√	√	O	O	O

√ In current release
O In Upcoming release
X Not supported

Notes:

Run-Control: standard Halt, Go, Single-Step, etc. commands.

LBR: Last Branch Record uses MSRs.

BTS: Branch Trace Store uses system memory.

Intel PT: Processor Trace uses system memory.

UEFI, AET and ME message trace use the Trace Hub, and can deliver trace data to system memory, MTB, or (with DCI DbC support) Streaming Trace out of reset.

MTB is Memory Storage Controller Trace Buffer and captures trace data directly from reset. Typically 2kB - 8kB in size.

Current Client platforms and Xeon platforms Sapphire Rapids and later support DbC2 (run-control + streaming trace over USB2). ICX supports DbC3 (run-control + trace over USB3) – which lacks power cycle/reset control.

Version 7.12 Build 16 – September, 2021

7.12.16 has the following new features and fixes:

- Update to Visual Studio 2019 toolchain
- Python 3.x support for CScripts
- New Project Wizard with Target Identification
- Sapphire Rapids reset fix and support through E0 (PRQ) stepping
- Alder Lake big.little support

- ICX-D U0 support
- Software breakpoints for JSL and EHL fixed
- Multithread AP code execution segment register display fixed

A detailed list of the issues ***resolved*** in this release is as follows (note: TT is short for "Trouble Ticket"):

TT-16449	Add memory map entry when Trace Hub CSR BAR is above 4GB
TT-16441	Incorrect text in GetNvVariableDataAddr() error printf in Variable.mac
TT-16440	**EHL**: Corrupted GPRs display in PEI
TT-16442	DCI displays "Not Active" threads
TT-16415	DumpACPITable() in AcpiTable.mac errors when it gets to SLIT table
TT-16409	**SPR**: C0 stepping not supported yet
TT-16408	Font size issue at 3840x2400 resolution
TT-16401	Wrong register/memory values after forced harvest of non-active processor
TT-16381	**SPR**: New architectural LBR support
TT-16365	**ICX-D**: U0 stepping not supported yet (Y0 is supported)
TT-16351	**EHL**: Soft breaks do not work. Workaround: use hardware (processor) breakpoints
TT-16358	**SPR**: Reset not supported. Workaround: User power cycle breakpoint
TT-16332	**JSL**: Target sometimes becomes unstable when trace is enabled. Occurs with LBR, BTS and Intel PT
TT-16276	**ADL**: Little Core not supported yet **ADL**: SP corrupts break address data (on Atom only) when SMM entry break and softbreak is set **ADL**: SMI breakpoints issue on Atom. Some GPR's, memory (and disassembly window) report wrong/bad data.

Version 7.11

Build 113

ICX-D U0 Support - Run control support added for ICX-D U0.

JSL breakpoint issue - Software breakpoints are now functional on Jasper Lake.

EHL breakpoint issue - Software breakpoints are now functional on Elkhart Lake.

EHL register corruption issue - Certain general register values would get corrupted during PEI debug. This has been resolved.

Build 109

SPR B0 dual package issue - Fixed issue with CS and SS registers first thread in second package sometimes cleared after running to breakpoint.

Build 108

SPR B0 support - Run control support added for SPR B0 stepping

Build 107

ADL-S support - Run control support added for ADL-S. Only the Core cores are supported at this time. Atom cores are ignored.

Build 106

TGL R0 support - Run control support added for TGL R0 stepping

EHL RCX issue - Fixed issue with RCX sometimes cleared when running to hardware breakpoint

Build 103

ICX-D support - Run control support added for ICX-D Y0/U0 stepping

RKL Trace Hub support - Trace Hub support added for RKL

Eagle Stream CScripts support - Support added for Eagle Stream (SPR) CScripts

Build 102

TGL P0 support - Run control support added for TGL P0 stepping

Build 100

Rocket Lake (RKL-S) - Run control support added for RKL-S

SPR Trace support - LBR, BTS and Intel PT trace support added for SPR

Build 99

Elkhart Lake support (EHL) - Run control support added for EHL

ICX AET support - AET trace support added for Ice Lake Server

Build 97

Sapphire Rapids support (SPR) - Run control support added for SPR.

SKL-D support - Run control support added for SKL-D.

Build 96

Jasper Lake support (JSL) - Run control support added for JSL

Build 95

IceLake Server (ICX) C0 support - Run control support added for ICX C0 stepping.

NDA processor support - Intel processors still under NDA are now supported in the standard SourcePoint release. It's no longer required to visit the SourcePoint Community to download support files.

Build 91

Comet Lake (CML) P0 support - Run control support added for Comet Lake P0 stepping

Build 89

Comet Lake (CML) G0 support - Run control support added for Comet Lake G0 stepping

Comet Lake (CML) DbC support - Run control support (via DbC) added for Comet Lake

Tiger Lake (TGL) DbC support - Run control support (via DbC) added for Tiger Lake

DbC connection status utility - DbC connection utility now provided with SourcePoint release. This utility is useful for troubleshooting DbC connection issues. It indicates whether the host computer's DCI driver has a valid connection to the target.

IceLake server (ICX) trace support - LBR trace and Intel PT trace are now supported on ICX.

Build 80

Comet Lake (CML) support - Run control support added for Comet Lake

Tiger Lake (TGL) support - Run control support added for Tiger Lake

Build 79

IceLake Server (ICX) support - Run control support added for two-package ICX.

Build 76

Ice Lake Server (ICX) support - Run control support added for ICX. Single package only.

DCI support - Added support for DCI (DbC). Allows for debug through a USB connection (without a debug probe).

MCE Breakpoints - New MCE breakpoint type allows trigger on machine check exceptions

Version 7.10.4

5th Generation Intel® Xeon™ processor (codename Skylake) – SourcePoint now supports the new 5th Generation Intel® Xeon™ processor.

Windows 10 support

Gemini Lake Support – Added support for GLK processors

Coffee Lake Support – Added support for CFL processors (requires NDA)

Cannon Lake Support – Added support for CNL processors (requires NDA)

IceLake Support – Added support for ICL processors (requires NDA)

BSSB Trace – Added support for BSSB streaming trace (requires DCI connection)

CFL Trace – Added support for CFL trace (requires NDA). Includes Intel PT, Software trace through the Trace Hub, and AET trace through the Trace Hub.

CNL Trace – Added support for CNL trace (requires NDA). Includes Intel PT, Software trace through the Trace Hub, and AET trace through the Trace Hub.

VS 2015 Support - Added symbolic support for VS 2015 compiler.

Improved C-State Handling

ICL Trace - Added support for ICL trace (requires NDA). Includes Intel PT, Software trace through the Trace Hub, and AET trace through the Trace Hub.

LBR Trace Bug Fix – Fixed bug that resulted in incorrect LBR trace when going off of a breakpoint.

Version 7.10.3

Trace Hub Support - SourcePoint now supports software / firmware trace through the Intel Trace Hub to system memory.

Intel PT Timestamp - SourcePoint now supports TSC, MTC and TMA packets in Intel PT. This allows Intel PT from multiple cores to be time aligned.

Version 7.10.2

Intel Processor Trace Support – Added support for Intel Processor Trace (Intel PT). See the Trace view section for more information.

Trace Search View - The Trace Search view has been added to support Intel PT. This view supports high level views of the trace. The view can be opened from the Trace view context menu.

Trace Statistics View - The Trace Statistics view has been added to support Intel PT. This view supports function profiling of instruction trace data. The view can be opened from the Trace view context menu.

Version 7.10.1

IvyTown Support - Support added for IvyTown including ureg_raw command and Python-CLI device model.

Alternate Processor Numbering - SourcePoint now supports both the Arium and ITP processor numbering schemes. The ITP numbering scheme is selected by setting the ItpCompatible control variable true.

XDP-Pins - The LX-INT tab in the Emulator Configuration dialog has been reworked to support the new LX-INT rev E-1 adapter. The tab has been renamed "XDP-Pins"

GD Bit - SourcePoint now supports the GD bit in DR6 to break on target software modifying the DR registers.

Improved Program Load Verification - When verifying a program loaded symbols only, SourcePoint now allows individual sections to be excluded from the verify (e.g., the Init section in a Linux kernel load).

Version 7.10

Target Configuration – Target configuration is now handled by a series of new commands executed in the target configuration event macro. See the new Target Configuration Application Note for more information.

Python Support – SourcePoint now has limited support for the Python Command language.

1024 Processor Support – The number of processors (threads) supported has been increased from 64 to 1024.

Haswell Support – The Haswell processor is now supported including Haswell NI instructions.

Editing of Macro File Errors – The Macro error dialog now allows opening an editor to fix macro file errors, and then resumption of the macro.

SelectFile and SelectDirectory commands – These new commands open dialogs to allow a filename or directory path to be returned to an nstring variable.

Symbol Search Improvement – The Symbol Finder dialog (Edit | Find Symbol) now allows searching for a symbol across multiple programs.

Program Save Improvement – The Program Save dialog now allows for saving a region of memory as an axf file. The Save (Upload) command also supports this.

Viewpoint View Improvements – The Viewpoint window now allows sleeping processors to be automatically hidden from the display. It also allows for individual processors to be hidden.

The following target configuration commands have been added (see Target Configuration Application Note for more information)

- ***JtagTest***
- ***JtagScan***
- ***JtagConfigure***
- ***VerifyJtagConfiguration***
- ***UncoreScan***
- ***UncoreConfigure***
- ***DeviceScan***
- ***DeviceConfigure***
- ***VerifyDeviceConfiguration***
- ***Autoconfigure***

- ***Disconnect***
- ***Reconnect***

Emulator

The table below describes the behavior of the status LEDs on the front of the emulator.

STS	Lights briefly after emulator has performed boot-level hardware initialization and prior to loading flash image. Also, the upper and lower amber LEDs flash in an alternating pattern if the flash file fails to load.
RST	When lit, the target is in reset mode.
RUN	When lit, the target is running.
PWR	When lit, the emulator's power is on.

The table below describes the behavior of the network LEDs on the back of the emulator.

100BT	When lit, the emulator is communicating at 100Mb/s
LINK	When lit, indicates Ethernet is connected.
RECV	When lit, indicates Ethernet is receiving data.
