DDR Memory Test: Modern Tools for Validation, Test and Debug

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Summary

The ongoing supply chain bottlenecks across the globe have caused the chip shortages that substantially affect the organization's product development. The outcome from the shortages drives product obsolescence and product redesigns. How does this affect test engineering? Products that were stable and good sellers can no longer be built and tested. Product redesigns can impact the Design for Test (DFT), the tools suitability that are in house, and the time pressure is enormous. Furthermore, we now have more counterfeit components on the market, and counterfeiters are getting better at hiding that fact. Therefore, the challenge of creating a new design in record time while having the manufacturing test rewritten and robust enough to fit the DFT plan are exceedingly difficult at best. Off-the-shelf test solutions or lack thereof will make or break some product lines.

This eBook dives into what is needed to effectively address the problems. This could have been about our ScanWorks BST solution, but instead, we have chosen to look at an existing board design and breakdown some of the test development needs. Too often, the test development needs are discussed late in the product development cycle. Newer devices and newer standards will have an impact on your product release cycle. Will you still be the market leader? Later, we will host a webinar where ScanWorks will be used on the same board and exercise all the various features to address the test complexity posed by this design.

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Overview

With the component shortages, component price hikes (which will continue based upon supply/demand curves), and finished goods inventory being depleted, many product/board manufactures are scrambling to create a new design to replace older ones.

There are at least two key issues that test engineers are facing. The first is the realization that designing with new components similar to what they have used in the past are being snapped up so rapidly that choosing the replacement parts for the "new design" takes on a life of its own and urgency. This pressure is likely to cause design issues. An example scenario is after spending hours selecting a component, then only to find the quantity needed for production is too expensive to make the product viable; thus, it compels them to search for another replacement. The luxury of creating the design based upon paper specifications and product samples without needing to order the part volumes necessary for production has been ceased until the component shortage is over. The component shortage is not likely to be resolved for some time (maybe years) according to some analysts.

The second problem that can be encountered is the tools in house (hardware, software, and test) might be out of date or the license will expire. Will the tools support the new FPGA, processor, SoC, or another intelligent device that you are expecting to use? What if the test tools and methods that were used for the older designs are not compatible with newer silicon advances? This would lead to either update the current tools or look for other tools that meet the DFT criteria. This eBook will take a relatively new design using the Xilinx Ultrascale + MPSoC and examine some of the components from a test perspective then see what is needed to maximize test coverage and performance as specified by IEEE and iNEMI. We will focus on memory devices as the test development and actual testing can be time consuming. The luxury of time is not something we have in these market conditions.

When choosing a tool for board test in rapidly changing times, it is critical that it supports the latest technologies and flexible enough to support legacy components. In our own experience, because of the Spartan-6 shortage announcement from Xilinx, we realized we needed to replace an FPGA in one design. In our research, we found a replacement part that matched the design specification of the old design. However, we discovered that the replacement was out-of-stock, so it pushed us to look for other pin compatible devices. Those devices were either out-of-stock or too expensive which prompted the team into design mode and the selection of a different vendor for our FPGA needs. Thankfully, we use our own ScanWorks products, and it supported the new FPGA due to the robust nature of the tool. Your design change might require a component that is using Chiplets/Tiles, or a new intelligent device that has BIST and used IJTAG for BIST control. Are your board test tools up to date on support of new devices or new standards?

The board for this paper, is the Avent UltraZed SOM (Figure 1) connected to an Avnet IO Carrier Card (Figure 5). The reason for using this board is it covers a spectrum of components that one might be planning to test. We will only examine a few devices but, most of the devices identified in the following paragraphs can be tested either structurally, functionally, or in some cases both.

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System on Module

Many designs today use a System on Module (SOM) implementation to accommodate flexibility in the market space. By using SOMs connected to other board designs, expand the flexibility and offer products to a wider range of customer requirements.

The SOM is fitted with Xilinx Zynq UltraScale+ MPSoC XCZU3EG, this provides a sophisticated SoC with processor and FPGA. Also, there are other devices that provide a rich foundation for developers and testing. The feature list is: DDR4 memory, Gigabit Ethernet PHY, Dual QSPI flash, eMMC flash, I2C EEPROM, USB 2.0 ULPI PHY, and other devices.
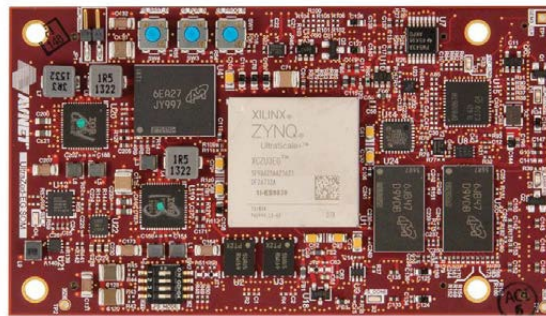

Figure 1 Avnet UltraZed SOM

The block diagram (Figure 2) shows the overall features of this SoC including the processing system (PS) and user-programmable logic (PL) having JTAG access.
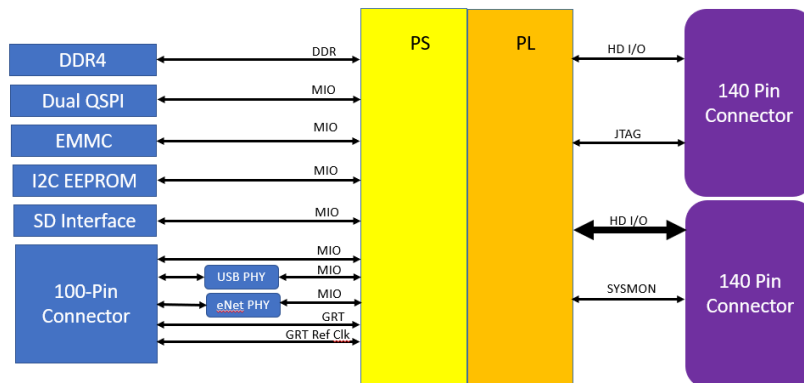

Figure 2 Zynq UltraScale+ Block Diagram

The block diagram is valuable as it shows the device mapping to some of the Multiplexed IO (MIO) space. This will provide the functional test developer some insights as to what may be needed in hardware configuration and device initialization.

The DDR4 memories components on the SOM are two Micron MT40A512M16JY-083E IT:B (96-pin BGA package) creating a 512M x 32-bit interface, totaling 2 GB of random-access memory. They are connected to the Processing Subsystem (PS) bank 504 as shown in the block diagram Figure 3.
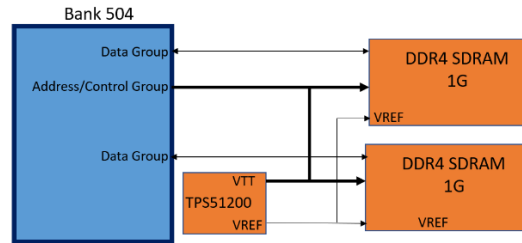
Figure 3 DDR4 to SoC Block Diagram

Also fitted to the SOM are two 4-bit SPI (quad-SPI) serial NOR flash devices organized in a dual configuration. This memory is connected to the PS bank 500 of the MPSoC to provide First Stage Boot Loader (FSBL), secondary boot, and storage as shown in Figure 4.
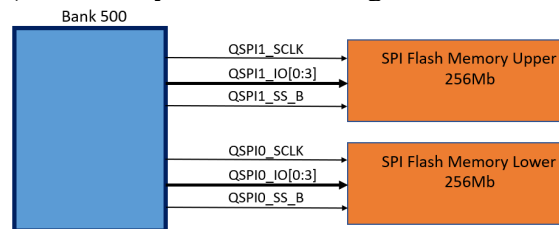

Figure 4 QSPI Flash to SoC block diagram

IO Carrier card

The IO Carrier card provides access to switches, pushbuttons, LEDs, micro-SD connector, USB 2.0/3.0 connector, RJ45 ethernet connector, SATA host interface, and 13 PMOD headers (12 for the PL and 1 PS) for extending access to other devices. Plus, power headers, power switches, Arduino connectors, and display port connectors. Finally, the three JX micro connectors (2 x 140, 1x100) providing the connection to the SOM and a PS JTAG interface.

Figure 5 Avnet IO Carrier Card

Another external memory device is fitted to the IOCC is the microSD connector. This is typically being used for OS, application, and data storage. The device is connected to the PS in the 501 Bank via the JX connector to the SOM.
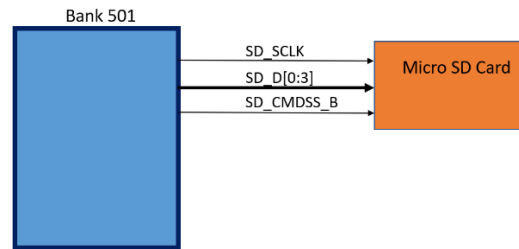

Figure 6 MicroSD to SoC block diagram

Manufacturing Board Test

So far, we have identified several devices that can be accessed for board test. There are two general types of board test: structural and functional. The most cost-effective way of testing a board such as this is via boundary scan using the 1149.1 (JTAG) interface. Digging a little deeper, we find that there are two different JTAG connection points on the carrier card. One is a USB-JTAG device, and the other is a small form factor header.
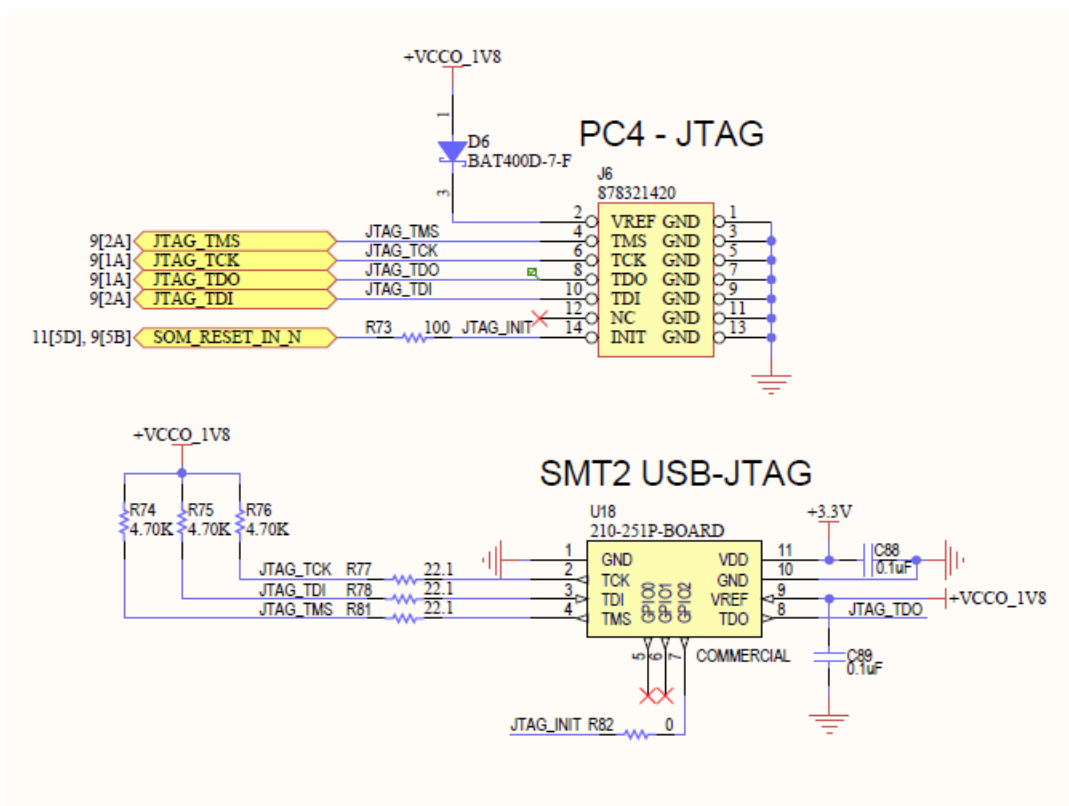

Figure 7 JTAG Connections

Both are connected to the JX1 header and finally connect to bank 503 of the PS on the UltraScale Plus SoC on the SOM.
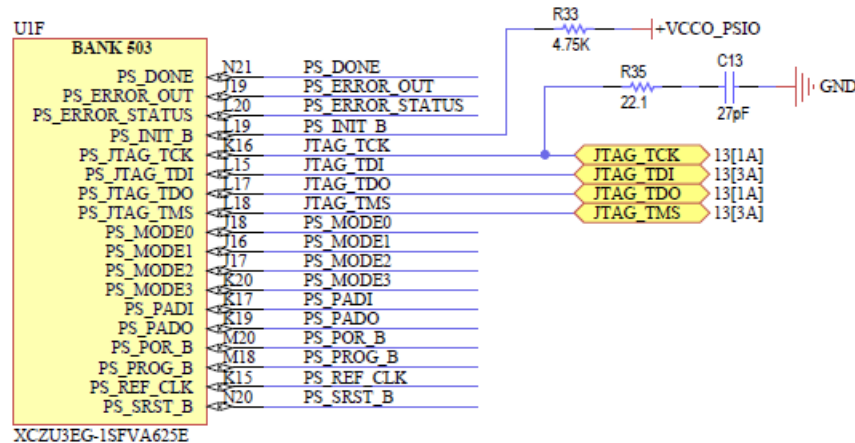

Figure 8 JTAG connection to SoC PS

With the insight to JTAG access, the questions for most designers will be what the board's real estate is, and the Bill of Materials (BOM) cost to determine which JTAG interface is more cost effective.

Test Development

Structural Test

Starting with structural test, we need data such as BSDL from the device vendor, coupled with netlist information about the board to provide the blueprint for what can be tested. Then analyzing the board design to see what the JTAG network structure is, like providing some guidance on what level of testing can be accomplished. In our research of the BSDL files for the SoC on the SOM, we found that there are two JTAG components for the SoC. One is for the SoC, and the other is for the Debug Adapter Port or DAP. In this design, it becomes necessary to enable the DAP to have a full boundary scan access.

The DFT process begins by "peeling-the-design" and seeing what configuration items might be needed like enabling the DAP and other configuration items within the SoC, as necessary. Below is the JTAG path that can be discovered by applying the data to the ScanWorks tool.
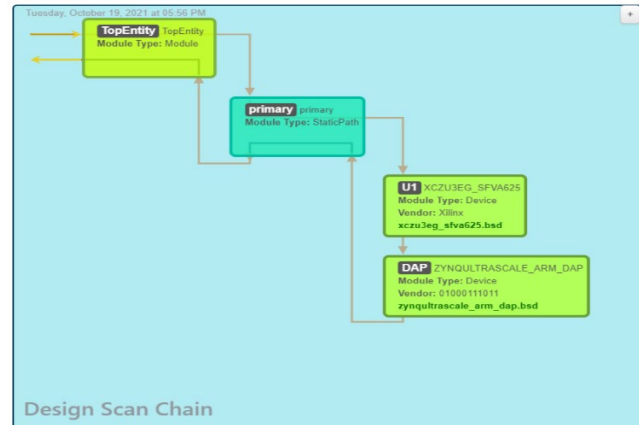
Figure 9 Design Scan Chain

DDR4 Analysis

Beginning with the DDR4 devices fitted to this board, we need to think about the type of structural testing that can be accomplished. We know we need an interconnect test to look for shorts and opens. It would also be helpful to write patterns to the memory to see if there are address or data signal issues. Wagner patterns are helpful in testing the address and data paths that would likely comprise two tests.

To get a better grasp of the potential for test, looking at the data sheets can reveal some good insights as to what is possible.

Looking at the schematics for these DDR4 devices, we see below that this device supports the Test Enable bit (TEN). However, the test enable pin is tied to ground which effectively disables the component test functionality of the DDR4 device.
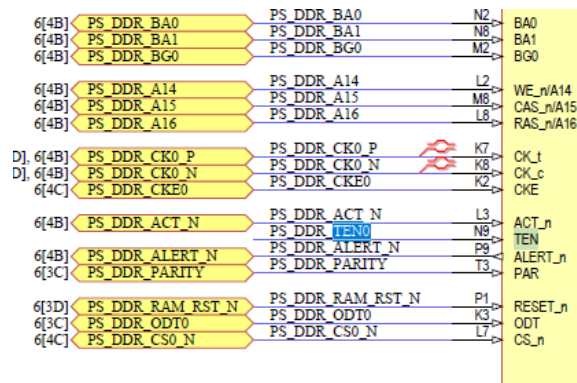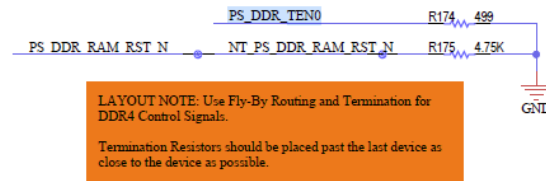

Figure 10 DDR4 TEN connection

Figure 11 DDR TEN Signal

If we were to modify the design and add IO control the TEN0 pin, we could use the Component Test capability in the DDR4 device. ASSET has written several eBooks on DDR testing, and the methodologies are described in Testing DDR Memory with Boundary-Scan/JTAG | Third Edition as just one example.

Our analysis has revealed that we can have structural test for the SOC (processor and FPGA), interconnect test and memory access for the DDR4, and it might be possible to create a component test of the DDR4. There are other components like the ethernet PHY, I2C, SPI flash, SD, and other IO components that could be also structurally tested.

Functional Test

We have examined the board from a structural test perspective. Now let us look at the board from a functional test point. To begin the functional analysis, we will require a deeper understanding of the PS unit of the SoC. Digging into the Technical Reference Manuals (TRM), we see that there are several embedded controllers built into the PS. Understanding the functional initialization of these controllers are necessary for test.

The first components we will look at are attached to the Multiplexed IO (MIO) signals. In Figure 12, the MIO has the GEM 1G Ethernet, SDIO, SPI, and other IO devices that can be connected to the PS. However, using the MIO requires some level of configuration as there are a limited number of MIO pins. Seventy-eight (78) of the general purpose I/Os (GPIO) are used as MIO. So, the board will need to boot or otherwise be configured properly. Needing to boot boards in a production environment always seems to be problematic. If the test tool can initialize the mux, then all the better.
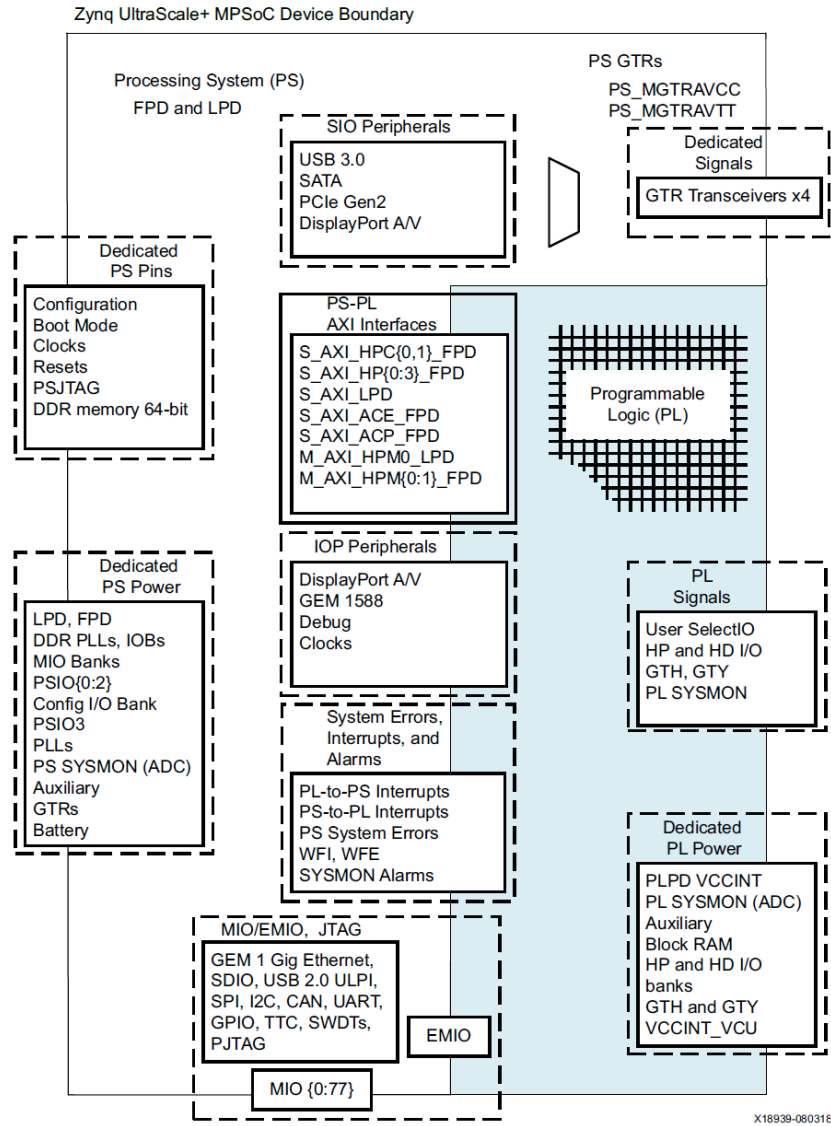
Figure 12 PS Interface Block Diagram

1Gib Ethernet functional Analysis

Looking at the TRM, Gigabit Ethernet Controller implements 10/100/100 Mb/s Ethernet MAC. The PS is equipped with four controllers. Fortunately, on the Avnet board, we are only dealing with one. Each GEM controller provides the management data MIO interface for PHY management. This configuration and access to the PHY provide a means to functionally test the PHY interface. There is a loopback mode that can be used in production test and can be done via functional test. Figure 13 provides a high-level look at the GEM interface. Your tools need to be able to load the appropriate configuration registers or have software (firmware or test) to do the correct initialization. Subsequently, some software will need to be developed to exercise/test the interface.
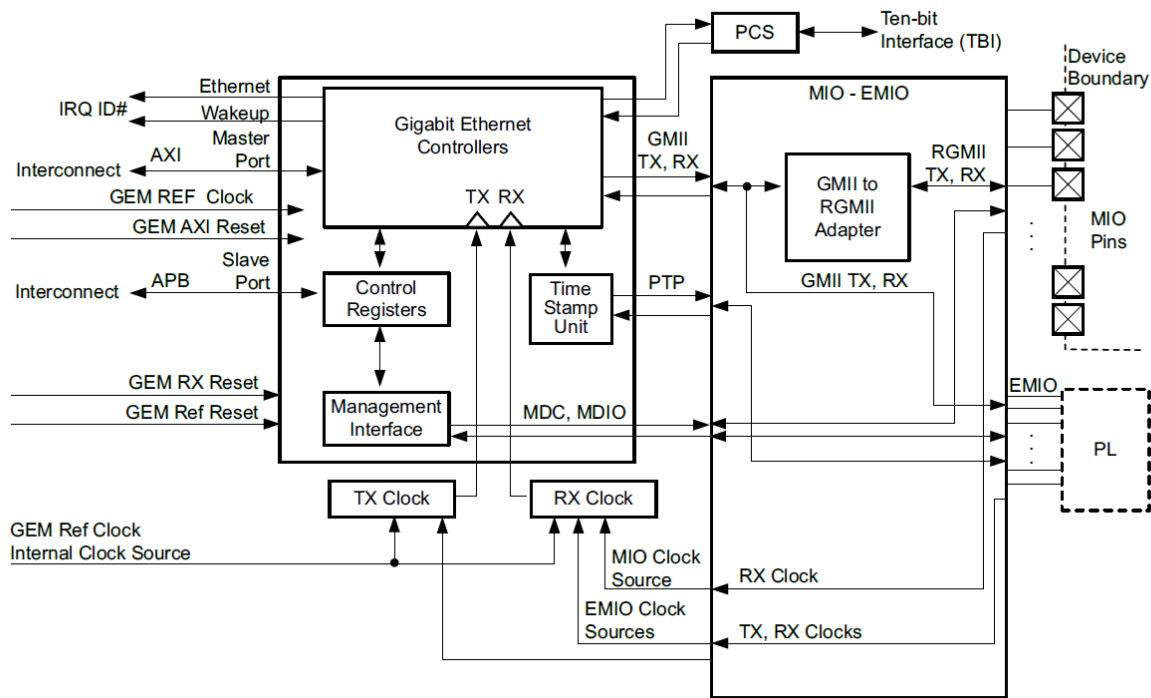
Figure 13 GEM Ethernet System

Quad-SPI Controller

We learned from the structural analysis that there are two memory devices; the data path is x8 on a parallel interface and the memories components are configured for quad mode. Looking at the TRM, we see there are two Quad-SPI controllers in the PS. One is a legacy, and the other is generic; however, they can only be enabled one at a time.
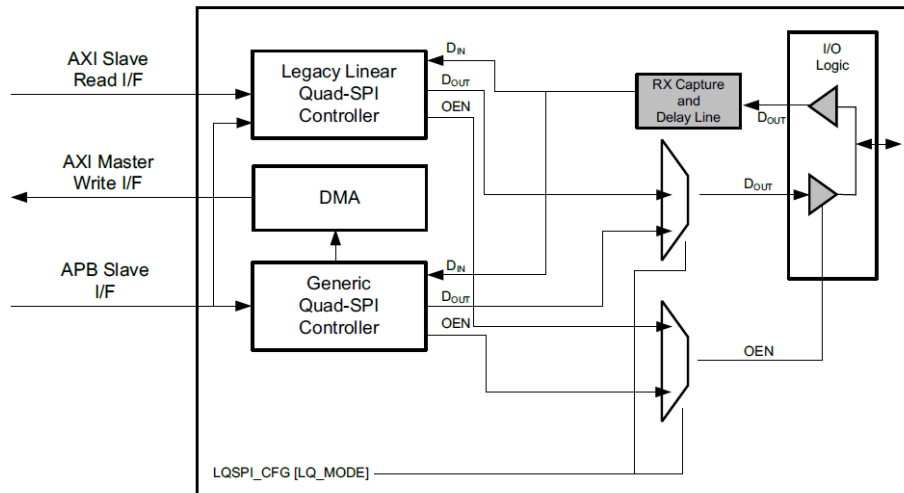

Figure 14 QUAD-SPI Controller

The TRM provides data on how to initialize and operate this controller although there are fifty-five pages to cover just the Quad-SPI controller. Items that need to be configured are the following: Chip Select, Max Clock rate, and Max clock rate reads. Setting these clock rates requires a knowledge of the PS Clock subsystem, which is yet another chapter. Other configuration items that the programming software will need are: Total device size, Erase Sector size, write buffer size, program timeout and erase timeout. Software would then need to be developed to implement the SPI commands Sector Erase, Read ID, Read, Write. The programming flow chart is also in the TRM, but it involves a bit of work to get this functional. The best approach, considering the time-to-market is purchasing test tools that reduce the effort for test/programming development.

SDIO Controller

There are two SD controllers in the PS and they can operate independently. In SD mode data transfers are in either 1-bit or 4-bit mode. In the TRM, all the supported standards for SD are sited in which the controller is compatible with. Mapping the MIO pins to the SDIO interface can be a bit challenging. The BootROM expects the SD card interface to be connected on MIO pins 13 through 25 for SD0 and MIO pins 39 through 51 for SD1. And yes, the TRM has a whole chapter on the MIO. The configuration of the SD controller has many aspects such as Command Control, SD Transmit and Receive Control, Clocks and Resets just to name a few.
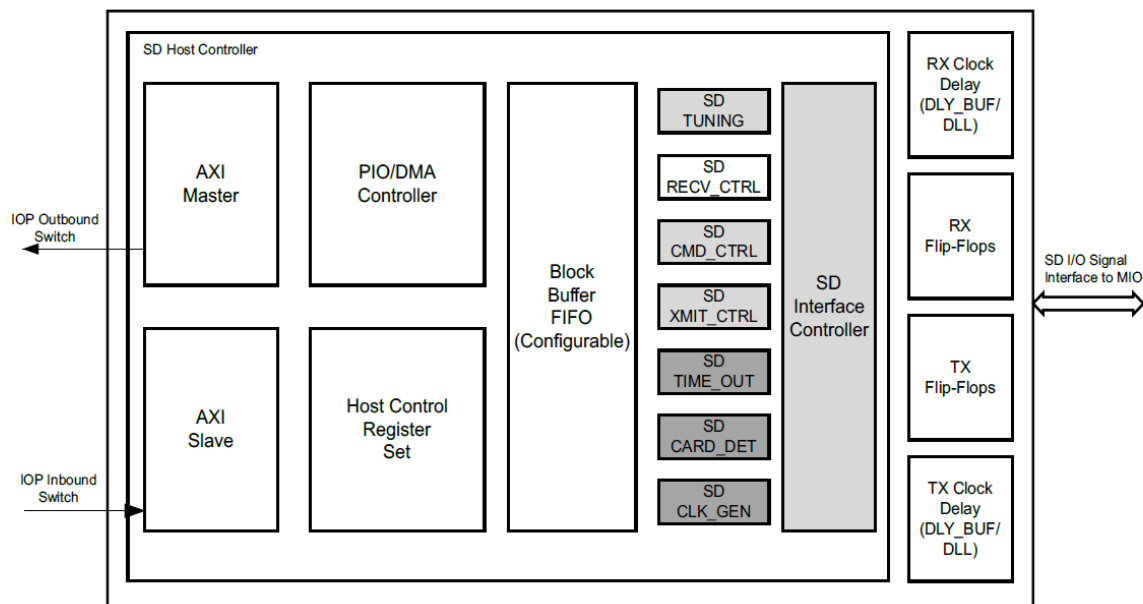

Figure 15 SDIO Controller Block Diagram

That is enough of the MIO analysis. If your redesign is moving from something much older and less sophisticated than what you can find in the market, it is very necessary to look at the board test and the tools in-house to determine the best path forward.

DDR Controller

Earlier in this document, we discussed structural test for the DDR4 memories on the SOM. One item to point out is that boundary scan test operates at JTAG clock frequencies and thus, even though the test can pass (interconnect and memory action verification), there still can be a problem as the memory is not being accessed at processor clock rate. Therefore, cross talk or other signal integrity errors can be missed. Additionally, the second test of the DDR4 memories should be functional tests. The DDR controller in the PS of Zynq UltraScale+ MPSoC subsystem supports DDR3, DDR3L, LPDDR3, DDR4, and LPDDR4. It can accept, read, and write requests from six application host ports that are connected to the controller using AXI bus interfaces. The connection are as follows: Real Time Processing Unit (RPU) tightly coupled memory (TCM), PL block UltraRAM memories, cache coherent interconnect (CCI), FPD DMA, and the DisplayPort controller. Accessible memories also include the external DDR DRAM and the internal On-chip memory.
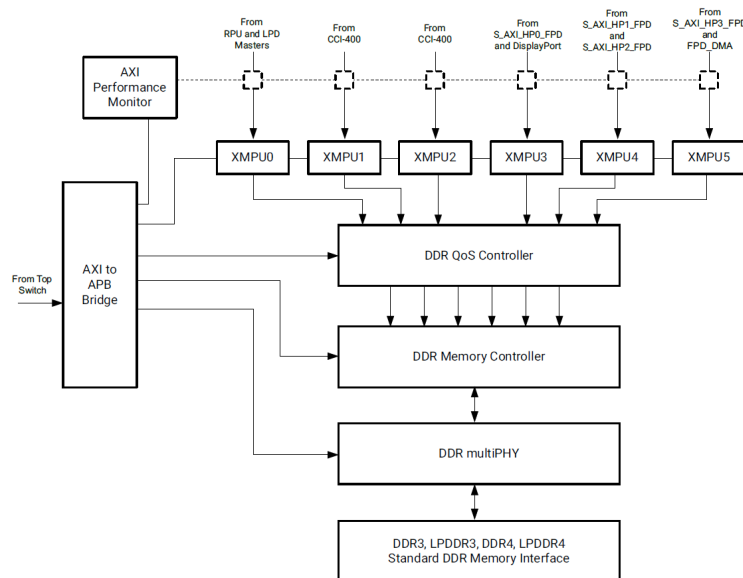

Figure 16 DDR Subsystem Block Diagram

There are dedicated chapters in the TRM or whole separate TRM's for certain memory connection ports. Each of the blocks above had sections with the TRM to discuss the setup of each block. We will not cover the Xilinx Memory Protection Unit (XMPU) or the DDR QoS Controllers. We will only cover some of the DDR Memory Controller and the DDR multiPHY as well as the external DDR DRAM portion of the design. The DDR I/O pins are located on bank 504 and can have a 16-bit, 32-bit or 64-bit data path to the DRAMs depending on the device type. There are eight pages of registers for the DDRPHY and three pages of registers for the DDR Controller. Some of the register setup will be done in the Vivado tool chain for each of these embedded components. By following the Xilinx methodology, the code is embedded in the psu_init.c, must be compiled, and placed in the First Stage Boot Loader (FSBL). Afterwards, program into the QSPI or the SD card depending on the boot configuration of the design. The Avent target has boot switches that allow the user to configure the boot location. This boot switch may or may not be implemented on your design. We have only scratched the surface (part of the DDR and DDRPHY controller) of what is required to configure the hardware for

manufacturing test. There is also the actual software to conduct the testing that should include address, data, noise, byte, word, burst and other. Moreover, we need to consider if there is a method of testing without booting the system to test DDR memories. It becomes a chicken-and-egg problem where you need RAM to execute the test software and the RAM has not been verified. As we can see, there are days of work (or more depending on experience level with the devices chosen) to develop functional test software for DDR test. We realized that this SoC is sophisticated and maybe beyond your need, but when evaluating replacement parts for your design, all the items covered in this eBook can be considered with a good DFT methodology.

Conclusion

It is vital that the tools you have for board test are robust and flexible to handle the ever-changing landscape in test to maintain your product leadership position.

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Avnet UltraZed-CG IO Carrier Card technical documents:
https://www.avnet.com/opasdata/d120001/medias/docus/178/UltraZed-IOCC-UG-V1.pdf

Xilinx Zynq UltraScale+ Device TRM https://docs.xilinx.com/v/u/en-US/ug1085-zynq-ultrascale-trm

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