

## **SourcePoint Home**

# **Getting Started Guide for the**

## AAEON UP Xtreme i11

## **Support for v0000 and v0001 boards**

**Revision 2.00** 



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### Introduction

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## Revision History

<b>Revision Number</b>	Description	Date
1.00	Original document, describes v0000	November 28, 2021
	board support	
2.00	Added content for new support of v0001	May 30, 2022
	(with the Type-C connector removed)	
	AAEON UP Xtreme i11 board	





#### Welcome!

Thank you very much for your SourcePoint Intel Individual or Institutional License purchase! We appreciate you acquiring our best-in-class debugger, and hope you enjoy using it. We strive to deliver the most powerful, easy-to-use and polished product as possible. So, please feel free to share your feedback directly at our contact information above, or via your favorite social media outlet.

As with any new tool, mastering SourcePoint takes an investment in terms of time and effort. JTAG-based debug is a fairly specialized area, and low-level "on the metal" firmware development on x86 platforms is even more so. So, in your use of the tool, you may encounter behavior that seems non-intuitive or even wrong. You may be encountering a tool corner case, a limitation inherent in JTAG or DCI, or even a bug. If so, try a few different options as may be referenced in the <u>Troubleshooting</u> section of this Guide, and if it persists, give us a call. We are here to serve.



## Which Board and Cables to Purchase?

The board supported by your SourcePoint Individual or Institutional license is the AAEON UP Xtreme i11 board, based upon the Intel Tiger Lake CPU. As of February 2022, to address part availability issues, AAEON redesigned the v0000 boards to remove the on-board 40-pin GPIO Bus header, Intel FPGA Altera Max V, and the USB Type-C port. The new v0001 boards support DCI in a similar way as the original v0000 boards, but via the Type-A USB3.0 ports.

The new v0001 boards come in four flavors: Celeron, i3, i5 and i7. As of this writing, only the i3, i5 and i7 have been tested and are supported by your license. The Celeron version of the board has not been tested; it may work, but we recommend the i3, i5 or i7 to get the most value out of your purchase. These are Tiger Lake (TGL) UP3 CPUs that supports all the latest Intel debug and trace features such as Intel Processor Trace (Intel PT), Intel Trace Hub (ITH), Architectural Event Trace (AET), and others.



#### WARNING:

Do <u>NOT</u> plug a regular USB cable into the target and attempt to use DCI. Specialty cables, with VBUS snipped, are required; using a regular USB cable may possibly fry your target, or worse.



For the older v0000 boards, the only source to purchase the DCI Type-A/C cable is <u>www.designintools.intel.com</u>. Accessing this site requires a confidential NDA with Intel. This target has its Type-C port enabled for DCI. If you have a debug host with a Type-A port, purchase the part # ITPDCIAMCM1MU (1.0 meter) cable. The longer 1.8-meter ITPDCIAMCM2MU will work as well. If your host has a Type-C port, purchase the ITPDCIC2CD2U1M. Using Type-A/C hubs have been seen to work, but are not warranted. Type A/C adapters have been seen not to work.

For the v0001 boards, purchase the DCI Type-A/A cable. The good news is that, in addition to <u>www.designintools.intel.com</u>, these cables can be purchased from DataPro: <u>https://www.datapro.net/products/usb-3-0-super-speed-a-a-debugging-cable.html</u>.



### **BIOS Settings**

The AAEON UP Xtreme i11 boards come equipped with an AMI Aptio BIOS that is based upon typical Intel Customer Reference Board (CRB) BIOS.

For the v0001 board, if there is a need to retrieve the BIOS and re-flash the board, it can be obtained here: <u>https://downloads.up-community.org/download/up-xtreme-i11-0001-version-uefi-bios-v1-0/</u>.

Luckily, the platform comes with all the necessary hardware hooks and firmware straps to support Intel Direct Connect Interface (DCI) out of the box.

For the v0000 board, the USB Type C port on the board is the port of interest:



For the v0001 board, the Type-A/A cable can be plugged into any of the three USB3.0 ports (the blue jacks) available. All three jacks support DCI. The USB2.0 port (the black one) does not support DCI.

There is only one BIOS setting change that must be made for either the v0000 or v0001 boards: to disable the board's Watchdog Timer (WDT). Go into the BIOS Boot menu,

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and set WDT Timer -> Disabled. If you don't, run-control will be successful, but the board will power-cycle every 30 seconds; putting a real crimp in your debugging!

Main Advanced Chipset	Aptio Setup – AMI Security Boot Save & B	Exit
Boot Configuration Quiet Boot	[Fnabled]	Enables or disables Quiet Boot option
FIXED BOOT ORDER Prioria Boot Option #1 Boot Option #2 Boot Option #3	[USB Hard Disk] [USB CD/DVD] [USB Key:UEFI: General USB Flash Disk 1100, Partition	<pre>++: Select Screen fl: Select Item Enter: Select</pre>
Boot Option #4 Boot Option #5 Boot Option #6 Boot Option #7 Boot Option #8	1] [USB Floppy] [USB Lan] [Hard Disk] [NVME] [CD/DVD]	+/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Versio	on 2.21.1278 Copyright (C) 2	021 AMI

And that's all that's needed. All the Debug Settings in the CRB Advanced menu can be safely ignored. You are now ready to test your connection, and then launch SourcePoint and begin debugging.



### DbCStatus.exe: Red is Bad, Green and Yellow are Good

Luckily, there is a convenient application in the SourcePoint install directory that will tell you that the DCI driver is successfully installed on your computer, and it is possible to make a connection between SourcePoint and the target.

Navigate to C:\Program Files (x86)\Arium\SourcePoint 7.12.XX (where XX is your current SourcePoint release), and launch the DbCStatus.exe. You should see the red ball, indicating that there is no connection:

DbC Connection Status	;	
Connection status:	No connection	
DCI driver version:	1.10.0.0	
		Close

For the v0000 board, ensure that the Type-C cable is firmly connected to both the host and target, power up the UP Xtreme i11. You should hear two beeps, and in a moment the ball should turn green:

DbC Connection Status		
Connection status:	USB 2.0	
DCI driver version:	1.10.0.0	
		Close

Let the platform boot to the UEFI shell. Congratulations! You have a working DCI connection. It's smooth sailing from here.

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For the v0001 board, the ball will be yellow, versus the green. This is due to a flash firmware strap setting, which changes the target behavior somewhat, as you'll see below; but otherwise does not affect debugging.

DbC Connection Status		
Connection status:	USB 3.1	
DCI driver version:	1.10.0.0	$\bigcirc$
		Close

Is the ball still red? Try cycling power on the target (don't just power cycle with the reset button; physically remove the power plug, then plug it back in again). Still red? See our <u>Troubleshooting</u> section.



## Getting Started with SourcePoint

When you launch SourcePoint for the first time, you will see the main screen, mostly grey:

ourcePoint			- Ø X
Edit View Processor Options Window Help	*****	L L L L Q	
p, F5:Go, Shift+F5:Stop, F8:Step Into, F10:Step Over, Shif	+F12:Reset	No power	

SourcePoint uses Projects (files with suffix .prj) as containers for your debugging session. You can create as many Projects as you want, with all your own preferences saved. Often, once you have the SourcePoint Project configured to your liking, you'll save it and use it repeatedly during your separate debugging sessions. Other users may wish to save a separate Project for each separate debugging session. That's really a matter of user preference and what you're debugging – it's your choice.

Now it's time to create the Project. Under File > Project... select New Project:



You'll be presented by the New Project Wizard (NPW). The emulator connection should be via DCI:





New Project Wizard: Welcome	×
Welcome to the New Project Wizard	
This wizard helps you:	
- Select or add an emulator connection.	
- Create a new project file.	
DCI, DCI ~ Add/Edit	
Select an emulator connection and click Next.	
< Back Next > Cancel	Help

After hitting Next, you'll be prompted for the Project Name, Location to store the Project, and the location of the Target Configuration file:



New Project Wiz	zard: Project File	×
Project file File name:		
Location: Target conf	C:\Users\alans\Documents\Arium\SourcePoint-IA_ Browse	
	Identify Target	
	< Back Next > Cancel Help	

Note that the Target Configuration (TC) files located in C:  $\My$ 

Documents\Arium\Targets are used in conjunction with the jtag-devices.xml file to define the specific silicon and SourcePoint settings necessary to ensure a successful DCI connection.

For the UP Xtreme i11 boards, custom TC files have been created, so you shouldn't do an Identify Target to automatically select the TC file of interest. Rather, manually select the specific TC file that is customized for this target (TGL\UP-Xtremei11\_DbC.tc) and hit Open:



🛞 Open			×	
← → • ↑ 🖡 « Sou	← → • ↑ 🖡 « SourcePoint-IA_7.12.20 » Targets » TGL » TGL-U • ひ 🖉 Search TGL-U			
Organize 🔹 New folder			•	
🦲 iCloud Drive 🖈 🔨	Name	Date modified	Туре	
Documents	TGL.tc	10/29/2021 4:15 AM	TC File	
lntel	TGL_DbC.tc	10/29/2021 4:15 AM	TC File	
Screenshots	UP-Xtreme-i11_DbC.tc	11/19/2021 2:10 AM	TC File	
SourcePoint-IA_ī				
😽 Dropbox				
OneDrive - Person				
🗢 This PC				
🗊 3D Objects				
Desktop				
🖆 Documents 🗸 🗸	<		>	
File nam	e: UP-Xtreme-i11_DbC.tc	<ul><li>Target Conf</li><li>Open</li></ul>	iguration Files (*.tc) V	

Then, your screen should look something like this:



New Project Wi	zard: Project File	×
Project file		
File name:	My Tiger Lake Project	
Location:	C:\Users\alans\Documents\Arium\SourcePoint-IA_ Browse	
Target conf	iguration file	
C:\Users\a	alans\Documents\Arium\SourcePoint-IA_7.12.15\Ta Browse	
	Identify Target	
	< Back Next > Cancel	Help

Hit Next, then Finish, and SourcePoint should successfully connect to the target. You should see "JtagTest: Successful operation" followed by "Configuration state: Connected" in the Status bar at the bottom left:





Now the fun part begins. Click on the buttons at the top to set up the Viewpoint, Code, Command, Registers and other windows to your own preference. Move the windows around and resize them to take best advantage of your available screen real estate. You can right-click in the title bar of each window to change its type and, for example, to dock the window to the bottom, right side, etc.



A sample layout is below:



🖀 SourcePoint v7.12.0 [DCI] - TigerLake - C:\Users\alans\D	ocuments\Arium\SourcePoint-IA_7.12.15\My Tiger Lake Project.prj (safe mode)				- 0	×
File Edit View Processor Options Code Window Help						
월 📽 🔛 😂 🔛 🚔 🔛 🚅	🆓 Load UEFI Macros 🎕 🍕 🥵 😁 🗶 🕒 🕩 🗊 🗊 👘 🌲 🍰 💿 Breakpoints 🕒 Code > Command 📓	log 🎹 Memory	<b>IP</b> Register	rs 🔍 Symbols 🧈 Trace I	● Viewpoint	Q. Watch
		<u>, , , , , , , , , , , , , , , , , , , </u>	2			Ý 💡
						-
Code (P0*) Tracking IP		00 Viewpoint				= 🔀
🕼 No Data Available - Processor not av	ailable	Name		Description		Status
			TigerLak		Running	
			TigerLak		Running	
			TigerLak		Running	
		° P3	TigerLak	(e	Running	
		<				>
		IP General Reg				
		■IA-32	Name	Value	0	
		Intel 64	RAX RBX	???????????????????????????????????????		
		General		???????????????????????????????????????		
		Floating	RDX	222222222222222222222222222222222222222		
		Segment	RBP	2222222222222222222		
	-	Control	RSI	222222222222222222222222222222222222222		
		Debug	RDI	???????????????????????????????????????		
Unknown V P Source V Go (	Cursor Set Break Track IP View IP Refresh	MMX	DSD	???????????????????????????????????????		
		YMM - SI	R8	222222222222222222222222222222222222222	?	
	🚥 Breakpoints 🗖 🗉 🔀	YMM - D	R9	???????????????????????????????????????	?	
	Identifier Address Attributes	YMM - In		???????????????????????????????????????		
	Address Address	■MSR	R11	???????????????????????????????????????		
		User	R12	???????????????????????????????????????		
			R13	???????????????????????????????????????		
			R14	222222222222222222222222222222222222222		
	Edit Add Remove Remove All Enable Disable All		R15 CS	222222222222222222222222222222222222222	<i>;</i>	
		-	DS	????		
E Log			SS	2222		_
Date Time Component	Message	1	ES	2222		
①11/16/2021 17:11:49.685 RefillDisplay	List Could not refill the display due to a lack of known code position	d l	FS	2222		
			GS	????		
			RIP	???????????????????????????????????????	?	
		< >	RFLAGS	???????????????????????????????????????	?	
			_		_	
Command						
Configuring Devices						^
Connecting						
	Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\aa\aaextend.mac					
PO>						
P0>						
1						~
F1:Help, F5:Go, Shift+F5:Stop, F8:Step Into, F10:Step Over	; Shift+F12:Reset	P0 1F: Ri	unning		Halt Mode	

**Power Tip**: the window layout can be saved as a separate file to your Project. That way, when you create a new Project, you can just Load the layout file separately, without having to create and move the windows around again. Choose File > Layout > Save Layout... to create a .lyt file, and then do a Load Layout... to save yourself time every time you create a new Project.

**Power Tip**: Exploring Options > Preferences... and some of the other menu items may give you some more labor-saving ideas. For instance, I like to ensure that both Load last project on startup and Save project on exit are disabled. This gives me more control on entry and exit from the application:



Preference	s								×
General	Emulator	Breakpoints	Code	Memory	Program	IPC	Colors		
Project	t								
Lo	ad last pro	ject on startup	þ						
⊡ Pr	ompt befor	e automaticall	y saving	project					
Sa	ive project	on exit							
	ad target c	onfiguration fi	le when	project loa	aded				
Fi	le name:	C:\Users\alar	is\Docun	nents\Ariur	m\SourcePo	oint-IA_7	.12.1	Browse	
- User ir	nterface								
		ed configurati	on settir	nas	Proform	ed editor:	notepa	he	$\sim$
	now tooltips	-	on ooten	.go	Fleielle	eu euitor.	посере		
	-								
	med windo								
.nt	erval: 10	second	S						
					ОК		Cancel	Hel	р

This is a good point to do a Project > Save Project... That way, you don't have to start all over, if for some reason your project gets messed up.

At this point, you are ready to fully begin your debug session. Many of the operations can be accessed via the toolbar at the top of the screen. You can issue a Stop on the target, Step Into, Reset it and halt at the reset vector, set some breakpoints, Go to the breakpoint, and so on.



000000064002218L CHECA PE 000000064002218L CHE102 PE 000000064002218L CHE102 PE 000000064002215L 3C02 CE 0000000640022025L 45888000000 PE 0000000640022025L 458880000000 PE 0000000640022025L FE 000000064002203L PE 000000064002203L PE 00000006400204EL PE 00000006400204EL PE 00000006400204EL PE 00000006400204EL PE 00000006400204EL PE 00000006400204EL PE 00000006400204EL PE 00000006400204EL PE 000000006400204EL PE 00000006400204EL PE 000000006400204EL PE 000000000000000000000000000000000000	MOV         RAX, f           MOV         RAX, f           SAL         ECX, f           MAU         ECX, f           MOV         RAX, f           JMP         00000           MOV         AL, D1           JMP         00000           MOV         RAX, f           JAP         00000           MOV         RAX, f           JE         short	WORD PTR [RCX] [RAX] 000640d201eL WORD PTR [R8]+000006 ptr 000000664d2038 WORD PTR [RCX] [RAX] 000640d201eL DX TE PTR [RCX] [RAX] 000640d201eL WORD PTR [RCX]+00001 AX	c0 aL		Viewpoint     Name     P0     P1     P2     P3     Viewpoint     P2     P3     Viewpoint     P1     P1	TigerLak TigerLak TigerLak TigerLak Mame RAX RBX	e e Value 000000000000000000000000000000000000	Stopped Stopped Stopped	State
0000000064072015L 85880C000000 M 00000006407215L 85CA M 00000006407215L 85CA M 00000006407215L 8580401 M 00000006407215L 8580401 M 000000064072025L 4588000000 M 000000064072025L 45880000000 M 000000064072025L 55C4000000 M 000000064072025L 8D0C12 M 000000064072025L 85C4000000 M 000000064072025L 55C4000000 M 000000064072025L 55C4000000 M 000000064072025L 55C4000000 M 000000064072025L 55C400000 M 0000000654072025L 55C400000 M 0000000654072025L 55C400000 M 000000054072025L 55C400000 M 000000054072025L 55C400000 M 00000005407205L 55C400000 M 00000005407205L 55C4000000 M 00000005500000000000 M 00000005407205L 55C4000000 M 00000005407205L 55C4000000 M 00000005407205L 55C500000 M 0000000550000000000000000000000	MOV         RAX, f           MOV         RAX, f           SAL         ECX, f           MAU         ECX, f           MOV         RAX, f           JMP         00000           MOV         AL, D1           JMP         00000           MOV         RAX, f           JAP         00000           MOV         RAX, f           JE         short	DX WORD PTR [RCX][RAX] 000640d20feL 000640d201 ptr 000000640d2032 WORD PTR [RCX][RAX] 000640d20feL DX TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+000001 AX	c0 aL		P0     P1     P2     P3      V     IP     General R     IA-32     Intel 64     General	TigerLak TigerLak TigerLak Mame RAX RBX	e e e Value 000000000000000000000000000000000000	Stopped Stopped Stopped	
000000064072018L C1E102 SE 000000064072018L 80401 SE 000000064072018L 80401 SE 000000064072023L 3C22 SE 000000064072023L 3C22 SE 000000064072025L 495880C000000 SE 000000064072025L 800C12 I 000000064072031L 0E77401 SE 000000064072031L SECA SE 000000064072031L SECA SE 000000064072031L SEA 000000064072031L SEA 000000064072031L SEA	MOV ECX, F SAL ECX, SAL MOV EAX, I MOV EAX, I MOV EAX, SAL JNE Short LEA ECX, I MOV RAX, C MOV EXX, F MOV AL, B MOV AL, B JAP 00000 MOV RAX, C SAL MOV RAX, SAL JE Short	DX WORD PTR [RCX][RAX] 000640d20feL 000640d201 ptr 000000640d2032 WORD PTR [RCX][RAX] 000640d20feL DX TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+000001 AX	c0 aL		P1     P2     P3     V     P3     V     IP General R     IA-32     Intel 64     General	TigerLak TigerLak TigerLak Agisters (PO*) Name RAX RBX	e e Value 000000000000000000000000000000000000	Stopped Stopped Stopped	• 8
00000000640D201EL 680401 P 000000640D201EL 690800000 S 000000640D201EL 690800000 P 000000640D2025L 498080000000 P 0000000640D202EL 750C G 0000000640D202EL 800C12 I 0000000640D203EL 80C12 R 0000000640D203EL 85C400000 G 000000640D203EL 85CA P 0000000640D203EL 8A0401 P 0000000640D203EL 8A0401 R 0000000640D203EL 8A00000 G 000000640D203EL 8A00000 G 0000000640D203EL 8A00000 G 0000000640D203EL 8A00000 G 0000000640D203EL 8A00000 G 0000000640D203EL 8A00000 G 0000000000000000000 G 0000000000	MOV EAX, 1 MP 00000 CMP AL, 00 MOV RAX, C MOV RAX, C MOV RAX, C MOV RAX, C MP 00000 MOV AL, B MOV AL, B MP 00000 MOV RAX, C SHOP 00000 MOV RAX, C SHOP 00000	WORD PTR [RCX][RAX] 000640d20feL wORD PTR [R8]+000000 ptr 00000640d203s WORD PTR [RCX][RAX] 000640d20feL DX TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+00001 AX	aL		P2 P3 P3  V IP General Re IA-32 Intel 64 General	TigerLak TigerLak egisters (PO*) Name RAX RBX	e e Value 000000000000000000000000000000000000	Stopped Stopped	= 2
00000000640D201EL         ESD8000000         2           0000000640D2023L         3C02         C           0000000640D2025L         49880C000000         P           0000000640D2025L         505700         P           0000000640D2025L         5057001         P           0000000640D203LL         67970401         P           0000000640D203LL         558700000         J           0000000640D203LL         58CA         P           0000000640D203LL         58A00000         J           0000000640D203LL         48A00000         J           0000000640D203LL         488500000         J           0000000640D204L         488514001000         P           0000000640D204ZL         48850         J           0000000640D204ZL         74A5         J	JMP         0000           CMP         AL,02           MOV         RAX,0           MOV         RAX,0           JNE         short           LEA         ECX,1           MOVZX         EAX,0           MOV         ECX,1           MOV         ECX,1           MOV         ECX,1           JMP         00000           MOV         ECX,1           JMP         00000           MOV         RAX,1           JE         short	000640d20feL WORD PTR [R8]+0000006 ptr 000000640d203 WORD PTR [RNX] [RNX] 000640d20feL IX TE PTR [RCX] [RAX] 000640d20feL WORD PTR [RCX] +00001 AX	aL		P3	TigerLak egisters (PO*) Name RAX RBX	e Value 000000000000000000000000000000000000	Stopped	
000000064012/231, 3002 C 000000064012/251, 498800000000 C 00000064012/251, 498800000000 D 00000064012/231L 0FD70401 P 000000064012/231L 0FD70401 P 000000064012/241L 400000 T 000000064012/241L 400000 T 000000064012/241L 40000 T 000000064012/241L 40000 T 000000064012/241L 40000 T 000000064012/241L 400000 T 0000000064012/241L 400000 T 00000000000000000000000000000	CMP         AL, D'S           MOV         RAX, C           MOV         RAX, C           JNE         short           LEA         ECX, I           MOVZX         EAX, F           JMP         00000           MOV         ECX, I, J           JMP         00000           MOV         ECX, I, J           JMP         00000           MOV         RAX, S           JJMP         00000           MOV         RAX, S           JE         short	WORD PTR [R8]+000000 ptr 000000640d2033 WORD PTR [RCX][RAX] 000640d20feL DX TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+000001 AX	aL		IP General Re IA-32 Intel 64 General	egisters (PO*) Name RAX RBX	Value 000000000000000000000000000000000000	00	
0000000640122025L 498880C000000 P 000000064012202CL 750C J 000000064012202L 8D0C12 J 000000064012203L 0E70401 P 000000064012203L ESC400000 J 000000064012203L 8A0401 P 000000064012203L 8A0401 P 000000064012203FL 858A00000 J 000000064012204L 4888514001000 P 000000064012204BL 4885C0 7 000000064012204BL 485C0 J	MOV         RAX           JNE         short           LEA         ECX,I           MOVZX         EAX,V           JMP         00000           MOV         ECX,F           MOV         ECX,I           JMP         00000           MOV         RAX,C           TEST         RAX,F           JE         short	WORD PTR [R8]+000000; ptr 00000064042033; WORD PTR [RDX][RDX] OND PTR [RCX][RAX] 000640d20feL DX TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+000001 AX	aL		IP General Re IA-32 Intel 64 General	Name RAX RBX	Value 000000000000000000000000000000000000	00	
000000064012022L 750C 3 00000064012022EL 8D0C12 I 000000064012035L ESC4000000 3 0000000064012035L ESC4000000 3 00000006401203AL 8BCA P 00000006401203FL ESA400000 3 00000006401203FL ESA400000 3 000000064012048L 488514001000 P 000000064012048L 48850 7 000000064012048L 4850 3	JNE short LEA ECX,I MOVZX EAX,Y MOVZ ECX,F MOV ECX,F MOV CCX,F MOV AL,BJ JMP 00000 MOV RAX,G TEST RAX,F JE short	ptr 000000640d203: WORD PTR [RDX][RDX] ORD PTR [RCX][RAX] 000640d20feL DX TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+000001 AX	aL		IP General Re IA-32 Intel 64 General	Name RAX RBX	Value 000000000000000000000000000000000000	00	
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00000006402031L 0FB70401 M 000000064012035L 8564000000 J 00000064012035L 856400000 J 000000064012035L 8A0401 M 000000006401203FL 89A8000000 J 00000006401203FL 4868814001000 M 000000064012048L 486850 J 000000064012048L 48550 J 0000000064012048L 48550 J 000000064012048L 48550 J 000000064012048L 48550 J 000000064012048L 48550 J 0000000064012048L 48550 J 000000064012048L 48550 J 000000000000000000000000000000000	MOVZX EAX, W JMP 00000 MOV ECX, F MOV AL, BJ JMP 00000 MOV RAX, C TEST RAX, F JE short	ORD PTR [RCX][RAX] 000640d20feL DX TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+000001 AX	140		■IA-32 ■Intel 64 General	Name RAX RBX	Value 000000000000000000000000000000000000	00	
00000006402203AL BBCA PR 0000000640D203CL BA0401 PR 0000000640D203FL S9BA000000 J 0000000640D204FL 486B814001000 PR 0000000640D204BL 485C0 T 0000000640D204BL 485C0 J	MOV ECX, F MOV AL, BY JMP 00000 MOV RAX, C TEST RAX, F JE short	DX TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+000001 AX	140		Intel 64 General	RAX RBX	000000000000000000000000000000000000000		
0000000640D203CL 8A0401 P 0000000640D203FL 85BA000000 J 0000000640D2045L 4888140010000 P 0000000640D2045L 4885C0 T 0000000640D2045L 74A5 J	MOV AL, BY JMP 00000 MOV RAX, C TEST RAX, F JE short	TE PTR [RCX][RAX] 000640d20feL WORD PTR [RCX]+00000] AX	140		General	RBX			
0000000640D203FL E9BA000000 J 0000000640D204L 488B5140010000 M 0000000640D204EL 4885C0 T 0000000640D204EL 74A5 J	JMP         00000           MOV         RAX,0           TEST         RAX,F           JE         short	000640d20feL WORD PTR [RCX]+00000] AX	L40		General				
0000000640D2044L 488B8140010000 M 000000640D204BL 4885C0 T 0000006640D204EL 74A5 J	MOV RAX, C TEST RAX, F JE short	WORD PTR [RCX]+000001 AX	140		Eleating		0000000606BF75		
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			51		Control	RBP	000000061DD699		
00000640D201EL V 🔎 Disassembly V Go		ptr 0000000640d1ff5			Debug	RSI RDI	0000000061CF214 0000000061DD699		
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					YMM - S	SF DO	00000000061DD699		
					YMM - D	DF DO	00000000061CF101		
	Sereakpo 💭				YMM - I		000000601D34203		
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						R14	0000000061CF214	4.4	
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Hit the Refresh button in the Code window after the first Stop. This is only necessary once; the Code window will automatically refresh with all run-control operations (stop, go, single-step, etc.) afterwards.

Refer to the <u>SourcePoint User Guide</u> in your install directory for detailed instructions on using all of the tool's features.

The v0000 board will halt automatically at the reset vector when you hit the SourcePoint Reset button:



🕒 Code (P0*): (16-bit) Tracking I	IP 00000000L - FFFFFFFI		
FFFFFFEBL 0000 FFFFFFEDL 0000	ADD	BYTE PTR [BX+SI], AL	^
FFFFFFEFL 00	ADD DB	BYTE PTR [BX+SI],AL 00	
FFFFFFF0L 90	NOP		
FFFFFFF1L 90	NOP		
FFFFFFF2L E923C0	JMP	nearl6 ptr ffffc018L	
FFFFFFF5L 0000	ADD	BYTE PTR [BX+SI],AL	
FFFFFFF7L 00FB	ADD	BL,BH	
FFFFFF9L 0000	ADD	BYTE PTR [BX+SI], AL	
FFFFFFFBL 0000 FFFFFFFDL 00FC	ADD ADD	BYTE PTR [BX+SI],AL	
FFFFFFFFL FF	DB	AH,BH ff	
			~
FFFFFFOL V	Disassembly 🗸 Go	io Cursor Set Break IP View IP Refresh	

This is desirable, because often you wish to start at early SEC or PEI to debug the portion of UEFI of interest.

But, the v0001 board has an incomplete implementation of DbC2, as you can see from the yellow ball reference earlier, so a couple of extra steps are needed to get there:

Firstly, after hitting the Reset button, an error message is thrown:



Hit OK, and then hit Go, to boot again to the UEFI shell (or as far as it will go before stopping autonomously). Then Stop and Refresh in the Code window if needed:



🍓 SourcePoint v7.12.0 [DCI] - TigerLake - C:\Users\ala	ins\Documents\A	rium\SourcePoint-IA_7.12.20\U	JP-Xtreme-i11_	DbC.prj								- 0 ×
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Code (P0*): (64-bit) Tracking IP 00000000000000000000000000000000000				- 0	×			Name		ription	Sta	
0000000063E22016L 8BCA 000000063E22018L C1E102	MOV SAL	ECX,EDX ECX,2			^		8	PO PO	TigerLake	npuon	Stopped	103
0000000063E22018L 8B0401	MOV	EAX, DWORD FTR [RC	X1 (RAX1					P1	TigerLake		Stopped	
-0000000063E2201EL E9DB000000	JMP	0000000063e220feL					C	7 P2	TigerLake		Stopped	
000000063E22023L 3C02	CMP	AL,02					C	P3	TigerLake		Stopped	
0000000063E22025L 498B80C0000000 000000063E2202CL 750C	MOV	RAX,QWORD PTR [R8 short ptr 0000000										
0000000063E2202EL 8D0C12	LEA	ECX, DWORD PTR [RD	X1 [RDX1									
000000063E22031L 0FB70401	MOVZX	EAX, WORD PTR [RCX	[RAX]									
000000063E22035L E9C4000000	JMP	0000000063e220feL						( -				
0000000063E2203AL 8BCA 0000000063E2203CL 8A0401	MOV MOV	ECX,EDX AL,BYTE PTR [RCX]	(DAV)						General Registers			- 0 X
0000000063E2203FL E9BA000000	JMP	0000000063e220feL							IA-32	Name	Value	
000000063E22044L 488B8140010000	VOM	RAX, QWORD PTR [RC		0				e e	Intel 64	RAX	000000000000000	000
000000063E2204BL 4885C0	TEST	RAX, RAX							General	RBX RCX	000000005D0A3 00000000000000	
0000000063E2204EL 74A5 000000063E22050L 458A8048010000	JE MOV	short ptr 0000000 R8B,BYTE PTR [R8]							Floating Point	RDX	000000000000000000000000000000000000000	
0000000063E22057L 41BA01000000	MOV	R10D,00000001	100000140						Segment	RBP	0000000061A5D	
000000063E2205DL 4438914A010000		BYTE PTR [RCX]+00	00014a,R10	В					Control	RSI	0000000061A5B	144
000000063E22064L 7579	JNE	short ptr 0000000							Debug	RDI	0000000061A5D	
0000000063E22066L 8A8968010000 000000063E2206CL 80F904	MOV	CL, BYTE PTR [RCX] CL, 04	+00000168						-MMX	RSP	000000005D0A3	
0000000063E2206EL 80F904	JNE	short ptr 0000000	063e220981						YMM - SP YMM - DP	R8	000000061A5D	
0000000063E22071L 66C1E202	SAL	DX,2								R9 R10	0000000061A5A 0000006001302	
000000063E22075L 488D4C2458	LEA	RCX, QWORD PTR [RS								R10 R11	00000000001302 0000000005D0A3	
000000063E2207AL 48894C2428	MOV	QWORD PTR [RSP]+2	8,RCX							R12	000000000000000000000000000000000000000	
0000000063E2207FL 488BC8 0000000063E22082L 440FB7CA	MOV MOVZX	RCX, RAX R9D, DX								R13	00000000000000	
0000000063E22086L 418D5201	LEA	EDX, DWORD PTR [R1	01+01							R14	0000000061A5B	
0000000063E2208AL 4C89542420	MOV	QWORD PTR [RSP]+2	0,R10							R15	0000000061A5D	598
000000063E2208FL FF5010	CALL	QWORD PTR [RAX]+1								CS	0038	
0000000063E22092L 8A442458 000000063E22096L EB66	MOV JMP	AL, BYTE PTR [RSP] short ptr 0000000	+58 063e220fet		~					DS	0030	
										SS ES	0030	
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📓 Log										RIP	000000063E22	01E
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Click on the Breakpoints button, and then set an Init breakpoint:

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FFFFFFF1L 90	NOP			_				0 P3				
FFFFFFF2L E923C0 FFFFFFF5L 0000	JMP nea	arl6 ptr ffffc018L										
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Hit Go.

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mmand ading Command Language Extensions: Ci\Users\alans\Documents\Arium\SourcePoint-IA_7.12.20\Macros\aa\aaextend.mac > > S > > > > > > > > > > > > > > >										~
ading Command Language Extensions: Cr\Users\alans\Documents\Arium\SourcePoint-IA_7.12.20\Macros\aa\aaextend.mac > ading User Defined Macro #0: Cr\Users\alans\Documents\Arium\SourcePoint-IA_7.12.20\Macros\EFT\EFI.mac >										
o ading User Defined Macro #0: C:\Users\alans\Documents\Arium\SourceFoint-IA_7.12.20\Macros\EFI\EFI.mac >										
> ading User Defined Macro #0: C:\Users\alans\Documents\Arium\SourceFoint-IA_7.12.20\Macros\EFI\EFI.mac > >		tensions: C:\Users\alans)	\Documents\Arium\SourceP	oint-IA_7.12.20\Macros\aa\	aaextend.mac					
ading User Defined Macro 40: C:\Users\alans\Documents\Arium\SourceFoint-IA_7.12.20\Macros\EFI\EFI.mac > >	0>									
	0> oading User Defined Macro	40: C:\Users\alans\Doouw	ents\&rium\SourcePoint-T	A 7.12.20\Macros\EET\EET	a					
	0>	eo. c. (osers (alans (bocum	ence (ALLina (SourcePoint-1							
relp. FSGa, Shift+FSStop, F&Step Into, F10Step Over, Shift+F12Arest PO 18: Stopped Special										
velp. F5Ga, Shift+F5Stop, F8Step Into, F10Step Over, Shift+F12Beset Process										
elp, FSGo, Shilt+F5Stop, F8Step Into, F10Step Over, Shilt+F12Reset P0 18: Stooped Special										
elp, Fs.Go, Shift+F5.Stop, F&Step Into, F10.Step Over, Shift+F12:Reset P0 18: Stopped Special										~
	Help, F5:Go, Shift+F5:Stop, F8:Step In	to, F10:Step Over, Shift+F12:Reset					PO	18: Stopped	Spe	ecial

Hit the Reset button again, and wait 20 seconds. Voila! You're at the reset vector:

Note that for the v0001 board, hitting Go will not necessarily take you all the way up to the UEFI shell; rather, it will break (Stop) for an Unknown Reason autonomously somewhere in DXE, often right after the splash screen display.

000000063C5CA03L CC	INT	Г 3	
000000063C5CA04L 8B	0596090000 MOV	/ EAX, DWORD	PTR [000000063c5d3a0]
000000063C5CA0AL 850	CO TES	ST EAX,EAX	
000000063C5CA0CL 75	OB JNE	E short ptr	000000063c5ca19L
000000063C5CA0EL B8	0000D0FE MOV	/ EAX,fed00	000
000000063C5CA13L 89		/ DWORD PTR	[000000063c5d3a0],EAX
000000063C5CA19L 48	05F0000000 ADI	RAX,00000	0f0
000000063C5CA1FL 44		/ R8D,DWORD	PTR [RAX]
000000063C5CA22L 3B			
000000063C5CA24L 73			000000063c5ca35L
000000063C5CA26L 41			
000000063C5CA29L 77			000000063c5ca2eL
000000063C5CA2BL B0			
000000063C5CA2DL C3			
000000063C5CA2EL 44		/	
000000063C5CA31L 72		short ptr	000000063c5ca2bL
000000063C5CA33L 3B			
000000063C5CA35L 76			000000063c5ca41L
000000063C5CA37L 44		/	
000000063C5CA3AL 73			000000063c5ca41L
000000063C5CA3CL 44		/	
000000063C5CA3FL 77			000000063c5ca2bL
000000063C5CA41L 3B			
000000063C5CA43L 0F			
000000063C5CA46L C3			
000000063C5CA47L CC			
000000063C5CA48L 40			
000000063C5CA4AL 48			020
000000063C5CA4EL 33		,	
000000063C5CA50L 8B			PTR [000000063c5d3a4]
000000063C5CA56L 830	C048 ADI	EAX,00000	048

This is a "feature" of either the different DbC2 implementation, or the fact that this BIOS is resetting the XHCI controller – you'll hear the beep from the DbCStatus.exe application – it's still under investigation. But regardless, SourcePoint will retain control of the target, and you can continue debugging.

Congratulations, you have mastered SourcePoint's basic capabilities, and are using run-control. Many users are content to just use these basic operations, because run-control by itself is very powerful. However, if you wish to master the product and use some of its more advanced features, read on.



## Advanced Topics: Using Trace

Trace is by far one of the most useful debugging utilities for triaging the most difficult, hard-to-reproduce bugs. Fortunately, the Tiger Lake CPU is equipped with all the latest-and-greatest trace logic, and SourcePoint supports them all.

Let's look at a few of them, and how to configure their use in SourcePoint.

#### Intel Trace Hub: SVEN

Event tracing on the TGL platform is accomplished by the Intel Trace Hub (ITH). Fortunately, using DCI, events supported by the ITH can be streamed directly out of system reset. The one limitation that exists is that some events (like Port IN/OUT tracing) happen so frequently at some points of the boot process that they overwhelm the capacity of the USB 2.0 (DbC2) connection and event processing, and thus cause buffer overflows – but these should be rare as long as the events collected are relatively close to the debug point of interest.

System Visibility Event Nexus (SVEN) is a means by which, within the AMI BIOS, printf statements are output through the ITH, as opposed to the serial port. This speeds up the boot time, and reduces the likelihood of port latency contributing to the masking of bugs.

NOTE: SVEN is only supported within the BIOS for the v0000 board. For the v0001 board, finish setting up the ITH per the steps below, and then skip ahead to the section on <u>Architectural Event Trace</u>.

The first thing to do is to configure the ITH. Reset the target and halt at the reset vector, address FFFFFF0:



🛞 SourcePoint v7.12.0 [DCI] - TigerLake - C:\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\My Tiger Lake Project.prj (safe mode)				– Ø ×
File Edit View Processor Options Code Window Help				
😰 🎬 🚼 😭 📽 😹 😌 👘 👹 👹 👹 👹 👹 👹 👘 🖬 🕛 🗊 👘 👘 🚱 Breakpoints 🕒 Code 🕨 Command 🔛	og 🎟 Memory	TP Registers	Symbols	Niewpoint Q Watch
	log minimory	Li negisters 🔩	(symbols y made o	O Viewpoint - Watch
				8
Code (P0*): (16-bit) Tracking IP 00000000L - FFFFFFFL	● Viewpoint			- • ×
FFFFFEBL 0000 ADD BYTE PTR [BX+SI],AL	Name	Desc	cription	Status
FFFFFEDL 0000 ADD BYTE PTR [BX+SI],AL	* P0	TigerLake		Stopped
FFFFFEFL 00 DB 00				
C PFFFFFF0L 90 NOP				
FFFFFFIL 90 NOP				
FFFFFF2L         E923C0         JMP         near16         ptr         ffffc018L           FFFFFF5L         0000         ADD         BYTE         PTR         [BX+S1], AL				
FFFFFFJL 000B ADD BLB FR [BA+31],AL	<			>
FFFFFF91 0000 ADD BYTE PTR [BX+SI],AL				
FFFFFFBL 0000 ADD BYTE PTR [BX+SI], AL	General Re			
FFFFFFDL 00FC ADD AH,BH	■IA-32		lue	
FFFFFFFL FF DB ff	Intel 64		000000000000000	
	General		0000000000000000	
	-Floating I		00000000000000000000000000000000000000	
	Segment		000000000000000000000000000000000000000	
	Control		000000000000000000000000000000000000000	
	Debug			
FFFFFF0L V P Disassembly Go Cursor Set Break Track IP View IP Refresh	MMX	DCD 00		
	YMM - S	D9 00	000000000000000	
📅 Breakpoints 🕞 🗉 🔀	YMM - D	R9 00	000000000000000000000000000000000000000	
Identifier Address Attributes	YMM - In		000000000000000000000000000000000000000	
Identifier Address Address	■MSR		000000000000000000000000000000000000000	
	User		000000000000000	
			0000000000000000	
Edit Add Remove All Enable Disable All			000000000000000000000000000000000000000	
	-	DS 00		
E Log		SS 00		
Date Time Component Message	1	ES 00		
11/17/2021 15:20:08.130 tco.clearbars Cleared PCI Express Base		FS 00		
		GS 00	00	
		RIP 00	0000000000FFF0	
	< >	RFLAGS 00	00000000010002	
Command				
Scanning Devices				^
Configuring Devices				
Connecting				
Loading Command Language Extensions: C:\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\aa\aaextend.mac				
P0>				
2005 Loading Reset (after): C:\Users\alans\Documents\Arium\SourcePoint-IA 7.12.15\Macros\Intel\ADL TCO Timer Disable.mac				
Post (arter). C. (osers (arter).				
				~
Target Stopped: Target reset	P0 18: St	opped S	pecial H	lalt Mode

The next step is to load in the ITH macros. This is accomplished by File > Macro > Load Macros... and selecting C:\My Documents\Arium\SourcePoint-IA\_7.12.15\Macros\Intel\TraceHub.mac. Then, in the Command window, at the P0> prompt, type:

npkEnableForce("cpcie=1", "tsact=1")

**Power tip**: If you want to know more about what this macro can do, type npkEnableForce\_Help().

Now, it's time to set up the ITH, and let it know what you want to trace. Click on the Trace button in the toolbar at the top, click on the Configure... button, and then click on the Trace Hub tab:





	- 42 42 42 44 14 14 14 14 14 14 14 14 14 14 14 14	Breakpoints     Code	e 🔰 Command 🔛 Lo	og 🎹 Memor	y <b>IF</b> Registe	rs 👒 Symbols 🕐 Trace e	Viewpo	oint 🔍 Wate
■ 🕐 📽 🎜 🛆 📃	Trace Configur	ation		×				= 53
Cold Of (TORIG) Hading & COCCOL CHAPTER         Preference         Prefer	(+SI], AL Masters to		PT Intel PT Memory	ne	TigerLak TigerLak TigerLak TigerLak		Stopped Not Act Not Act	
FFFFFFF5L 0000 FFFFFFF5L 0000 FFFFFFF5L 0000 FFFFFFF5L 0000 FFFFFFF5L 0000	INSTRUCTION	Example: 8, 32-255		ral R	egisters (P0*)	Value		
FFFFFFFL FF	Trace Hu Intel PT: AET: System me @ Use BI O Use So	b: System memory System Memory Trace Hub mory trace buffer DS settings urcePoint settings		1 -	F RCX RDX RBP RSI RDI RDI RSP R8 R9 R10 R11 R12 R13		) - - ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) )	
Log	Length:	~			R14	000000000000000000000000000000000000000		• ×
Date         Time         Component         M           11/17/2021         15:48:607.673         npk.checkenabled         T           11/17/2021         15:48:07.673         npk.checkenabled         T           11/17/2021         15:48:07.673         npk.checkenabled         T           11/17/2021         15:48:07.673         npk.checkenabled         T           11/17/2021         15:48:07.655         npk.setbase         M           11/17/2021         15:48:08.004         npk.setbase         F           11/17/2021         15:48:09.733         npk.setbase         F           11/17/2021         15:48:09.829         npk.setbase         F           11/17/2021         15:48:09.829         npk.setbase         F	lessage race Hub Device Now Er CH Trace Hub PCI Conf. TB BAR not configured W_BAR not configured		cy: CTC 16	5e]				
ommand tsact=0/1 -> Enable Time Stamp cpcie=0/1 -> Clear PCI Express log=07 -> Set the Logging L	MMIO Base after conf	ОК	Cancel H	elp				

If they're not already set, go to the bottom and click select the C:\MyDocuments\Arium\SourcePoint-

IA 7.12.15\Targets\TGL\TraceHub\TGL Ports.xml file to define the Master / Channel definitions. Click OK, and then go back in again, click on List under Masters to trace and select the ellipses (...) to look at the choices available:

SourcePoint v7.12.0 [DCI] - TigerLake - C:\Users\alans\Doc	uments\Arium\SourcePoint-IA	_7.12.15\My Tiger Lake Project.prj	(safe mode)					- 0 ×
File Edit View Processor Options Trace Window Help	🖁 Load UEFI Macros 🍓 🍓 4	2 8 K G G Q Q = :	🖁 🚭 Breakpoints 🕒 C	Code 🕻 Command 📓	Log 🎹 Memory	IP Registers 🔍 Sy	mbols 🧨 Trace 🖲	OViewpoint Q Watch
								<b>S</b>
Code (P0*): (16-bit) Tracking IP 00000000L - FFFFFFFL		Trace Configuration		×	Name	Descrip	tion	Status
FFFFFEBL 0000 ADD FFFFFFEDL 0000 ADD	BYTE PTR [BX+SI],A BYTE PTR [BX+SI],A					TigerLake		Stopped
FFFFFFEFL 00 DB	00	LBR BTS Trace Hub AET	Intel PT Intel PT Memo	ory		TigerLake		Not Active
FFFFFF0L 90 NOP		Masters to trace		_				
FFFFFF2L E923C0	near16 ntr ffffc01	○ None			• P3			
FFFFFF5L 0000 FFFFFF7L 00FB				Masters to Trace		~		>
FFFFFFF9L 0000 STATE Pn ADDR	INSTRUC			Masters to Trace		~		
FFFFFFFL 0000 FFFFFFFL 00FC	enabled	List: Example: 8, 32-25		20: UEFI:SVEN		^		
FFFFFFFL FF				21: 22:			00000000000000000	
		Trace routing		23:				
		Trace Hub: System memor	y ~	24: 25:			000000806C1	
		Intel PT: System Memor	v ~	26:			000000000000000000000000000000000000000	
				27: 28:			000000000000000000000000000000000000000	
FFFFFFOL		AET: Trace Hub	$\sim$	29:			000000000000000000000000000000000000000	
				2A:		~		
		System memory trace buffer			Clear All	Set All	00000000000000	
•		Use BIOS settings						
Disassem	nbly ~ Configure	O Use SourcePoint settings		Select the masters t	o enable for trace	e.	000000000000000000000000000000000000000	
		Base address: 00000000	0P				000000000000000000000000000000000000000	
Log		base aduress.			ОК	Cancel		
Date Time Component 11/17/2021 15:48:09.928 npk.enableforc	Message e.option Clear P	Length:	$\sim$					^
11/17/2021 15:54:10.724 processGlobalS				bbles sv	wapped"			
-		Timestamp		_				
		Alignment packets	Frequency: CTC 16	~				
				_				
		Master / Channel definitions						*
		Filename: It-IA_7.12.15\Targ	ets\TGL\TraceHub\TGL Port:					
Command	le Time Stamp Count							
	r PCI Express MMIO	04	Course 1					^
	the Logging Level f ride the default MTr	ОК	Cancel	Help				
	ride the default SW							
<pre>fwbar=BAR -&gt; Over P0&gt;npkEnableForce("cpcie=1", "tsact=1")</pre>	ride the default FW_	BASE with BAR						
PO>npkEnableForce("cpcle=1", "tsact=1") PO>								
Filler Free Shift Freins Filter Inte Free Com	Chiff - E12-Dt				00 (7 7		(-1 ) · · ·	lalt Mode
F1:Help, F5:Go, Shift+F5:Stop, F8:Step Into, F10:Step Over,	Shirt+F12:Reset				P0 18: S	topped Spec	iai H	alt Mode

For now, select 20: (UEFI:SVEN) and 48 (UEFI:SVEN). Also, under Trace Routing, select Trace Hub and set to DbC:



ce Configuration				×
BR BTS Trace	e Hub AET	Intel PT	Intel PT Mem	ory
Masters to trace				
○ None				
List: 20,48				
Trace routing				
Trace Hub: DbC		$\checkmark$		
Intel PT: Syst	em Memory	$\sim$		
AET: Trac	e Hub	$\sim$		
<ul> <li>Use BIOS settin</li> <li>Use SourcePoin</li> </ul>	t settings			
Base address:	00000000P			P
Length:		$\sim$		
Timestamp				
Alignment pack	ets Fre	equency: (	CTC 16	~
Master / Channel de	efinitions			
Filename: It-IA_7	12.15\Targets	\TGL\Trace	eHub\TGL Ports	•
	ОК	Са	ncel	Help



Hit OK.

Now, and this is very important, you need to calibrate the ITH. The Trace window should be right-clicked and set to Trace Hub - SW/FW Trace (if it isn't already). Click on the Calibrate button, and you should be rewarded with it being successfully detected:

															1
Code (PO'): (16-bit) Trackin FFFFFEBL 0000 FFFFFFED 000 FFFFFFFL 00 FFFFFFFL 90 FFFFFFFL 90 FFFFFFFL 0000 FFFFFFF1L 0000 FFFFFFFFL 0000	g IP 0000000L - FFFFFF ADD DB NOP .TMD .TMD .TMD STATE ADDR NO data availab)	BYTE PTR BYTE PTR 00 near16 r Trace	E [BX+SI],A E [BX+SI],A tr ffffc01 INSTRUCTIO	L 81.			3 • • ×	-		Niewpo     Nam     P0     P1     P2     P3     <      TPGcongr		Lake Lake Lake Lake		Stopped Not Act Not Act	
FFFFFFDL 00FC FFFFFFFFL FF	< -00000018 Dise	ssembly v Co	nfigure	Display	SourcePo		uccessfully de OK			-Segn -Contr -Debu -MMX -YMM -YMM	ral RBX ing F RCX Pol RSI Ig RDI - SF R8 - DF R8 - Inf R10 R11 R12 R13		lue 000000000000000000000000000000000000	) - - ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) )	
Log											R14	00			
Date Time 11/17/2021 16:07:3 11/17/2021 16:07:3	Component 1.693 npk.enablei 1.796 npk.enablei	orce.option		nable Bit CI Expres											
ommand															
0>npkEnableForce("c 0> oading Reset (after	<pre>swbar=BAR -&gt; 0 fwbar=BAR -&gt; 0 pcie=1", "tsact=1 ): C:\Users\alans pcie=1", "tsact=1</pre>	Verride the ")	default FW	BASE wit	h BAR	acros\Int	≥1\ADL_TC	0_Timer	_Disable.ma						

**Power tip**: The Calibrate button only needs to be used once per project. The npkEnableForce("cpcei=1", "tsact=1") command must be re-issued after each reset.

NOTE: SVEN is only supported within the BIOS for the v0000 board. For the v0001 board, skip ahead to the section on <u>Architectural Event Trace</u>.

Then, hit the Go button in the top toolbar, and boot to the UEFI shell. Then hit Stop. You will see the SVEN printf data in all its glory:



STATE	ADDR	INSTRUCT	ION			
	UEFI:SVEN:C	CONSOLE				
	POSTCODE=	<00000060>				
-000000074		UEFI:	SVEN: CONSOLI	E="B"		
-000000064		UEFI:	SVEN: CONSOLI	E="b"		
-000000059		UEFI:	SVEN: CONSOLI	E="-%-0"		
-000000054		UEFI:	SVEN: CONSOLI	E=""		
-000000049		UEFI:	SVEN: CONSOLI	E=""		
-000000044		UEFI:	SVEN: CONSOLI	E=""		
-000000041		UEFI:	SVEN: CONSOLI	E="POST"		
-000000036		UEFI:	SVEN: CONSOLI	E="CODE"		
-000000031		UEFI:	SVEN: CONSOLI	E="=<00"		
-000000026		UEFI:	SVEN: CONSOLI	E="0000"		
-000000021		UEFI:	SVEN: CONSOLI	E="60>-"		
-000000016		UEFI:	SVEN: CONSOLI	E="-"		
٢						>
-000000074	Disassembly	<ul> <li>Configure</li> </ul>	Display	Filter	Calibrate	Refr

Actually, it looks better if you select the Display... button, and de-select Data lines:

Trace Display Settings	×
Disassembly	Source code
Object code Instruction lines	Source lines Every instruction
Symbols Data lines	Line numbers
Pseudo-ops 🛛 Label lines	Source code file information
Display case: Mixed $\lor$	Filename Function
Radix indicator: None ~	Path Offset
Instruction width: 50	Line numbers Every instruction
	Timestamp
	🗌 Delta 🛛 Accumulate
	Time align with other views
Colors	OK Cancel





🛃 Trace Hub - SW/FW Trace	
STATE ADDR INSTRUCTION	TIMESTAMP
POSTCODE=<00000B41>	
-000001033 UEFI:SVEN:CONSOLE	-3.271 sec
POSTCODE=<00000B42>	
-000000973 UEFI:SVEN:CONSOLE	-3.220 sec
POSTCODE=<00000B47>	2,000
-00000912 UEFI:SVEN:CONSOLE POSTCODE=<00000C80>	-3.202 sec
-00000852 UEFISVEN:CONSOLE	-3.107 sec
POSTCODE=<00000C81>	3.107 Sec
-000000792 UFT:SVEN:CONSOLE	-3.107 sec
POSTCODE=<00000C82>	0.107 500
-000000732 UEFI:SVEN:CONSOLE	-3.106 sec
POSTCODE=<00000C83>	
-000000673 UEFI:SVEN:CONSOLE	-3.100 sec
POSTCODE=<00000A61>	
-000000613 UEFI:SVEN:CONSOLE	-3.100 sec
POSTCODE=<00000A63>	
-000000554 UEFI:SVEN:CONSOLE	-3.094 sec
POSTCODE=<00000A03>	2 004 555
-000000494 UEFI:SVEN:CONSOLE	-3.094 sec
POSTCODE=<00000A65> -000000435 UEFI:SVEN:CONSOLE	-3.093 sec
POSTCODE=<00000A64>	5.055 Sec
-000000375 UEFI:SVEN:CONSOLE	-3.092 sec
POSTCODE=<00000B0F>	0.002 500
-00000315 UEFI:SVEN:CONSOLE	-3.061 sec
POSTCODE=<00000C6A>	
-000000255 UEFI:SVEN:CONSOLE	-3.059 sec
POSTCODE=<00000C71>	
-000000195 UEFI:SVEN:CONSOLE	-3.057 sec
POSTCODE=<00000C7F>	
	-622.562 ms
POSTCODE=<0000004F>	10
-00000074 UEFI:SVEN:CONSOLE	+0 ns 🗸
-000000375 Disassembly V Configure Display Filter Calibrate Refresh	

This BIOS is not particularly verbose, so all we see here are the POST codes. But, you get the idea.

#### Architectural Event Trace

Click on the Trace button in the top toolbar, and select Configure... again. Within the Trace Hub tab, add '18' to the list of Masters to trace.



asters to trace   None   All   List: 18,20,48   Trace routing   Trace Hub:   DbC   Intel PT:   System Memory   AET:   Trace Hub   vstem memory trace buffer   Use BIOS settings   Use SourcePoint settings   Base address:	ce Configuration				×
<ul> <li>None</li> <li>All</li> <li>List: 18,20,48</li> <li>Trace routing</li> <li>Trace Hub: DbC</li> <li>Intel PT: System Memory</li> <li>AET: Trace Hub</li> <li>AET: Trace Hub</li> <li>vstem memory trace buffer</li> <li>Use BIOS settings</li> <li>Use SourcePoint settings</li> <li>Base address: 0000000P</li> </ul>	BR BTS Trace	Hub AET	Intel PT	Intel PT Mem	ory
All List: 18,20,48 Trace routing Trace Hub: DbC Intel PT: System Memory AET: Trace Hub AET: Trace Hub AET: O0000000P	Masters to trace				
<ul> <li>List: 18,20,48</li> <li>Trace routing</li> <li>Trace Hub: DbC </li> <li>Intel PT: System Memory</li> <li>AET: Trace Hub</li> <li>AET: Trace Hub</li> <li>vstem memory trace buffer</li> <li>Use BIOS settings</li> <li>Use SourcePoint settings</li> <li>Base address: 0000000P</li> </ul>	○ None				
race routing Trace Hub: DbC Intel PT: System Memory AET: Trace Hub Vstem memory trace buffer Use BIOS settings Use SourcePoint settings Base address: 0000000P					
Trace Hub: DbC Intel PT: System Memory AET: Trace Hub vstem memory trace buffer Use BIOS settings Use SourcePoint settings Base address: 0000000P	List: 18,20,48				
Intel PT: System Memory ~ AET: Trace Hub ~ vstem memory trace buffer Use BIOS settings Use SourcePoint settings Base address: 0000000P	Trace routing				
AET: Trace Hub  vstem memory trace buffer  Use BIOS settings  Use SourcePoint settings Base address: 00000000P	Trace Hub: DbC		$\sim$		
vstem memory trace buffer Use BIOS settings Use SourcePoint settings Base address: 00000000P	Intel PT: Syste	m Memory	$\sim$		
vstem memory trace buffer Use BIOS settings Use SourcePoint settings Base address: 00000000P	AET: Trac	Hub	$\sim$		
Use BIOS settings Use SourcePoint settings Base address: 00000000P					
Use SourcePoint settings Base address: 00000000P	System memory tra	e buffer			
Base address: 00000000P	Use BIOS settin	S			
	◯ Use SourcePoint	settings			
length: 8M ~	Base address:	00000000P			P
Longui.	Length:	3M	$\sim$		
mostamp	Timostomo				
<b>CTO</b> 4.6	Timestamp			TC 16	~
Alignment packets Frequency: CIC 16		<b>S</b> 176	equency:	01010	
aster / Channel definitions	Master / Channel de	initions			
			\TGL\Trace	eHub\TGL Port	
OK Cancel Help		OK	Ca	ncel	Help





Then click on the AET tab, select p0 as Processors to trace, and select RDMSR/WRMSR and Port In/Out as events to trace:



ce Configuration			$\times$
BR BTS Trace Hub Al	ET Intel PT	Intel PT Memory	
Processors to trace			
○ None			
List: p0			
(e.g., P0, P4-P7)			
Event sharing			
• Apply events to all proces	ssors		
Apply events to:	~~~		
O Apply events to:	V		
Event	Enabled	LBR	
HW/SW Interrupt			
IRET			
Exception			
RDMSR/WRMSR	Z		
Port In/Out			
Code breakpoint			
Data breakpoint			
BTM			
SMI/NMI/RSM			
MONITOR/MWAIT			
WBINVD			
SGX			
	Advanced	Clear all	
Ok	Cano		
UK	Cano	cel Helj	



Now, you can simply do a Go/Stop to capture the event trace data. Below shows the use the Command window to simulate a break on any read/write of, say, port x'CF8', the PCI CONFIG\_ADDRESS. This is conveniently done by issuing at the Command window P0> prompt:

go til cf8io

This will run the target until the next IN or OUT to CF8.

Event:         Port Out:         Port=0021, Data=000000FF           -000000586 P0         000000067EE16D1 OUT         DX, AL         -72.813 us	Stopped (hit Stopped (hit Stopped (hit Stopped (hit Stopped (hit
Abbde         Fin         ADDR         INSTRUCTION         TIMESTAMP           available         -         Event: Port Out: Port=0021, Data=000000FF         -	Stopped (hit Stopped (hit Stopped (hit
Event: Port Out: Port=0021, Data=000000FF         -72.813 us           -000000568 P0         000000067EE16D1 OUT         DX,AL         -72.813 us           Event: Port Out: Port=00A1, Data=000000FF         -00000550 P0         000000067EE16D7 OUT         DX,AL           -000000550 P0         000000067EE16D7 OUT         DX,AL         -66.406 us           Event: Port In: Port=1830         -000000514 P0         -66.276 us	Stopped (hit Stopped (hit
-000000586 P0 000000067EE16D1 OUT Dx,AL -72.813 us Event: Port Out: Port=00A1, Data=000000FF -000000550 P0 000000067EE16D7 OUT DX,AL -66.406 us Event: Port In: Port=130 -000000514 P0 000000067EE16DD IN EAX,DX -66.276 us	Stopped (hit
Event: Port Out: Port=00A1, Data=000000FF         -66.406 us           -000000550 P0         000000067EE16D7 OUT         DX,AL         -66.406 us           Event: Port In: Port=1830         -000000514 P0         0000000067EE16DD IN         EAX,DX         -66.276 us	
-000000550 P0 000000067EE16D7 OUT DX,AL -66.406 us Event: Port In: Port=1830 -000000514 P0 0000000067EE16DD IN EAX,DX -66.276 us	Stonned (his
Event: Port In: Port=1830 -000000514 P0 000000067EE16DD IN EAX,DX -66.276 us	wohher unt
-000000514 P0 000000067EE16DD IN EAX, DX -66.276 us	
-000000478 P0 000000067EE16DD IN EAX, DX -64.036 us	
Event: Port Out: Port=1830, Data=80002030	
-000000442 P0 000000067EE16E1 OUT DX,EAX -62.240 us 000008	
Event: Port In: Port=1830 000000	
-000000406 P0 000000067EE179B IN EAX,DX -51.406 us 000000	
Event: Port In: Port=1830, Data=80002033 000CF8	
-000000370 P0 000000067EE179B IN EAX, DX -48.281 us 0A3CC0	
Event: Port Out: Port=1830, Data=80002033	
Barton	
000000000 D0 000000007751700 TN FAX DV 043040	
E903000296 P0 000000006 FEI A0 IN EAA, DA EAA,	
-000000262 P0 000000067EE17A0 IN EAX,DX -44.115 us	
EAX, DX EAX, D	
-000000226 P0 000000067651784 001 DA,688 -42.316 US	
Evene, role out, role-over, baca-overout	
175 Disassembly V Event: Port Out: Port=00A1, Data=000000FF	-
-000000154 P0 000000067EE17E7 OUT DX, AL -17.161 us	
Event: Port Out: Port=0070, Data=000000B2	
Time -0.00000118 P0 0000000640CE1B6 OUT DX, AL -8.099 us	
a livenc. rore odc. rore-ooro, baca-ooooooo	
-494.731 IIS	
Event: Port Out: Port=0CF8, Data=80000008	
-000000046 P0 0000000640CE1E4 OUT DX, EAX +0 ns	
· ·	
-000000500 Disassembly V Configure Display Filter Calibrate Refresh	
2021 16:35:39.976 E Event: Port-001: Port=0076, Data=00000005 2021 16:35:49.222 F -000000082 P0 0000000640CE1CD OUT DX,AL Event: Port-01CF8, Data=0000008	

After issuing the command, you'll see something like this:

Scrolling up a little, you'll see a mix of Port In/Out and RDMSR/WRMSR. All timestamped, and with a STATE that can be used to correlate with other trace sources.

**Power tip**: The Last Branch Record (LBR) stack associated with each event can be captured as well. This is a very powerful debugging utility, especially when troubleshooting code execution leading up to events before system memory is initialized and Intel Processor Trace is available.



ce Configuration		×
BR BTS Trace Hub AE	T Intel PT Intel PT Me	mory
Processors to trace		
○ None		
Onone		
List: p0		
(e.g., P0, P4-P7)		
Event sharing		
_	sore	
Apply events to all proces	5015	
○ Apply events to:	$\sim$	
Event	Enabled LBR	
HW/SW Interrupt		
IRET		
Exception		
RDMSR/WRMSR		
Port In/Out		
Code breakpoint		
Data breakpoint		
BTM		
SMI/NMI/RSM		
MONITOR/MWAIT		
WBINVD		
SGX		
	Advanced Clear	all
ОК	Cancel	Help

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#### Intel Processor Trace

Intel PT is available only after system memory is initialized.

It's easy to set up. Click on the Trace button in the top toolbar, click the Configure... button, click on the Intel PT tab, put p0 in Processors to trace, and click on TSC and Cycle accurate under the Timestamp heading:

Trace Configuratio	n	×
LBR BTS	Trace Hub AET Intel PT Intel PT Memory	
Processors to	trace	
○ None		
List: p0		
Share filter / ti	mestamp settings	
	ngs to all processors	
◯ Apply setti	ngs to: P0 🗸	
Filters		
Range 1:	Enter symbol or start-end	
Range 2:	Enter symbol or start-end	
CPL:	User	
CR3:		
Timestamp		
TSC		
	Frequency: CTC 6	
MTC		
🗹 Cycle accu	rate Threshold: 0 (fine) ~	
	OK Cancel Help	

That's all. Then use the go til cf8io trick to capture some instruction trace data:



Trace Hub - SW/FW Trace TATE ADDR data available - Unable	Event Trace																	
	Event frace																her mentioned her her	Stat
	STATE	Pn	ADDR		INSTRU	JCTION								Т	IMESTAM	P A	Stopped	
				Por			- 10											_
	-000000658	PO	0000000	067	🛃 Intel Processor													×
			Event:		STATE Pn	ADDR			NSTRU								TIMESTAME	
	-000000622	PO	0000000		-00415 P0			0B14C2 M			K, RBX						-267.970 i	.S
	000000505	50	Event:		PO			0B14C5 M					Ob8],RDI					
	-000000586	50	0000000 Event:		P0 P0			0B14CC M				SP]+30 000020						
	-000000550	DO	00000000		PO			0B14D1 A		RD		100020						
	-00000000000000	FO	Event:		PO			0B14D5 P		KD								
	-000000514	PO			-00409 P0			OCD67D X		EC	K, ECX	i i					-267,969 1	s
			Event:		PO			OCD67F M			C. RAX							
	-000000478	PO	0000000	067	PO	0000	000064	OCD682 C	ALL	00	00000	0640ce0	20L					
			Event:		PO	0000	000064	OCE020 M	VOI	[R	SP]+0	8,RBX						
	-000000442	PO	0000000		P0			OCE025 M				0,RSI						
			Event:		PO			OCE02A P		RD								
	-000000406	P0	0000000		PO			OCE02B SI				00020						
			Event:		PO			OCEO2F L				0000006	40cd000]					
	-000000370	<b>P</b> 0	0000000		PO			OCE036 M			L,CL							
	-000000334	no	Event: 0000000		P0 P0			OCE039 TI OCE03B JI			, CL	0640ce1:	2.41					
	-000000334	PO	Event:		PO			OCE12D M					40ce338]					
	-000000298	PO	00000000		PO			OCE120 H			C, EBX		40062361					
	0000002.00	1.0	Event:		PO			OCE136 J				0640ce1	481.					
	-000000262	PO	0000000		PO			OCE148 TI			C, RAX		1.0.44					
0000375 Disassembly ~			Event:		PO			OCE14B J				0640ce1	38L					
	-000000226	PO	0000000	067	PO	0000	000064	OCE14D TI	EST	DI	L, DIL	,						
			Event:	Por	PO	0000	000064	OCE150 JI	NE	00	00000	0640ce2	11L					
e Time (	-000000190	P0	0000000		PO			OCE156 DI				00640ce						
17/2021 16:35:49.222 p			Event:		PO			OCE15C M					40ce3b8]					
17/2021 16:51:03.122 d	-000000154	<b>PO</b>	0000000		PO			OCE162 CI				00000a						
			Event:		PO			OCE165 JI				0640ce2						
	-000000118	P0	0000000 Event:		P0 P0			OCE16B M				X1 [RAX*:	40ce3b8]					- v
	2			FOI														-
	-000000586	Disas	sembly ~	Co	-00409	Disasse	mbly ~	Configure	e	Display		Filter	Calibrate	Re	efresh			
				_														_
ind																		
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There's a lot more that you can see and do with these Trace utilities. SourcePoint can use Intel PT to display a Call Chart and Call Tree. You can open up Code Tracking windows that update dynamically as you walk through the code, showing you exactly where you are and the interaction between code and events. When you have source and symbols available, the firmware flow becomes much more intuitive and visual. Indulge your curiosity and imagination.

The video at <u>https://www.asset-intertech.com/wp-content/uploads/2021/11/UP-Xtreme-i11-Getting-Started.mp4</u> shows some of these capabilities. The <u>SourcePoint User Guide</u> also provides a very thorough, comprehensive review of the tool. And visit our <u>SourcePoint Academy</u> for helpful "How To" content.



## Troubleshooting Tips

At some point, you'll run into something strange. We're the first to admit that JTAGbased run-control and trace are not always deterministic. JTAG is a 30-year hardware protocol, and when something goes astray at a very low level, SourcePoint tries to (but sometimes doesn't) recover gracefully. There will be times that the board will power cycle on its own. Or the firmware thinks that a thread is running but gets out of sync with the SourcePoint software, which thinks it's halted. Or the DbCStatus.exe ball stays red instead of turning green, while you swear you have a good DbC connection. Sometimes you have no choice but to quit SourcePoint and power cycle the target. That usually clears up the one-of's. But if the issue is repeatable, we ask that you collect as much information as you can, and open a ticket with us at <u>https://www.asset-</u> intertech.com/support/. We'll respond as soon as possible.

In the meantime, here are a few errata that we've noticed on the UP Xtreme i11, and the steps needed to mitigate.

#### Firmware gets out of sync with software

On the host PC using DCI, functionality is roughly partitioned between software (SourcePoint application with its GUI) and firmware (lower-level run-control primitives). Broad-brushing it, SourcePoint software on the host communicates with the firmware, that encapsulates JTAG traffic into packets which are sent to the PCH, which in turn performs the JTAG mastering function.

Somewhere along the line, the firmware may get out of sync with the software. You may see symptoms like:

In the Viewpoint window, the threads are shown as Running, whereas the Status Bar at the bottom right shows Stopped.

P0 in the Viewpoint window is Running, with one or more threads below it are in the Stopped state.

If this happens, you'll likely have to quit SourcePoint, kill the AssetDCI process (see below), power-cycle the target, then start over. Sorry. Then please enter <code>aalog = 20987</code> in the <code>Command</code> window, and try to reproduce. We're extremely interested in these cases, so capture the verbose logs in the <code>Log</code> window and send to us.

#### Trace buffer overflows

DCI traffic processing has its limitations. When you try to collect too much trace data, the trace buffer overflows, causing aberrant behavior.

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Although the trace data is highly compressed, some trace sources, in particular with AET, running through the Trace Hub can exceed the capacity of the USB 2.0 connection. In theory running at 480Mbps, in practicality SourcePoint can only process trace data at approximately 100Mbps. Beyond that, we collect ~ 20kB of trace data before a buffer in SourcePoint overflows, and we don't recovery gracefully.

NSTRUCTION TIMESTAMP GLOBAL=0249F00000 AET-18:C01=000000067EF94B1 AET-18:C01=0000180800EFD2C1 AET-18:C01=000000007EF94B1 AET-18:C01=000000007EF94B1 AET-18:C01=000000007EF94B1 AET-18:C01=00002067EF94B1 AET-18:C01=00002067EF94B1 AET-18:C01=000000007FF94B1 AET-18:C01=000000007FF94B1 AET-18:C01=000000007FF94B1 AET-18:C01=000001067EF94B1 AET-18:C01=000001067EF94B1	De Lake Lake Lake Lake Lake	scription Stopped Stopped Stopped Stopped	Statu
GLOBAL-0249F00000 ART-13:C01-000000067EF94B1 ART-13:C01-00004700047ADE ART-13:C01-00004500047ADE ART-13:C01-00000000067E994B1 ART-13:C01-0000000001808 ART-13:C01-0000000001808 ART-13:C01-00000000793015 ART-13:C01-00000067E94B1 ART-13:C01-00000067E94B1 ART-13:C01-00000067E794B1	A De Lake Lake Lake Lake	scription Stopped Stopped Stopped	
GLOBAL-0249F00000 ART-13:C01-000000067EF94B1 ART-13:C01-00004700047ADE ART-13:C01-00004500047ADE ART-13:C01-00000000067E994B1 ART-13:C01-0000000001808 ART-13:C01-0000000001808 ART-13:C01-00000000793015 ART-13:C01-00000067E94B1 ART-13:C01-00000067E94B1 ART-13:C01-00000067E794B1	De Lake Lake Lake Lake	Stopped Stopped Stopped	Statu
AET-18:c01-0000000006FEF94B1         AET-18:c01-0000108000FF2C1         AET-18:c01-0000006070201         AET-18:c01-0000000674F94B1         AET-18:c01-0000000674F94B1         AET-18:c01-0000000674F94B1         AET-18:c01-0000000674F94B1         AET-18:c01-0000000674F94B1         AET-18:c01-000000674F94B1         AET-18:c01-000000674F94B1         AET-18:c01-0000006793015         AET-18:c01-000000674F94B1         AET-18:c01-000000674F94B1         AET-18:c01-000000674F94B1         AET-18:c01-000000674F94B1	Lake Lake Lake	Stopped Stopped	
AET-18:C01-0000180800EFD2C1           AET-18:C01-00034500004FADE           AET-18:C01-000000007998021           AET-18:C01-00000000067898           AET-18:C01-0000000001808           AET-18:C01-00000228000004FADE           AET-18:C01-0000000798015           AET-18:C01-0000000678981           AET-18:C01-0000006798015           AET-18:C01-000000678981           AET-18:C01-000000678981           AET-18:C01-000000678981           AET-18:C01-000000678981           AET-18:C01-000000678981           AET-18:C01-00000060678981           AET-18:C01-00000066789481           AET-18:C01-00000066782           AET-18:C01-0000006782	Lake Lake	Stopped	
AET-18:C01-000345000004FADE           AET-18:C01-0000000C0A7998C21           AET-18:C01-00000000067EF94B1           AET-18:C01-00000000001808           AET-18:C01-00002500004FADE           AET-18:C01-0000000004FADE           AET-18:C01-0000000004FADE           AET-18:C01-0000000004FADE           AET-18:C01-0000000004FADE           AET-18:C01-0000000006F2F94B1           AET-18:C01-000000006F2F94B1           AET-18:C01-000000006F2F24C	Lake		
AET-13:c01-000000CA7998c21           AET-13:c01-0000000FEF84B1           AET-13:c01-0000000FEF84B1           AET-13:c01-000000FADE           AET-13:c01-000000FADE           AET-13:c01-000000FADE           AET-13:c01-000000FADE           AET-13:c01-000000FADE           AET-13:c01-000000FADE           AET-13:c01-000000FADE           AET-13:c01-000000FF294B1           AET-13:c01-000000FF202C	Lake		
AET-18:CO1-0000000067EF94B1 AET-18:CO1-0000C00000001808 AET-18:CO1-000025000004FADE AET-18:CO1-00000000C0A79A3015 AET-18:CO1-0000000067EF94B1 AET-18:CO1-0000180800EFJ2CC		Cooppon	
AET-18:C01=000325000004FADE AET-18:C01=000000CA79A3015 AET-18:C01=000000067EF9AB1 AET-18:C01=0000180800EFD2CC	(D0*)		
AET-18:C01-000000C0A79A3015 AET-18:C01-00000000067EF94B1 AET-18:C01-0000180800EFD2CC	(00*)		
AET-18:C01=000000067EF94B1 AET-18:C01=0000180800EFD2CC	(DO*)		
AET-18:C01=0000180800EFD2CC			
		/alue	
AET-18:C01=000345000004FADE		0000000FED000FF	
AET-18:C01=000000C0A79A3C49		00000005F0A4C60	
AET-18:C01=0000000067EF94B1		000000000000000	
GLOBAL=000000000000000000000000000000000000		0000000000000A1	
tiple masters ***		000000063A335D0	
GLOBAL=01		00000005F0A4C68	
GLOBAL=00000000000492 +333.522 se		00000005F0A4CA8	
AET-18:C01=000325000004FADE		00000005F0A4BE8	
AET-18:C01=000000C0A7A11E1F	0	0000000000000000	
AET-18:C01=000000067EF94B1		00000000000000E	
AET-18:C01=0000180800EFD31E AET-18:C01=000345000004FADE	0	000000000000000000000000000000000000000	
AET-18:C01=000047A12C09	0	00000005F0A4B80	
AET-18:C01=000000067EF94B1	0	000000000000000000000000000000000000000	
AET-18:C01=00000000001808	0	000000000000001	
AET-18:C01=000325000004FADE	0	000000063A308F0	
AET-18:C01=000020004FAEE			• 8
AET-18:C01=000000067EF94B1			
AET-18:C01=0000180800EFD324			
AET-18:C01=000345000004FADE			
	~		
rigure Display Filter Calibrate Refresh			
AET-18:C01=000000C0A7A1C3D           AET-18:C01=00000000067EF94B1           Figure         Display         Filter         Calibrate         Refresh		v	v

You'll see these symptoms of this occurrence in the SW/FW Trace window:

A few of these overflows are no big deal. But, if you're tracing a huge amount of data, SourcePoint may spin, as it tries to process all that data, and deal with the mess. Sometimes, after maybe a few minutes, it recovers. Sometimes, you end up in limbo.

The only solution at this point is to quit SourcePoint, do an End task on the AssetDCI Background process, power cycle the target, and start over:

💐 Task Ma	anager											×	
ile Option	ıs View												
Processes	Performance	App history	Startup	Users	Details	Service	es						
		,	^						3	1%	84%		
Name								Status		CPU	Memory		
🚔 Ad	lobe Collaborat	tion Synchron	izer 21.7 (	(32 bit)						0%	1.2 MB		
🚔 Ad	lobe Collaborat	tion Synchron	izer 21.7 (	(32 bit)						0%	1.1 MB		
🚔 Ad	lobe Collaborat	tion Synchron	izer 21.7 (	(32 bit)						0%	2.0 MB		ľ
🚔 Ad	obe Collaborat	tion Synchron	izer 21.7 (	(32 bit)						0%	2.2 MB		
> 🔳 Ad	lobe Genuine S	Software Integ	rity Servio	ce						0%	1.2 MB		
> 🔳 Ad	lobe Genuine S	Software Servi	ce							0%	1.7 MB		
💿 Ad	obe Installer									0%	0.9 MB		
🔄 Ad	lobe IPC Broke	r (32 bit)								0%	2.8 MB		
> 💿 Ad	lobe Update Se	ervice								0%	1.1 MB		
🔳 Ар	plication Fram	e Host								0%	8.3 MB		
🔳 ari	umlmd daemo	n								0%	1.4 MB		
🍇 As	setDCI (32 bit)									0%	51.5 MB		
💿 cc	Libraries									0%	0.1 MB		
💿 cc	XProcess									0%	0.1 MB		
۲												>	
	<sup>-</sup> details											End ta	> End task

Ultimately, we're working on improving the performing of the AssetDCI driver, and behaving more graciously when overflow is encountered. But, in the interim, it is key to ensure that the trace data collected is relatively "sparse". Focus your debugging in the specific area of interest. Don't try to collect all Port IN/OUT from reset through to the UEFI shell. At 750K I/Os per second, you'll swamp the host debugger processing, and you can't deal with all that data anyway.

Note that this only happens with AET – that is, you can only overflow by collecting too much AET data. It does not apply to LBR, SW/FW Trace, SVEN, or Intel Processor Trace. It may take some trial and error to limit the scope of your event data collection.

NOTE: Release 7.12.18 and later addressed the performance of the ASSET DCI driver. Except in very rare circumstances, trace buffer overflows should not be seen. We've preserved this section of the Getting Started Guide in case they are still encountered out in the wild – please contact our <u>Support</u> line directly if you see one.

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#### Intel Processor Trace – Slow!

When you configure Intel PT, you can specify the size of the buffer in system memory to collect trace data:

Trace Configuration					×
LBR BTS Tr	ace Hub	AET	Intel PT	Intel PT Me	emory
Trace buffer					
O Use processo	or setting	S			
Use SourcePo	oint settir	nas:			
Base address		)000000F	0		
Dase address		/0000001		P	
Length per co	ore: 16k		~		
Trace capture m	32k				
<ul> <li>Overwrite</li> </ul>	256 512				
	1M 2M	ĸ			
	4M 8M 16N 32N 64N 128 256 512 1G 2G	1 1 M M			
		OK	Ca	ancel	Help

Note that Intel PT directs instruction trace data to system memory. Although highly compact and efficient, we are not streaming over DCI to the host in this case; we buffer the code execution data until the platform is halted, at which point SourcePoint uses JTAG over DCI to collect the trace data out of system memory, reconstruct and display it. JTAG operates at fairly low speeds, and for large buffer sizes the transfer of all that data can be slow. It starts to become noticeable beyond a buffer size of 64kB. If you try to collect 1GB of data from system memory over JTAG, you can enjoy a cup of coffee and cake while this is in process. SourcePoint will display as Not Responding, and you'll get the "grey screen" if you're too persistent. SourcePoint will eventually recover, but in the interest of time and frustration, it's probably best not to try to save huge collections of instruction trace. Focus your debug efforts in the vicinity of the bug.



#### My board is not booting – what now?

Once in a while, especially during an intense debug session, we have found that the target goes into la-la land. You get to the UP splash screen, and then it just stops. Or the screen stays black. SourcePoint run-control continues to work, but it won't boot all the way up to the UEFI shell. Quitting SourcePoint, unplugging the DCI cable, killing the AssetDCI process – all are good steps in this instance, when you need to recover.

But then, once in a while, you wait the needed 20 seconds; and it doesn't boot. The screen stays blank or frozen.

Don't panic! For reasons we're not sure of just yet, after about 60 seconds, the board "wakes up" and should boot all the way to the UEFI shell.

There's only one thing: it has gone back to the factory settings, so you need to reset the WDT timer, as per <u>BIOS Settings</u> section in this manual.

Then, you'll be back in business.



## Conclusion

Thank you for getting this far! We hope that you have enjoyed the ride, and are using the power of SourcePoint successfully in your debugging and learning journeys.

Feel free to browse the SourcePoint Academy at <u>https://www.asset-</u> <u>intertech.com/sourcepoint-academy/</u> for helpful reference guides, help material and "how to" videos.

If you ever have any questions, please call, email or open a Support Case here: <u>https://www.asset-intertech.com/support/</u>. We'll be glad to help!

