

SourcePoint Intel

Getting Started Guide for the

AAEON UP Xtreme i11

Revision 1.00



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Introduction

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Revision History

Revision Number	Description	Date
1.00	Original document	November 28, 2021





Welcome!

Thank you very much for your SourcePoint Intel Individual or Institutional License purchase! We appreciate you acquiring our best-in-class debugger, and hope you enjoy using it. We strive to deliver the most powerful, easy-to-use and polished product as possible. So, please feel free to share your feedback directly at our contact information above, or via your favorite social media outlet.

As with any new tool, mastering SourcePoint takes an investment in terms of time and effort. JTAG-based debug is a fairly specialized area, and low-level "on the metal" firmware development on x86 platforms is even more so. So, in your use of the tool, you may encounter behavior that seems non-intuitive or even wrong. You may be encountering a tool corner case, a limitation inherent in JTAG or DCI, or even a bug. If so, try a few different options as may be referenced in the <u>Troubleshooting</u> section of this Guide, and if it persists, give us a call. We are here to serve.



Which Board and Cables to Purchase?

The board supported by your SourcePoint Individual or Institutional license is the AAEON UP Xtreme i11 board. It comes in three flavors: i3, i5 and i7. All three flavors are supported by your license. The Celeron version of the board is not supported by your license; it may work (we haven't tried it) but we recommend the i3, i5 or i7 to get the most value out of your purchase. This is a Tiger Lake (TGL) UP3 CPU that supports all the latest Intel debug and trace features such as Intel Processor Trace (Intel PT), Intel Trace Hub (ITH), Architectural Event Trace (AET), and others.



WARNING:

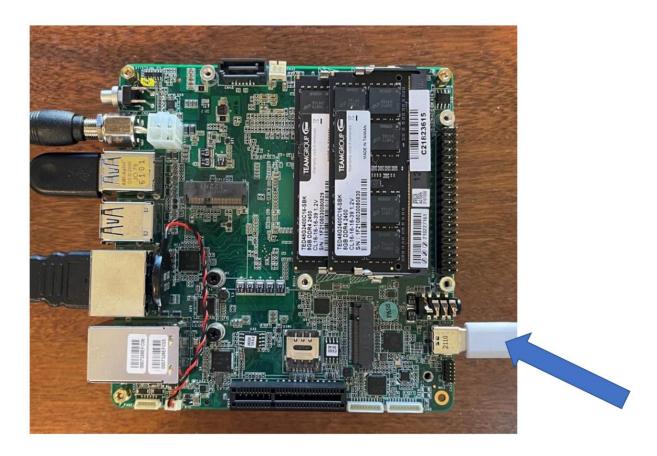
Do <u>NOT</u> plug a regular USB cable into the target and attempt to use DCI. Specialty cables, with VBUS snipped, are required; using a regular USB cable may possibly fry your target, or worse. Purchase a DCI Type-A/C cable from designintools.intel.com or mouser.com. This target has its Type-C port enabled for DCI. If you have a debug host with a Type-A port, purchase the part # ITPDCIAMCM1MU (1.0 meter) cable. The longer 1.8 meter ITPDCIAMCM2MU will work as well. If your host has a Type-C port, purchase the ITPDCIC2CD2U1M. Using Type A/C hubs have been seen to work, but are not warranted.Type A/C adapters have been seen not to work.

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BIOS Settings

The AAEON UP Xtreme i11 board, as of November 19, 2021, comes equipped with an AMI Aptio BIOS that is based upon typical Intel Customer Reference Board (CRB) BIOS. As of the time of this writing, this is Release 1.3, and can be found as a standalone image here: <u>https://downloads.up-community.org/download/up-xtreme-i11-uefibios-v1-3/</u>. Luckily, the platform comes with all the necessary hardware hooks and firmware straps to support Intel Direct Connect Interface (DCI) out of the box. The USB Type C port on the board is the port of interest:



There is only one BIOS setting change that must be made: to disable the board's Watchdog Timer (WDT). Go into the BIOS Boot menu, and set WDT Timer -> Disabled. If you don't, run-control will be successful, but the board will power-cycle every 30 seconds; putting a real crimp in your debugging!



Main Advanced Chipset	Aptio Setup - AMI Security Boot Save 8	Exit
Soot Configuration Quiet Boot MDT Timer	[Enabled] [Disabled]	▲ Enables or disables Quiet Boot option
FIXED BOOT ORDER Priori Boot Option #1 Boot Option #2 Boot Option #3	ties [USB Hard Disk] [USB CD/DVD] [USB Key:UEFI: General USB Flash Disk 1100, Partition 1]	→+: Select Screen f↓: Select Item Enter: Select
Boot Option #4 Boot Option #5 Boot Option #6 Boot Option #7 Boot Option #8	[USB Floppy] [USB Lan] [Hard DisK] [NVME] [CD/DVD]	 +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

And that's all that's needed. All the Debug Settings in the CRB Advanced menu can be safely ignored. You are now ready to test your connection, and then launch SourcePoint and begin debugging.



DbCStatus.exe: The "Green Ball" indicates a Good Connection

Luckily, there is a convenient application in the SourcePoint install directory that will tell you that the DCI driver is successfully installed on your computer, and it is possible to make a connection between SourcePoint and the target.

Navigate to C:\Program Files (x86)\Arium\SourcePoint 7.12.XX (where XX is your current SourcePoint release), and launch the DbCStatus.exe. You should see the red ball, indicating that there is no connection:

DbC Connection Status		
Connection status:	No connection	
DCI driver version:	1.10.0.0	
		Close

Ensure that the Type-C cable is firmly connected to both the host and target, power up the UP Xtreme i11. You should hear two beeps, and in a moment the ball should turn green:

DbC Connection Status		
Connection status:	USB 2.0	
DCI driver version:	1.10.0.0	
		Close

Let the platform boot to the UEFI shell. Congratulations! You have a working DCI connection. It's smooth sailing from here.

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Is the ball still red? Try cycling power on the target (don't just power cycle with the reset button; physically remove the power plug, then plug it back in again). Still red? See our <u>Troubleshooting</u> section.

Getting Started with SourcePoint

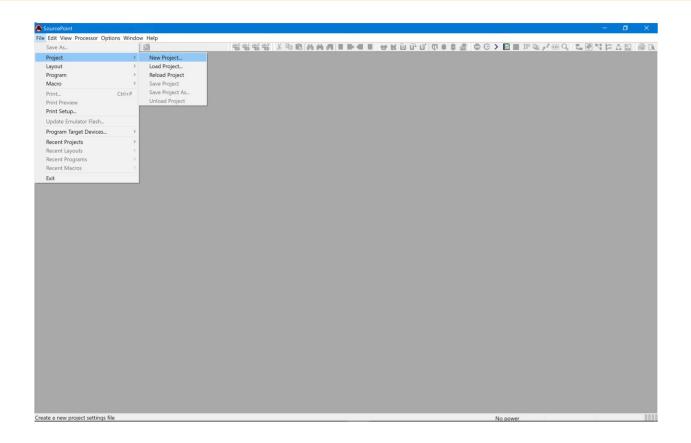
When you launch SourcePoint for the first time, you will see the main screen, mostly grey:

ourcePoint			- Ø X
Edit View Processor Options Window Help	*****	C L L L (, , , , , , , , , , , , , , , ,	
p, F5:Go, Shift+F5:Stop, F8:Step Into, F10:Step Over, Shif	+F12:Reset	No power	

SourcePoint uses Projects (files with suffix .prj) as containers for your debugging session. You can create as many Projects as you want, with all your own preferences saved. Often, once you have the SourcePoint Project configured to your liking, you'll save it and use it repeatedly during your separate debugging sessions. Other users may wish to save a separate Project for each separate debugging session. That's really a matter of user preference and what you're debugging – it's your choice.

Now it's time to create the Project. Under File > Project... select New Project:





You'll be presented by the New Project Wizard (NPW). The emulator connection should be via DCI:





New Project Wizard: Welcome	×
Welcome to the New Project Wizard	
This wizard helps you:	
- Select or add an emulator connection.	
- Create a new project file.	
DCI, DCI ~ Add/Edit	
Select an emulator connection and click Next.	
< Back Next > Cancel	Help

After hitting Next, you'll be prompted for the Project Name, Location to store the Project, and the location of the Target Configuration file:



New Project Wiz	zard: Project File	×
Project file File name:		
Location: Target conf	C:\Users\alans\Documents\Arium\SourcePoint-IA_ Browse	
	Identify Target	
	< Back Next > Cancel Help	

Note that the Target Configuration (TC) files located in C: \My

Documents\Arium\Targets are used in conjunction with the jtag-devices.xml file to define the specific silicon and SourcePoint settings necessary to ensure a successful DCI connection.

You can do an Identify Target to automatically select the TC file of interest, or you can manually select the Tiger Lake DbC TC file (TGL_DbC.tc) and hit Open:





pen				
→ 🗸 🛧 📜 > Thi	is PC > Documents > Arium > So	ourcePoint-IA_7.12.15 > Targets > TGL	v ت	🔎 Search TGL
ganize • New folde	er			· .
OneDrive - Person	Name	Date modified	Туре	Size
This PC	📕 TraceHub	10/31/2021 3:16 PM	File folder	
	TGL.tc	10/29/2021 4:15 AM	TC File	4 KB
3D Objects	TGL_DbC.tc	10/29/2021 4:15 AM	TC File	4 KB
Desktop				
Documents				
Downloads				
👌 Music				
Pictures				
🚆 Videos				
😂 Local Disk (C:)				
Network 🗸				
File na	me: TGL_DbC.tc		~	Target Configuration Files (*.tc)
				Open Cancel

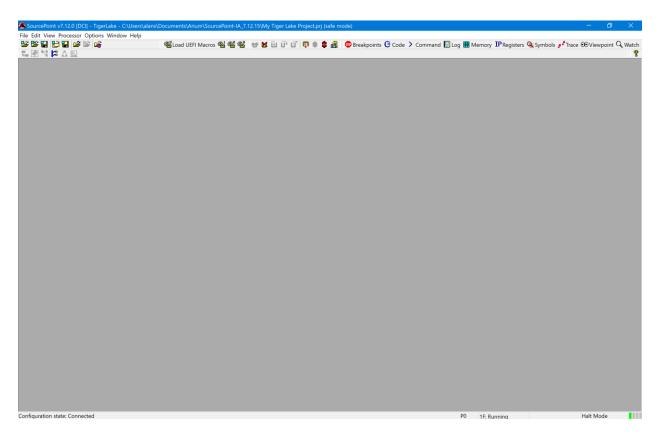
Be sure to select the DbC version! Then, your screen should look something like this:



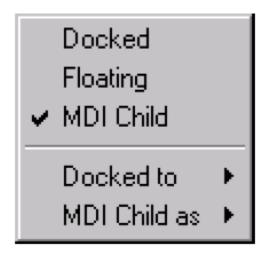
New Project Wi	zard: Project File	×
Project file		
File name:	My Tiger Lake Project	
Location:	C:\Users\alans\Documents\Arium\SourcePoint-IA_ Browse	
Target conf	figuration file	
C:\Users\a	alans\Documents\Arium\SourcePoint-IA_7.12.15\Ta Browse	
	Identify Target	
	< Back Next > Cancel	Help

Hit Next, then Finish, and SourcePoint should successfully connect to the target. You should see "JtagTest: Successful operation" followed by "Configuration state: Connected" in the Status bar at the bottom left:





Now the fun part begins. Click on the buttons at the top to set up the Viewpoint, Code, Command, Registers and other windows to your own preference. Move the windows around and resize them to take best advantage of your available screen real estate. You can right-click in the title bar of each window to change its type and, for example, to dock the window to the bottom, right side, etc.



A sample layout is below:



🖀 SourcePoint v7.12.0 [DCI] - TigerLake - C:\Users\alans\D	ocuments\Arium\SourcePoint-IA_7.12.15\My Tiger Lake Project.prj (safe mode)				- 0	×
File Edit View Processor Options Code Window Help						
월 🖀 😫 🔛 🚅 🔛 🚅	🆓 Load UEFI Macros 🎕 🍕 🥵 😁 🗶 🕒 🕩 🗊 🗊 👘 🌲 🍰 💿 Breakpoints 🕒 Code > Command 📓	log 🎹 Memory	IP Register	rs 🔍 Symbols 🧈 Trace I	● Viewpoint	Q. Watch
		<u>, , , , , , , , , , , , , , , , , , , </u>	2			Ý 💡
						-
Code (P0*) Tracking IP		00 Viewpoint				= 🔀
🕼 No Data Available - Processor not av	ailable	Name		Description		Status
			TigerLak		Running	
			TigerLak		Running	
			TigerLak		Running	
		° P3	TigerLak	(e	Running	
		<				>
		IP General Reg				
		■IA-32	Name	Value	0	
		Intel 64	RAX RBX	???????????????????????????????????????		
		General		???????????????????????????????????????		
		Floating	RDX	222222222222222222222222222222222222222		
		Segment	RBP	2222222222222222222		
	-	Control	RSI	222222222222222222222222222222222222222		
		Debug	RDI	???????????????????????????????????????		
Unknown V P Source V Go (Cursor Set Break Track IP View IP Refresh	MMX	DSD	???????????????????????????????????????		
		YMM - SI	R8	222222222222222222222222222222222222222	?	
	🚥 Breakpoints 🗖 🗉 🔀	YMM - D	R9	???????????????????????????????????????	?	
	Identifier Address Attributes	YMM - In		???????????????????????????????????????		
	Address Address	■MSR	R11	???????????????????????????????????????		
		User	R12	???????????????????????????????????????		
			R13	???????????????????????????????????????		
			R14	222222222222222222222222222222222222222		
	Edit Add Remove Remove All Enable Disable All		R15 CS	222222222222222222222222222222222222222	<i>;</i>	
		-	DS	????		
E Log			SS	2222		_
Date Time Component	Message	1	ES	2222		
①11/16/2021 17:11:49.685 RefillDisplay	List Could not refill the display due to a lack of known code position	d l	FS	2222		
			GS	????		
			RIP	???????????????????????????????????????	?	
		< >	RFLAGS	???????????????????????????????????????	?	
			_		_	
Command						1.1
Configuring Devices						^
Connecting						
	Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\aa\aaextend.mac					
P0>						
P0>						
1						~
F1:Help, F5:Go, Shift+F5:Stop, F8:Step Into, F10:Step Over	; Shift+F12:Reset	P0 1F: Ri	unning		Halt Mode	

Power Tip: the window layout can be saved as a separate file to your Project. That way, when you create a new Project, you can just Load the layout file separately, without having to create and move the windows around again. Choose File > Layout > Save Layout... to create a .lyt file, and then do a Load Layout... to save yourself time every time you create a new Project.

Power Tip: Exploring Options > Preferences... and some of the other menu items may give you some more labor-saving ideas. For instance, I like to ensure that both Load last project on startup and Save project on exit are disabled. This gives me more control on entry and exit from the application:



Preference	es									\times
General	Emulator	Breakpoints	Code	Memory	Program	IPC	Colors			
Project	t									
	ad last pro	ject on startup	D							
<mark>∕ P</mark> r	ompt befor	e automaticall	y saving	project						
Sa	ive project	on exit								
	oad target o	configuration fi	le when	project loa	aded					
Fi	le name:	C:\Users\alar	s\Docun	nents\Ariur	n\SourcePo	oint-IA_7	.12.1	Browse		
User ir	nterface									
⊡ Sł	now advanc	ed configurati	on settir	ngs	Preferre	ed editor:	notepa	ad	\sim	
⊡ Sł	now tooltips	5								
П	med windo	w refresh								
int	erval: 10	second	S							
					OK		Cancel		Help	

Now, for the AAEON UP Xtreme i11 board, there is one important thing to do to ensure that SourcePoint recognizes the memory layout and can perform some of the advanced Trace functions: this is to adjust the Memory Map. This will also eliminate some extraneous "address translation" errors in the Log window, in case you happened to notice those (they are generally, but not always, harmless). Go into Options > Target Configuration, and you should see the default mapping:



Add Edit Remove All Load Save	Start End Type Access 00000000000 00000FEFFFFF DRAM 32 bits 00001000000 00000FFFFFFF DRAM 32 bits 000010000000 0007FFFFFF DRAM 32 bits Add Edit Remove All Load Save Safe Mode (no automatic DRAM memory reads) Target Memory Target Memory Uniform Memory Access (UMA) Image: Enabled Image: Uniform Memory Access (UMA) Image: Uniform Memory Access (UMA) Image: Uniform Memory Access (UMA)	get Configur	ation								
000000000000000000000000000000000000	00000000000 00000FEFFFFF DRAM 32 bits 00000FF000000 00000FFFFFFF ROM 32 bits 000010000000 0007FFFFFFF DRAM 32 bits Add Edit Remove Remove All Load Safe Mode (no automatic DRAM memory reads) Target Memory \square Enabled \square Uniform Memory Access (UMA)	emory Map	Progran	n Flash Tar	rget Devices						
00000FF000000 00000FFFFFFF ROM 32 bits 000010000000 0007FFFFFFF DRAM 32 bits Add Edit Remove All Load Save Safe Mode (no automatic DRAM memory reads) Target Memory Save Target Memory ☑ Enabled ☑ Uniform Memory Access (UMA) ☑ Uniform Memory Access (UMA)	00000FF000000 00000FFFFFFF ROM 32 bits 000010000000 0007FFFFFFF DRAM 32 bits Add Edit Remove All Load Save Safe Mode (no automatic DRAM memory reads) Target Memory Save Target Memory Safe Mode (no automatic DRAM memory reads) Target Memory Uniform Memory Access (UMA) Safe nabled Uniform Memory Access (UMA) Save		00000								
Safe Mode (no automatic DRAM memory reads) Target Memory Image: Enabled Image: Uniform Memory Access (UMA) Image: Enable on target reset or SourcePoint invocation Image: Uniform Memory Access (UMA)	Safe Mode (no automatic DRAM memory reads) Target Memory Image: Description of the set of the se	00000FF0	00000	00000F	FFFFFFF	ROM	32	bits			
Safe Mode (no automatic DRAM memory reads) Target Memory Image: Description of the set of the se	Safe Mode (no automatic DRAM memory reads) Target Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Target Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Target Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Target Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Target Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Access (UMA) Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Access (UMA) Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Access (UMA) Image: Safe Mode (no automatic DRAM memory reads) Image: Safe Memory Access (UMA)										
 ✓ Enabled ✓ Uniform Memory Access (UMA) ✓ Enable on target reset or SourcePoint invocation 	 ✓ Enabled ✓ Uniform Memory Access (UMA) ✓ Enable on target reset or SourcePoint invocation 								d	Sa	ve
Enable on target reset or SourcePoint invocation	Enable on target reset or SourcePoint invocation			natic DRAM	memory read	ls)			mory Acc	ess (UN	4A)
☑ Disable after first Go	☑ Disable after first Go	 ⊡ Enable	on targe	t reset or So	ourcePoint inv	vocation					
		🗹 Disable	e after fir	st Go							
OK Cancel Help									-		Help

For this Tiger Lake board, you need to change these default settings (note that this is an excerpt out of your Project .prj file):

[MemoryMap] Range0=0-feffffff Range0_AccessWidth=32 bits Range0_Processor=All Range0_Type=DRAM Range1=ff000000-ffffffff Range1_AccessWidth=32 bits Range1_Processor=All Range1_Type=ROM



Range2=10000000-7ffffffff
Range2_AccessWidth=32 bits
Range2_Processor=All
Range2_Type=DRAM

to:

[MemoryMap] Range0=0-bffffff RangeO AccessWidth=32 bits Range0 Processor=All Range0 Type=DRAM Range1=c000000-fefffff Rangel AccessWidth=32 bits Rangel Processor=All Rangel Type=SRAM Range2=ff000000-fffffff Range2 AccessWidth=32 bits Range2 Processor=All Range2 Type=ROM Range3=10000000-7ffffffff Range3 AccessWidth=32 bits Range3 Processor=All Range3 Type=DRAM

The easiest way to do this is to Edit the first entry in the Memory Map, changing OFEFFFFF to OBFFFFFFF, and then do an Add to add in OCOOO0000 OFEFFFFFF SRAM 32 bits. The new Memory Map will look like this:



get Configur	ation								
lemory Map	Program	Flash	Target Devices						
Start		△ End		Туре	Acc	ess			
00000000	00000	0000	OBFFFFFFF	DRAM	32	bits			
000000000			OFEFFFFFF	SRAM		bits			
00000FF0			OFFFFFFFF	ROM		bits			
00001000	00000	0007	FFFFFFFFFF	DRAM	32	bits			
Add		Edit	Remove	Pom	ove All	Load	1	Sal	/e
Auu		Luit	Remove	Kelli		LUat		Jav	/e
Safe Mode	(no autom	natic DRA	M memory read	s)	Target I	Memory-			
🖂 Enable	-					-	nory Acce	cc (LIN	14)
	u				V OII		nory Acce	55 (01-	IA)
🗹 Enable	on target	reset o	r SourcePoint inv	ocation					
Disable	ofter fire	+ Co							
🗹 Disable	e after firs	t Go							
🗹 Disable	e after firs	st Go							
🗹 Disable	e after firs	st Go							
⊡ Disable	e after firs	st Go							
⊡ Disable	e after firs	t Go			OF	/	Cance	1	Help

Next, it is necessary to disable the platform TCO Timer, so that you can halt at the reset vector successfully, without the target going into limbo. Click on File > Macro > Configure Macros... and click on the Event Macros tab. Click on Browse and select the Macros\Intel\ADL_TCO_Timer_Disable.mac. This is the one you need to choose for the Reset (after) event.

This is a good point to do a Project > Save Project... That way, you don't have to start all over, if for some reason your project gets messed up.

At this point, you are ready to fully begin your debug session. Many of the operations can be accessed via the toolbar at the top of the screen. You can issue a Stop on the



22

target, Step Into, Reset it and halt at the reset vector, set some breakpoints, Go to the breakpoint, and so on.

MOV ECX, EI SAL ECX, 2 MOV EAX, DW JMP 000000 CMP AL, 02	ORD PTR [R8]+000000c0			• P1	ligerLake ligerLake		copped	Statu
MOV ECX, 2 SAL ECX, 2 MOV EAX, DW JMP 000000 CMP AL, 02	X ORD PTR [RCX][RAX]	Ê		* P0 • P1	ligerLake ligerLake	St	opped	
SAL ECX, 2 MOV EAX, DW JMP 000000 CMP AL, 02	ORD PTR [RCX][RAX]					St	opped	
JMP 000000 CMP AL,02								
CMP AL,02	00640d20feL			• P2	ligerLake	St	opped	
				• P3	FigerLake	St	opped	
	ORD PTR [R8]+000000c0			۲.				
	ptr 00000000640d203aL							
				General Re	gisters (PO*)			8
				∎IA-32				
				Intel 64				
				General				
				-Floating F	RCX			
				Segment	RDX			
- Diote	per obcoccocciulition	· ·						
Go Cursor Set Break	Track IP View IP F	Refresh			Dep			
				YMM - SI				
Breakpoin				-YMM - D	DQ			
		Attaitudee		YMM - In	R10	000000601D34203C		
Identilier	Address	Attributes			R11	00000000606BF800		
				User				
Edit	Add Remove	Remove All Enable	Disable All					
· · · · · · · · · · · · · · · · · · ·								
Mes	sage							
		or in 0000000640D201E	L					
				< >				
	MOVZX EAX, WA JMP 000000 MOV ECX, ED MOV EX, EX JMP 000000 MOV RAX, GM MOV RAX, GM IEST RAX, GA JE short ic Cursor Set Break	MOVZX EAX, MORD PTF. [FCX] [FAX] JMF 00000000640420 feL MOV ECX, EXX MOV AL, BYTE PTR. [RCX] (FAX] JMF MOV RAX, GRAD PTR. [RCX] +0000140 RAX, GRAD PTR. [RCX] +0000140 RAX, RAX JE short ptr 000000064011ff5L io Cursor Set Break ∑Track IP View IP I © Breakpoints Identifier Address Edit Add Remove Message	MOVZX EAX, MORD PTR [RCX][RAX] JMP 0000000640d20feL MOV ECX, EDX MOV ECX, EDX MOV RAX, GRORD PTR [RCX]+00000140 RAX, GRORD PTR [RCX]+00000140 TEST RAX, RAX JE short ptr 0000000640d1ff5L short ptr 0000000640d1ff5L © Breakpoints Identifier Address Attributes Edt Add Remove Remove All Enable Message	MOVZX EAX, MORD PTR [REX][RAX] JMP 00000000640d20feL MOV ECX, EDX MOV ECX, EDX MOV RAX, GWORD PTR [RCX] + 00000140 TEST RAX, RAX JE short ptr 0000000640d1ff5L © Breakpoints Identifier Address Attributes Edit Add Remove Remove All Enable Disable All Message	MOVZX EAX, MORD PTR [REX][RAX] JMP 00000000640d20feL MOV ECX, EDX MOV RAX, QWORD PTR [RCX] (FAX) JMP 0000000640d20feL MOV RAX, QWORD PTR [RCX]+00000140 REST RAX, RAX JE short ptr 0000000640d1ff5L jo Oursor Set Break Orrack IP View IP Refresh VMM - DI VMM - DI Identifier Address Attributes MSR User Message Massage Handling Exception: Translation error in 00000000640D201EL	MOVZX EAX, MORD PTH: [REX] [RAX] JMP 00000000640420feL MOV ECX, EDX MOV ECX MOV ECX Edt	MOVZX EAX, MORD PTR [ECX][RAX] MV ECX, EDX MOV EAX, OKOBO PTR [ECX] + 00000140 TEST EAX, RAX So Cursor Set Break Identifier Address Address Attributes MMM - Fig MMM - Fig Mov RAX Address Attributes Mov - Fig Mov - Fig Mov - Fig Mov - Fig Besage	MOVZX EAX, MORD PTR [RCX][RAX] MV EAX, EAX MORD ORDOROGOGAD20FL. MOV ECX, EDX MOV ECX, CONDONOGOGAD20FL. So Cursor Set Break @ Drackpoints Control Bereakpoints Control Identifier Address Add Remove Message Exception: Translation error in 00000006400201EL

Hit the Refresh button in the Code window after the first Stop. This is only necessary once; the Code window will automatically refresh with all run-control operations (stop, go, single-step, etc.) afterwards.

Refer to the <u>SourcePoint User Guide</u> in your install directory for detailed instructions on using all of the tool's features.

Congratulations, you have mastered SourcePoint's basic capabilities, and are using run-control. Many users are content to just use these basic operations, because run-control by itself is very powerful. However, iff you wish to master the product and use some of its more advanced features, read on.

Advanced Topics: Using Trace

Trace is by far one of the most useful debugging utilities for triaging the most difficult, hard-to-reproduce bugs. Fortunately, the Tiger Lake CPU is equipped with all the latest-and-greatest trace logic, and SourcePoint supports them all.

Let's look at a few of them, and how to configure their use in SourcePoint.

Intel Trace Hub: SVEN

Event tracing on the TGL platform is accomplished by the Intel Trace Hub (ITH). Fortunately, using DCI, events supported by the ITH can be streamed directly out of system reset. The one limitation that exists is that some events (like Port IN/OUT tracing) happen so frequently at some points of the boot process that they overwhelm the capacity of the USB 2.0 (DbC2) connection and event processing, and thus cause buffer overflows – but these should be rare as long as the events collected are relatively close to the debug point of interest.

System Visibility Event Nexus (SVEN) is a means by which, within the AMI BIOS, printf statements are output through the ITH, as opposed to the serial port. This speeds up the boot time, and reduces the likelihood of port latency contributing to the masking of bugs.

The first thing to do is to configure the ITH. Reset the target and halt at the reset vector, address FFFFFF0:



🛞 SourcePoint v7.12.0 [DCI] - TigerLake - C:\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\My Tiger Lake Project.prj (safe mode)				– Ø ×
File Edit View Processor Options Code Window Help				
😰 🎬 🚼 😭 📽 🞼 🥵 🥵 🔩 🥵 🔮 🖬 🕑 🗊 👘 🚔 🚱 Breakpoints 🕒 Code > Command 🔯	og 🎟 Memory	TP Registers	Symbols	Niewpoint Q Watch
	log minimory	Li negisters 🔩	(symbols y made o	O Viewpoint - Watch
				8
Code (P0*): (16-bit) Tracking IP 00000000L - FFFFFFFL	● Viewpoint			- • ×
FFFFFEBL 0000 ADD BYTE PTR [BX+SI],AL	Name	Desc	cription	Status
FFFFFEDL 0000 ADD BYTE PTR [BX+SI],AL	* P0	TigerLake		Stopped
FFFFFEFL 00 DB 00				
C PFFFFFF0L 90 NOP				
FFFFFFIL 90 NOP				
FFFFFF2L E923C0 JMP near16 ptr ffffc018L FFFFFF5L 0000 ADD BYTE PTR [BX+S1], AL				
FFFFFFJL 000B ADD BLB FR [BA+31],AL	<			>
FFFFFF91 0000 ADD BYTE PTR [BX+SI],AL				
FFFFFFBL 0000 ADD BYTE PTR [BX+SI], AL	General Re			
FFFFFFDL 00FC ADD AH,BH	■IA-32		lue	
FFFFFFFL FF DB ff	Intel 64		000000000000000	
	General		0000000000000000	
	-Floating I		00000000000000000000000000000000000000	
	Segment		000000000000000000000000000000000000000	
	Control		000000000000000000000000000000000000000	
	Debug			
FFFFFF0L V P Disassembly Go Cursor Set Break Track IP View IP Refresh	MMX	DCD 00		
	YMM - S	D9 00	000000000000000000000000000000000000000	
📴 Breakpoints 🕞 🗉 🔀	YMM - D	R9 00	000000000000000000000000000000000000000	
Identifier Address Attributes	YMM - In		000000000000000000000000000000000000000	
Identifier Address Address	■MSR		000000000000000000000000000000000000000	
	User		000000000000000	
			000000000000000	
Edit Add Remove All Enable Disable All			000000000000000000000000000000000000000	
	-	DS 00		
E Log		SS 00		
Date Time Component Message	1	ES 00		
11/17/2021 15:20:08.130 tco.clearbars Cleared PCI Express Base		FS 00		
		GS 00	00	
		RIP 00	0000000000FFF0	
	< >	RFLAGS 00	00000000010002	
Command				
Scanning Devices				^
Configuring Devices				
Connecting				
Loading Command Language Extensions: C:\Users\alans\Documents\Arium\SourcePoint-IA_7.12.15\Macros\aa\aaextend.mac				
P0>				
2005 Loading Reset (after): C:\Users\alans\Documents\Arium\SourcePoint-IA 7.12.15\Macros\Intel\ADL TCO Timer Disable.mac				
Post (arter). C. (osers (arter).				
				~
Target Stopped: Target reset	P0 18: St	opped S	pecial H	lalt Mode

The next step is to load in the ITH macros. This is accomplished by File > Macro > Load Macros... and selecting C:\My Documents\Arium\SourcePoint-IA_7.12.15\Macros\Intel\TraceHub.mac. Then, in the Command window, at the P0> prompt, type:

npkEnableForce("cpcie=1", "tsact=1")

Power tip: If you want to know more about what this macro can do, type npkEnableForce_Help().

Now, it's time to set up the ITH, and let it know what you want to trace. Click on the Trace button in the toolbar at the top, click on the Configure... button, and then click on the Trace Hub tab:





경 1월	📭 🌒 🏥 🌋 😊 Breakpoints 🕒 Code 🕨 Command 🖾 Log 🏢 M	emory IP Registers 🎕 Symbols 📌 Trace 👀 Viewpoint 🔍 Wate
	Trace Configuration X	oint 🗆 🗆 🗶
Cost of (10:50) flacing) # 0000000 FFFFFFF Description Description <thdescription< th=""> Description</thdescription<>	LBR BTS Trace Hub AET Intel PT Intel PT Memory Masters to trace None	ne Description Status TigerLake Stopped TigerLake Not Active TigerLake Not Active TigerLake Not Active
FFFFFF5L 0000 FFFFFF7L 0000 FFFFFFF0 0000 FFFFFFF1 0000 FFFFFFF1 0000 Trace source is not enabled FFFFFFF1 000C	All List: Example: 8, 32-255	al Registers (P0')
FFFFFFFL FF FFFFFL Y Disassembly V Configure Display Filter	Trace routing Trace routing Trace Hub: System memory AET: Trace Hub System memory trace buffer © Use BIOS settings Use SourcePoint settings Base address: 000000000P	IA RAX 000000000000000000000000000000000000
Log Message Date Time Component Message 11/17/2021 15:48:06.723 npk.checkenabled Trace Hub has not been 11/17/2021 15:48:07.673 npk.checkenabled Trace Hub Device Now E 11/17/2021 15:48:07.673 npk.enable PCH Trace Hub PCI Conf 11/17/2021 15:48:07.655 npk.setbase MTB_BAR not configured 11/17/2021 15:48:07.455 NK BAR not configured	Length:	R14 000000000000000000000000000000000000
11/17/2021 15:48:08.149 npk.setbase FW_BAR not configured. 11/17/2021 15:48:09.733 npk.setloglevel Logging level set to 0: 11/17/2021 15:48:09.829 npk.enableforce.option TSACT Enable Bit=lb	Master / Channel definitions Filename	se]
ommand tsact=0/1 -> Enable Time Stamp Counter in Trace Hub cpcie=0/1 -> Clear PCI Express MMIO Base after conf log=0.7 -> Set the Logging Level for Trace Hub mtbbar=BAR -> Override the default MTB BASE with BAR subar=BAR -> Override the default SW BASE with BAR	OK Cancel Help	
<pre>buble of the default of default of many with bar fwbar=Bar -> Override the default FW_BASE with BAR 0>npkEnableForce("cpcie=1", "tsact=1") 0></pre>		18: Stropped Special Halt Mode

Go to the bottom and click select the C:\MyDocuments\Arium\SourcePoint-IA_7.12.15\Targets\TGL\TraceHub\TGL Ports.xml file to define the Master / Channel definitions. Click OK, and then go back in again, click on List under Masters to trace and select the ellipses (...) to look at the choices available:



≝ ≌ ⊒ ≌ ⊒ ≥ ≡ ≥ • ● * ≓ Δ ⊡	📸 Load UEFI Macros 🍓 🥁	n 🖞 🖶 🖬 🖬 🗊 🗊 🗊 🕸 🌲 🖉 Breakpoints 🕒	Code 🕻 Command 📗	🛛 Log 🎹 Memory 👖	Registers 🔍 Symbols 📌 Tr	ace 🖲 Viewpoint 🔍 Watch
Code (P0*): (16-bit) Tracking IP 00000000L - FFFFFFFL				•••Viewpoint		X
FFFFFEBL 0000 ADD FFFFFEDL 0000 ADD FFFFFFEDL 000 DB FFFFFFFFEDL 90 NOP	BYTE PTR [BX+SI], BYTE PTR [BX+SI], 00	LDR DIS Hacehab Act InterPT InterPT Mem	Nory	• P1 Tig	Description erLake erLake erLake	Stopped Not Active Not Active
FFFFFFF1L 90 NOP FFFFFFF2L 5923C0 MD FFFFFF7L 0000 FFFFFF7L 0000 FFFFFFF1L 0000 STATE Pn ADDR Trace source is no	nearl6 ptr ffffc01 INSTRUC t enabled	Masters to trace None All Example: 8, 32-255	Masters to Trace		erLake X	Not Active
FFFFFFDL OOFC		Trace routing Trace Hub: System memory ~ Intel PT: System Memory AET: Trace Hub System memory trace buffer	22: 22: 22: 22: 24: 25: 26: 27: 28: 29: 29:		D000000 D000000	00000 00000 006C1 00000 00000 00000 00000
•		Use BIOS settings		Clear All	Set All 00000000	
Disasse	mbly V Configure	O Use SourcePoint settings	Select the masters	to enable for trace.	00000000 00000000 00000000	0000
Date Time Component	Message			OK	Cancel	
●11/17/2021 15:48:09.928 npk.enablefor ●11/17/2021 15:54:18.724 processGlobal	ce.option Clear P	Longon.	bbles a	swapped"		
		Master / Channel definitions				~
Command		Filename It-IA_7.12.15\Targets\TGL\TraceHub\TGL Port	2			1
cpcie=0/1 -> Cle log=07 -> Set mtbbar=BAR -> Ove swbar=BAR -> Ove	ble Time Stamp Count ar PCI Express MMIO the Logging Level f rride the default MT rride the default SW	OK Cancel BASE with BAR	Help			^
P0>npkEnableForce("cpcie=1", "tsact=1")	rride the default FW	BASE with BAR				
P0>						

For now, select 20: (UEFI:SVEN) and 48 (UEFI:SVEN). Also, under Trace Routing, select Trace Hub and set to DbC:



ace Configuration				\times
.BR BTS Trac	e Hub AET	Intel PT	Intel PT Mem	ory
Masters to trace				
○ None				
List: 20,48				
Trace routing				
Trace Hub: DbC	2	\sim		
Intel PT: Sys	tem Memory	\sim		
AET: Tra	ce Hub	\sim		
 Use BIOS settin Use SourcePoir 				
Base address:	00000000P			J.
Length:		\sim		
Timestamp				
Alignment pack	ets Fre	equency:	CTC 16	~
Master / Channel d	efinitions			
Filename: It-IA_7	.12.15\Targets	\TGL\Trac	eHub\TGL Port	
	ОК	Ca	ncel	Help



Hit OK.

Now, and this is very important, you need to calibrate the ITH. The Trace window should be right-clicked and set to Trace Hub - SW/FW Trace (if it isn't already). Click on the <code>Calibrate</code> button, and you should be rewarded with it being successfully detected:

FFFFEBL 0000 FFFFEDL 0000 FFFFEDL 00 FFFFFIL 90 FFFFFIL 902 FFFFFIL 923C0 FFFFFIL 0000 FFFFFFIL 0000	IP 00000000L - FFFFFFFL ADD DB NOP NOP mp Trace Hub - SW/FW Tra STATE ADDR No data available	BYTE PTR [BX+SI BYTE PTR [BX+SI 00	018L					Viewpoin Name P0 P1 P2			Stoppe	
FFFFEDL 0000 FFFFFEL 90 FFFFFL 90 FFFFFL 923C0 FFFFFL 9000 FFFFF2L 823C0 FFFFF2L 9000 FFFFF2L 9000 FFFFF2L 9000 FFFFF2L 9000 FFFFF2L 9000	ADD DB NOP .TMD Trace Hub - SW/FW Tra STATE ADDR	BYTE PTR [BX+SI 00 pear16 ptr ffff	018L					• PO • P1	TigerLak TigerLak	e :e		ed
FFFFEL 00 FFFFF0L 90 FFFFFL 90 FFFFF2L E923C0 FFFFF5L 0000 FFFFF7L 00FB FFFFF9L 0000 FFFFFDL 000C	DB NOP NOP .TMD Trace Hub - SW/FW Tra STATE ADDR	00 near16_ptr_ffff, ce	c018I.					• P1	TigerLak			
FFFFF0L 90 FFFFF1L 90 FFFFF5L 0923C0 FFFFF5L 0000 FFFFF5L 0000 FFFFF5L 0000 FFFFF5L 0000 FFFFF5L 000C	NOP NOP .TMD Trace Hub - SW/FW Tra STATE ADDR	nearl6 ntr ffff										
FFFFF2L E923C0 FFFFF5L 0000 FFFFF7L 00FB FFFFF9L 0000 FFFFFBL 0000 FFFFFBL 000FC	Trace Hub - SW/FW Tra STATE ADDR	ce										
FFFFF5L 0000 FFFFF7L 00FB FFFFF9L 0000 FFFFFBL 0000 FFFFFDL 00FC	Trace Hub - SW/FW Tra STATE ADDR	ce						• P3				
FFFFF9L 0000 FFFFFBL 0000 FFFFFBL 0000 FFFFFDL 00FC	STATE ADDR		TON					<				_
FFFFFBL 0000 FFFFFBL 00FC		indinou				~						
FFFFFDL 00FC			101					IP General I	Registers (PO*)			• ×
FFFFFFL FF								■IA-32	Name	Value	-	
								■Intel 64	RAX RBX	000000000000000000000000000000000000000		
						_	_	-Genera -Floatin		000000000000000000000000000000000000000		
				SourcePoi			×	Segme	nt RDX	0000000000806C		
					T 111	c		Control	RBP	000000000000000		
					Trace Hub su	cessfully detecte	d	Debug	RSI RDI	000000000000000000000000000000000000000		
FFFOL 🗸 🖌				_		OK		MMX	DSD	000000000000000000000000000000000000000		
								-YMM -	SF R8	0000000000000000000	0	
							_	YMM - YMM -	DF R9	000000000000000000000000000000000000000		
	<					Ň		•MSR	R10 R11	000000000000000000000000000000000000000		
-						, <u>, , , , , , , , , , , , , , , , , , </u>		User	R11 R12	000000000000000000000000000000000000000		
	-00000018 Disasse	embly ~ Configure	Display	Filter	Calibrate	Refres			R13	000000000000000000000000000000000000000		
L									R14	000000000000000000000000000000000000000	0	
te Time	Component	Messa	nge F Enable Bit	11-								1
/1//2021 16:0/:31. /17/2021 16:07:31.	.693 npk.enablefor .796 npk.enablefor	ce.option TSAC	r Enable Bits r PCI Expres									
1772021 1010101	not aparonabioioi	ore of the other	tor improv	0 2400								
and												
	swbar=BAR -> Ove	rride the default	SW BASE wit	h BAR								_
pkEnableForce("cpo	<pre>fwbar=BAR -> Ove cie=1", "tsact=1")</pre>	rride the default	FW_BASE with	h BAR								
ing Reset (after):	C:\Users\alans\D	ocuments\Arium\Sou	ircePoint-IA	7.12.15	Macros\Inte	ADL TCO Ti	mer Disable.ma	z				
	cie=1", "tsact=1")						_					

Power tip: The Calibrate button only needs to be used once per project. The npkEnableForce("cpcei=1", "tsact=1") command must be re-issued after each reset.

Then, hit the Go button in the top toolbar, and boot to the UEFI shell. Then hit Stop. You will see the SVEN printf data in all its glory:



Frace Hub -	SW/FW Trace					• ×
STATE	ADDR	INSTRUCT	ION			^
	UEFI:SVEN:C	ONSOLE				
	POSTCODE=	<00000060>				
-000000074		UEFI:	SVEN: CONSOI	LE="B"		
-000000064		UEFI:	SVEN: CONSOI	LE="b"		
-000000059		UEFI:	SVEN: CONSOI	LE="-%-0"		
-000000054		UEFI:	SVEN: CONSOI	LE=""		
-000000049		UEFI:	SVEN: CONSOI	LE=""		
-000000044		UEFI:	SVEN: CONSOI	LE=""		
-000000041		UEFI:	SVEN: CONSOI	LE="POST"		
-000000036		UEFI:	SVEN: CONSOI	LE="CODE"		
-000000031		UEFI:	SVEN: CONSOI	LE="=<00"		
-000000026		UEFI:	SVEN: CONSOI	LE="0000"		
-000000021		UEFI:	SVEN: CONSOI	LE="60>-"		
-000000016		UEFI:	SVEN: CONSOI	LE="-"		~
<					1912	>
-000000074	Disassembly	 Configure 	Display	Filter	Calibrate	Refre

Actually, it looks better if you select the Display... button, and de-select Data lines:

Trace Display Settings	×
Disassembly	Source code
Object code Instruction lines	Source lines Every instruction
Symbols Data lines	Line numbers
Pseudo-ops 🛛 Label lines	Source code file information
Display case: Mixed \lor	Filename Function
Radix indicator: None ~	Path Offset
Instruction width: 50	Line numbers Every instruction
	Timestamp
	🗌 Delta 🛛 Accumulate
	Time align with other views
Colors	OK Cancel





🛃 Trace Hub - SW/FW Trace	
STATE ADDR INSTRUCTION	TIMESTAMP 🔨
POSTCODE=<00000B41>	
-000001033 UEFI:SVEN:CONSOLE	-3.271 sec
POSTCODE=<00000B42>	
-000000973 UEFI:SVEN:CONSOLE	-3.220 sec
POSTCODE=<00000B47>	2,000
-00000912 UEFI:SVEN:CONSOLE POSTCODE=<00000C80>	-3.202 sec
-00000852 UEFISVEN:CONSOLE	-3.107 sec
POSTCODE=<00000C81>	3.107 Sec
-000000792 UFT:SVEN:CONSOLE	-3.107 sec
POSTCODE=<00000C82>	0.107 500
-000000732 UEFI:SVEN:CONSOLE	-3.106 sec
POSTCODE=<00000C83>	
-000000673 UEFI:SVEN:CONSOLE	-3.100 sec
POSTCODE=<00000A61>	
-000000613 UEFI:SVEN:CONSOLE	-3.100 sec
POSTCODE=<00000A63>	
-000000554 UEFI:SVEN:CONSOLE	-3.094 sec
POSTCODE=<00000A03>	2 004 555
-000000494 UEFI:SVEN:CONSOLE	-3.094 sec
POSTCODE=<00000A65> -000000435 UEFI:SVEN:CONSOLE	-3.093 sec
POSTCODE=<00000A64>	5.055 Sec
-000000375 UEFI:SVEN:CONSOLE	-3.092 sec
POSTCODE=<00000B0F>	0.002 500
-00000315 UEFI:SVEN:CONSOLE	-3.061 sec
POSTCODE=<00000C6A>	
-000000255 UEFI:SVEN:CONSOLE	-3.059 sec
POSTCODE=<00000C71>	
-000000195 UEFI:SVEN:CONSOLE	-3.057 sec
POSTCODE=<00000C7F>	
	-622.562 ms
POSTCODE=<0000004F>	10
-00000074 UEFI:SVEN:CONSOLE	+0 ns 🗸
-000000375 Disassembly V Configure Display Filter Calibrate Refresh	

This BIOS is not particularly verbose, so all we see here are the POST codes. But, you get the idea.

Architectural Event Trace

Click on the Trace button in the top toolbar, and select Configure... again. Within the Trace Hub tab, add '18' to the list of Masters to trace.



ce Configuration				×
BR BTS Trac	e Hub AET	Intel PT	Intel PT Memo	ory
Masters to trace				
○ None				
List: 18,20,4	8]	
Trace routing				
Trace Hub: DbC		~		
Intel PT: Syst	em Memory	\sim		
AET: Trad	ce Hub	\sim		
 Use BIOS settir Use SourcePoint 				
Base address:	00000000P			P
Length:	8M	\sim		
Timestamp Alignment pack Master / Channel d		equency: CT	°C 16	~
Filename: It-IA_7	.12.15\Targets`	\TGL\TraceH	lub\TGL Ports	
	ОК	Cano	cel	Help





Then click on the AET tab, select p0 as Processors to trace, and select RDMSR/WRMSR and Port In/Out as events to trace:



			×
BR BTS Trace Hub AE	T Intel PT I	ntel PT Memory	
Processors to trace			
○ None			
List: p0			
(e.g., P0, P4-P7)			
(6.9., 10, 1417)			
Event sharing			
 Apply events to all process 	core		
	5015		
O Apply events to:	\sim		
		· · · · · · · · · · · · · · · · · · ·	
Event	Enabled	LBR	
HW/SW Interrupt			
IRET			
IRET Exception			
IRET Exception RDMSR/WRMSR			
IRET Exception RDMSR/WRMSR Port In/Out			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint	□ ☑ ☑		
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM MONITOR/MWAIT			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM MONITOR/MWAIT WBINVD			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM MONITOR/MWAIT WBINVD SGX			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM MONITOR/MWAIT WBINVD			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM MONITOR/MWAIT WBINVD			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM MONITOR/MWAIT WBINVD			
IRET Exception RDMSR/WRMSR Port In/Out Code breakpoint Data breakpoint BTM SMI/NMI/RSM MONITOR/MWAIT WBINVD	Advanced	Clear all	



Now, the trick here is not to try to capture too much data, otherwise you'll overwhelm the ITH packet processing. So, you should debug only close to your event or code of interest. One way to demonstrate this is to use the Command window to simulate a break on any read/write of, say, port x'CF8', the PCI CONFIG_ADDRESS. This is conveniently done by issuing at the Command window P0> prompt:

go til cf8io

This will run the target until the next IN or OUT to CF8. This happens fairly frequently, so you'll not likely overflow any buffers.

ace Hub - SW/FW Trace				
1000 3000	Fevent Trace			
				010
data available - Unable	STATE Pn	ADDR INSTRUCTION	TIMESTAMP	 Stopped (hit
The second s		Event: Port Out: Port=0021, Data=000000FF		Stopped (hit
	-000000586 P0	000000067EE16D1 OUT DX,AL	-72.813 us	Stopped (hit
	Contraction of the second second	Event: Port Out: Port=00A1, Data=000000FF		Stopped (hit
	-000000550 P0	000000067EE16D7 OUT DX,AL	-66.406 us	
		Event: Port In: Port=1830		
	-000000514 P0	000000067EE16DD IN EAX, DX	-66.276 us	
		Event: Port In: Port=1830, Data=80002033		6 8
	-000000478 P0	000000067EE16DD IN EAX, DX	-64.036 us	
		Event: Port Out: Port=1830, Data=80002030		
	-000000442 P0	000000067EE16E1 OUT DX,EAX	-62.240 us	000008
		Event: Port In: Port=1830		000000
	-000000406 P0	000000067EE179B IN EAX,DX	-51.406 us	000000
		Event: Port In: Port=1830, Data=80002033		000CF8
	-000000370 P0	000000067EE179B IN EAX, DX	-48.281 us	0A3CC0
		Event: Port Out: Port=1830, Data=80002033		0CD000
	-000000334 P0	000000067EE179F OUT DX,EAX	-46.484 us	B81C00
		Event: Port In: Port=1830		0A3C40
	-000000298 P0	000000067EE17A0 IN EAX, DX	-46.354 us	E9D3B0
		Event: Port In: Port=1830, Data=80002033		
	-000000262 P0	000000067EE17A0 IN EAX, DX	-44.115 us	00000E
		Event: Port Out: Port=1830, Data=80002033		000000
	-000000226 P0	000000067EE17A4 OUT DX, EAX	-42.318 us	OA3AFO
		Event: Port Out: Port=0021, Data=000000FF		A23018
	-000000190 P0	000000067EE17DD OUT DX,AL	-24.922 us	000002
0375 Disassembly ~		Event: Port Out: Port=00A1, Data=000000FF		000001
in the second se	-000000154 P0	000000067EE17E7 OUT DX, AL	-17.161 us	
		Event: Port Out: Port=0070, Data=000000B2		_ O
Time (-000000118 P0	0000000640CE1B6 OUT DX,AL	-8.099 us	
7/2021 16:35:39.976 p		Event: Port Out: Port=0076, Data=00000005		
7/2021 16:35:49.222	-000000082 P0	0000000640CE1CD OUT DX,AL	-494.791 ns	
		Event: Port Out: Port=OCF8, Data=80000008		
	-000000046 P0	0000000640CE1E4 OUT DX, EAX	+0 ns	
	000000010 20	oreconcertainer our prijzen		~
	Transa Transa			
	-000000550 Dis	assembly <u>Configure</u> Display Filter Calibrate Re	efresh	
L	L			
ng Reset (after): C:\U	sers\alans\Docum	ments\Arium\SourcePoint-IA 7.12.15\Macros\Intel\ADL TCO Tim	mer Disable.mac	
EnableForce("cpcie=1"	, "tsact=1")	an se an a statement de la catal de la		
til cf8io				
C11 01010				

After issuing the command, you'll see something like this:

Scrolling up a little, you'll see a mix of Port In/Out and RDMSR/WRMSR. All timestamped, and with a CYCLE that can be used to correlate with other trace sources.

Power tip: The Last Branch Record (LBR) stack associated with each event can be captured as well. This is a very powerful debugging utility, especially when troubleshooting code execution leading up to events before system memory is initialized and Intel Processor Trace is available.



ce Configuration			×
BR BTS Trace Hub AE	T Intel PT I	Intel PT Memory	
Processors to trace			
○ None			
Onone			
List: p0			
(e.g., P0, P4-P7)			
Event sharing			
_	corc		
Apply events to all proces	5015		
○ Apply events to:	\sim		
Event	Enabled		
HW/SW Interrupt			
IRET			
Exception			
RDMSR/WRMSR	Y		
Port In/Out	Y		
Code breakpoint			
Data breakpoint			
BTM			
SMI/NMI/RSM			
MONITOR/MWAIT			
WBINVD			
SGX			
	Advanced	Clear all	
ОК	Cano	cel He	

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Intel Processor Trace

Intel PT is available only after system memory is initialized.

It's easy to set up. Click on the Trace button in the top toolbar, click the Configure... button, click on the Intel PT tab, put p0 in Processors to trace, and click on TSC and Cycle accurate under the Timestamp heading:

Trace Configuratio	n	×
LBR BTS	Trace Hub AET Intel PT Intel PT Memory	
Processors to	trace	
○ None		
List: p0		
Share filter / ti	mestamp settings	
	ngs to all processors	
◯ Apply setti	ngs to: P0 🗸	
Filters		
Range 1:	Enter symbol or start-end	
Range 2:	Enter symbol or start-end	
CPL:	User	
CR3:		
Timestamp		
TSC		
	Frequency: CTC 6	
MTC		
🗹 Cycle accu	rate Threshold: 0 (fine) ~	
	OK Cancel Help	

That's all. Then use the go til cf8io trick to capture some instruction trace data:



data available - Unable	🛃 Event Trace												
data available - Unable												Test reservices of the test reservices of test reser	Sta
	STATE	Pn	ADDR	INST	RUCTION					TIMESTAN	IP A	Stopped (hit
			Event: Po	r Intel Process									~
	-000000658	P0		E STATE Ph	ADDR	THORD	LOT TON						^
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	-000000442	P0	00000006		00000006	40CE025 MOV	[R	SP]+10,RSI					
			Event: Po:			40CE02A PUSH	RD						
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			Event: Po:			40CE02F LEA		1,[00000006	40cd000]				
	-000000370	P0	000000006			40CE036 MOV		L,CL					
			Event: Po			40CE039 TEST		,CL					
	-000000334	P0	000000006			40CE03B JE		000000640ce1					
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	-000000298	P0	000000006			40CE134 XOR		K,EBX					
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There's a lot more that you can see and do with these Trace utilities. SourcePoint can use Intel PT to display a Call Chart and Call Tree. You can open up Code Tracking windows that update dynamically as you walk through the code, showing you exactly where you are and the interaction between code and events. When you have source and symbols available, the firmware flow becomes much more intuitive and visual. Indulge your curiosity and imagination.

The video at <u>https://www.asset-intertech.com/wp-content/uploads/2021/11/UP-Xtreme-i11-Getting-Started.mp4</u> shows some of these capabilities. The <u>SourcePoint User Guide</u> also provides a very thorough, comprehensive review of the tool. And visit our <u>SourcePoint Academy</u> for helpful "How To" content.



Troubleshooting Tips

At some point, you'll run into something strange. We're the first to admit that JTAGbased run-control and trace are not always deterministic. JTAG is a 30-year hardware protocol, and when something goes astray at a very low level, SourcePoint tries to (but sometimes doesn't) recover gracefully. There will be times that the board will power cycle on its own. Or the firmware thinks that a thread is running but gets out of sync with the SourcePoint software, which thinks it's halted. Or the DbCStatus.exe ball stays red instead of turning green, while you swear you have a good DbC connection. Sometimes you have no choice but to quit SourcePoint and power cycle the target. That usually clears up the one-of's. But if the issue is repeatable, we ask that you collect as much information as you can, and open a ticket with us at <u>https://www.assetintertech.com/support/</u>. We'll respond as soon as possible.

In the meantime, here are a few errata that we've noticed on the UP Xtreme i11, and the steps needed to mitigate.

Firmware gets out of sync with software

On the host PC using DCI, functionality is roughly partitioned between software (SourcePoint application with its GUI) and firmware (lower-level run-control primitives). Broad-brushing it, SourcePoint software on the host communicates with the firmware, that encapsulates JTAG traffic into packets which are sent to the PCH, which in turn performs the JTAG mastering function.

Somewhere along the line, the firmware may get out of sync with the software. You may see symptoms like:

In the Viewpoint window, the threads are shown as Running, whereas the Status Bar at the bottom right shows Stopped.

P0 in the Viewpoint window is Running, with one or more threads below it are in the Stopped state.

If this happens, you'll likely have to quit SourcePoint, kill the AssetDCI process (see below), power-cycle the target, then start over. Sorry. Then please enter <code>aalog = 20987</code> in the <code>Command</code> window, and try to reproduce. We're extremely interested in these cases, so capture the verbose logs in the <code>Log</code> window and send to us.

Trace buffer overflows

DCI traffic processing has its limitations. When you try to collect too much trace data, the trace buffer overflows, causing aberrant behavior.

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Although the trace data is highly compressed, some trace sources, in particular with AET, running through the Trace Hub can exceed the capacity of the USB 2.0 connection. In theory running at 480Mbps, in practicality SourcePoint can only process trace data at approximately 100Mbps. Beyond that, we collect ~ 20kB of trace data before a buffer in SourcePoint overflows, and we don't recovery gracefully.

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You'll see these symptoms of this occurrence in the SW/FW Trace window:

A few of these overflows are no big deal. But, if you're tracing a huge amount of data, SourcePoint may spin, as it tries to process all that data, and deal with the mess. Sometimes, after maybe a few minutes, it recovers. Sometimes, you end up in limbo.

The only solution at this point is to quit SourcePoint, do an End task on the AssetDCI Background process, power cycle the target, and start over:



File Options View Processes Performance App history Startup Users Details Services Name	Status	31% CPU 0%	84% Memory				
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Ultimately, we're working on improving the performing of the AssetDCI driver, and behaving more graciously when overflow is encountered. But, in the interim, it is key to ensure that the trace data collected is relatively "sparse". Focus your debugging in the specific area of interest. Don't try to collect all Port IN/OUT from reset through to the UEFI shell. At 750K I/Os per second, you'll swamp the host debugger processing, and you can't deal with all that data anyway.

Note that this only happens with AET – that is, you can only overflow by collecting too much AET data. It does not apply to LBR, SW/FW Trace, SVEN, or Intel Processor Trace. It may take some trial and error to limit the scope of your event data collection.

Intel Processor Trace – Slow!

When you configure Intel PT, you can specify the size of the buffer in system memory to collect trace data:



race Configuration				×	<
LBR BTS Trace	Hub AET	Intel PT	Intel PT	Memory	
Trace buffer					
⊖ Use processor se	ttings				
Use SourcePoint	settings:				
Base address:	10000000P		P		
Length per core:	16k 16k	~			
Trace capture mode	32k 64k 128k	_			
Overwrite	256k 512k				
() Append	1M 2M 4M 8M 16M 32M 64M 128M 256M 512M 1G				
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Note that Intel PT directs instruction trace data to system memory. Although highly compact and efficient, we are not streaming over DCI to the host in this case; we buffer the code execution data until the platform is halted, at which point SourcePoint uses JTAG over DCI to collect the trace data out of system memory, reconstruct and display it. JTAG operates at fairly low speeds, and for large buffer sizes the transfer of all that data can be slow. It starts to become noticeable beyond a buffer size of 64kB. If you try to collect 1GB of data from system memory over JTAG, you can enjoy a cup of coffee and cake while this is in process. SourcePoint will display as Not Responding, and you'll get the "grey screen" if you're too persistent. SourcePoint will eventually recover, but in the interest of time and frustration, it's probably best not to try to save huge collections of instruction trace. Focus your debug efforts in the vicinity of the bug.



My board is not booting – what now?

Once in a while, especially during an intense debug session, we have found that the target goes into la-la land. You get to the UP splash screen, and then it just stops. Or the screen stays black. SourcePoint run-control continues to work, but it won't boot all the way up to the UEFI shell. Quitting SourcePoint, unplugging the DCI cable, killing the AssetDCI process – all are good steps in this instance, when you need to recover.

But then, once in a while, you wait the needed 20 seconds; and it doesn't boot. The screen stays blank or frozen.

Don't panic! For reasons we're not sure of just yet, after about 60 seconds, the board "wakes up" and should boot all the way to the UEFI shell.

There's only one thing: it has gone back to the factory settings, so you need to reset the WDT timer, as per <u>BIOS Settings</u> section in this manual.

Then, you'll be back in business.



Conclusion

Thank you for getting this far! We hope that you have enjoyed the ride, and are using the power of SourcePoint successfully in your debugging and learning journeys.

Feel free to browse the SourcePoint Academy at <u>https://www.asset-</u> <u>intertech.com/sourcepoint-academy/</u> for helpful reference guides, help material and "how to" videos.

If you ever have any questions, please call, email or open a Support Case here: <u>https://www.asset-intertech.com/support/</u>. We'll be glad to help!

