# Eliminate Production Programming Frustrations

Use the Right Tool for the right job: Vivado for Development, ScanWorks for Production

BY Larry Osborn

Fast Flash Programming Technologies







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ASSET is a member of the Xilinx partner program, and one value ASSET provides is production test and programming solutions complementing Xilinx tools and supporting Xilinx silicon. As part of the partnership, we jointly support customers, so they are successful. As part of that activity, I have noticed many customers posting on the Xilinx support community struggles they are having trying to use Vivado/SDK/Platform Cable for production in-system programming. Xilinx clearly states those products are not intended for production use.

Due to seeing this issue again and again on the Xilinx community, I was motivated to understand the challenges engineers were having and show a better way to solve the issue. This eBook discusses the challenges and shows the better way to do in-system programming in production.

This eBook is to address what ASSET is seeing with our customer base that are trying to use Xilinx tools for device programming in a **production** setting. In 2021 I did a webinar <u>In-System Fast Flash</u> <u>Programming Technologies</u> on the need/impact of *fast flash programming* in system to address beat rate issues and other process management issues. In this webinar I programmed an QSPI device that was connected to the Zynq-7020PS and another QSPI device that was connected to the Zynq-7020PS and another using a direct connect method and finally a SD card. After speaking with a few customers, I got curious how the silicon vendors were programming devices in production. So, I embarked on a project to use the Zedboard from Avent and the tool chain from Xilinx (Vivado and SDK) with the Platform Cable to experience for myself what customers experience.

#### **QSPI-PS** Programming

Starting with the document "<u>Workshop for Beginners</u>" from Avent I was able to build a Vivado design using the Zedboard as the target. Then using the Xilinx SDK, I was able to build an application to program into the QSPI device on the Zedboard located at IC15.



Trying to use the Platform Cable I was surprised that the programming cable could only load bit files into the FPGA or load code into DDR. I then realized that the Xilinx method was to build a First Stage Boot Loader (FSBL) and adding the application to the FSBL. The FSBL did some DDR and QSPI initialization and then use the code within the ps7\_int code to program the QSPI from DDR. From a production perspective it is very dangerous to assume too much about the target status without first testing the fit and interconnects between the devices on the Unit Under Test (UUT). This Xilinx method for production programming would mean a change out of tools from test to programming as the Platform Cable is using the same JTAG interface likely being used for test. In production this change of tools would have a significant hit on the beat rate which would be unacceptable. With ScanWorks the switch from test to programming is simply a different action.

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Design: Zedboard		TCK Frequency: 30,000 MHz	Lindates Available
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		Compatible with Design? Yes	
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Action Name	туре	Test	
0) SPV1	Scan Path Verify	F	
1)SPI_PMOD_Flash	SPI		
2)SPI1_QUAD	SPI	Programming	
3)SPI DIO1	SPIDIO	Trogramming	
4)SPI Direct1	SPI Direct		
S)Load_SVF1_IC16_Short_Chain	SVF		
6)SPI_FLASH_Short_Chain	SPI		
7)Load_SVF_ICT6_SPI_FLASH_IP	SVF		
8)SPI Hash IP1	SPI Hash IP		
	Processor Past Programming		
93)Program SDMINC over Ethernet	Processor Past Programming		
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PPT Test TO     Program SDMMC over ITAG	Processor Fast Programming		
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Figure 2 ScanWorks Project for Test and Programming

All the JTAG controllers used in the ScanWorks platform can perform test as well as programming. A single connection and single tool for more efficient for production usage.





## QSPI-PL Programming

The next step was to add IP with Vivado in the design for the AXI Quad SPI interface and do some configuration to program the QSPI device connected off the PL. Adding the AXI Quad SPI interface to the design was straight forward and then adding the constraints to handle the connections between the pins of the FPGA bank and the PMOD header was quite easy.



Figure 3 Vivado Project with AXI QUAS SPI IP Block

The data for the constraints is driven by the Zedboard schematics. The Digilent PMOD SF3 32MB NOR Flash uses a N25Q256A SPI device from Micron. This device supports both dual and quad protocols. With the design built and verified, at this point I couldn't see how to program this device unless the Platform Cable had that ability built within. After a call to support, I was informed that a need to write the programming code but, there was an example program that would work. With help from support, they showed me where the code was located and how to include it in the SDK project. Then after building the project and executing it, the programming example failed. Then I was pointed to a reference manual to develop the code.

I used the SDK debugger to only find that the initialization had failed but, there were no error message in the code or clue as to what was causing the failure. During the debug execution, stepping the code behaved badly as the stepping was not in a predictable sequence based upon the source code. This leads to questions about the build and digging further into this issue was not an acceptable use of time.

For ScanWorks the programming of the N25Q256A was a matter of using FPGA Fast Programming action to create the SPI programming bitstream image and program the FPGA. Then run a second action pointing the flash image source and preforming the programming . In the <u>video</u> there are two methods





used to program this flash device connected on the PMOD interface. The first is using short chain (detailed in the video at 26:20) where the JTAG chain of the FPGA is shorted from 100+ cells to just 8 cells. As we are using JTAG to program the device shortening the scan chain increases the programming throughput. The second method is similar to Vivado except we provide the SPI programming IP that does the actual programming of the flash device. This is covered in detail at 29:30 of the <u>video</u>.

Southeast Pr. Cethoant, Sample Prect. CSI. Jeaboard Project: PFX, Zedboard_Example_Project_IC35 Design: Zedboard Projects Designs Actions Sequences Create C. Ananon @ Build		CK Frequency: 30.000 MHz         IP Address: 192.168.1.00         Compatible with Design?         Yes         Status       Notes         Mappings       Reports	Image: Second
	Search:		
Action Name	туре		
O) SPV1	Scan Path Verify		
1)SPI_PMOD_Flash	SPI		
2)SPI1_QUAD	SPI		
3)SPI DIO1	SPI DIO		
4)SPI Direct1	SPI Direct	Shart Chain	
5)Load_SVF1_IC16_Short_Chain	SVF	Short Chain	
6)SPI_FLASH_Short_Chain	SPI		
7)Load_SVF_IC16_SPI_FLASH_IP	SVF		
8)SPI Flash IP1	SPI Flash IP	CDI Flack ID	
91)Program QSPI Flash over Ethernet	Processor Fast Programming	SPIFIASHIP	
93)Program SDMMC over Ethernet	Processor Fast Programming		
9_Program_QSPI_Flash_via_JTAG	Processor Fast Programming		
Ethernet Loopback	Processor Functional Test		
PFT Test IO	Processor Functional Test		
Program SDMMC over JTAG	Processor Fast Programming		
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Figure 4 ScanWorks with Short Chain and SPI Flash IP





After hitting a dead end with programming, using Vivado/SDK with the flash device that was connected to the PL. I examine the possibility of programming the same device via a direct method of just using the Platform Cable. I found no way to accomplish this. This is however possible with the ScanWorks. Below is a picture of the target connection using Direct connect. This is also covered within the video.



Figure 5 Zedboard with ScanWorks Direct Connect SPI Flash

## SD Programming

Moving to SD programming in the exercise provided in the Avnet Workshop for Beginners the method described for using the SD card for autonomous booting was to create a FSBL with a boot image then copy the files generated to the SD card on the PC. That's not programming the SD card from a production perspective. So, I started my search to see if the PS was configured for the use of the SD card. Below is the PS7 IP block diagram which shows SD0 is enabled.







Figure 6 ZYNQ7 with SD0 enabled

And the MIO mapping had been configured.





Re-customize IP									×
<b>ZYNQ7 Processing Sy Documentation</b>	y <b>stem (5.5)</b> sets 🗁 IP Location 🂠 Imj	port XPS Settings							4
Page Navigator	MIO Configuration						5	Summary Re	port
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Figure 7 SD 0 MIO Configuration

Then I searched for some example code or guidance on how to program the SD card. The search resulted in finding nothing. My assumption is that the Xilinx approach was documented in the Avnet example which is not acceptable for production.

Within the ScanWorks platform there is built-in capability to program the SD Card or eMMC devices. In this case the programming code is not via the FPGA but rather through the processor. The code is loaded in the OCM, and we also enable the use of the Ethernet on the Zedboard to provide a high-speed data pipe for the flash image. Thus, we run a processor speed and without DDR for an extremely high rate of programming throughput. This method allows for the programming eMMC devices in a production setting.







Figure 8 ScanWorks PFx with SD/eMMC Programming

## Summary

After weeks of effort to get a grasp on what issues customers might be seeing while using the Platform Cable and the tool chain (Vivado and SDK), I can see why customers are struggling to use this tool in production. However, in the documentation for the Platform Cable, it clearly states that the tool should only be use in a **Prototype environment**. To Xilinx credit there is tons of documentation. It is a challenge to find what documentation is appropriate for the task of simply programming a UUT. Again, the Xilinx tools are designed for FPGA developers not for production test engineers. Test engineers need tools that focus on test engineering roles and responsibilities and ScanWorks is designed for that engineering sector.

I found using the combination of Vivado and SDK user interface too complex to address the needs of production. I realize that development engineers would provide the FSBL with the attached application that could do the programming but, as stated earlier it is too presumptuous to assume the health of the target to be fully operational. I also found that it is possible to have a design rebuilt and without moving the design into the SDK workspace you can build a boot loader with the wrong design and not be aware. There are more detail findings in the white paper "A Users Perspective of Using Xilinx Vivado in Production for Programming"





Overall, the Xilinx tools are not intended for production usage but, they do a great job in address in the needs of the FPGA designer that is using Xilinx silicon.



