Squeezing Out More Test Coverage:

Bridging the Gap Between

Boundary Scan and Functional Test

Quality

Coverage

100%

Functional

Component

Boundary Scan
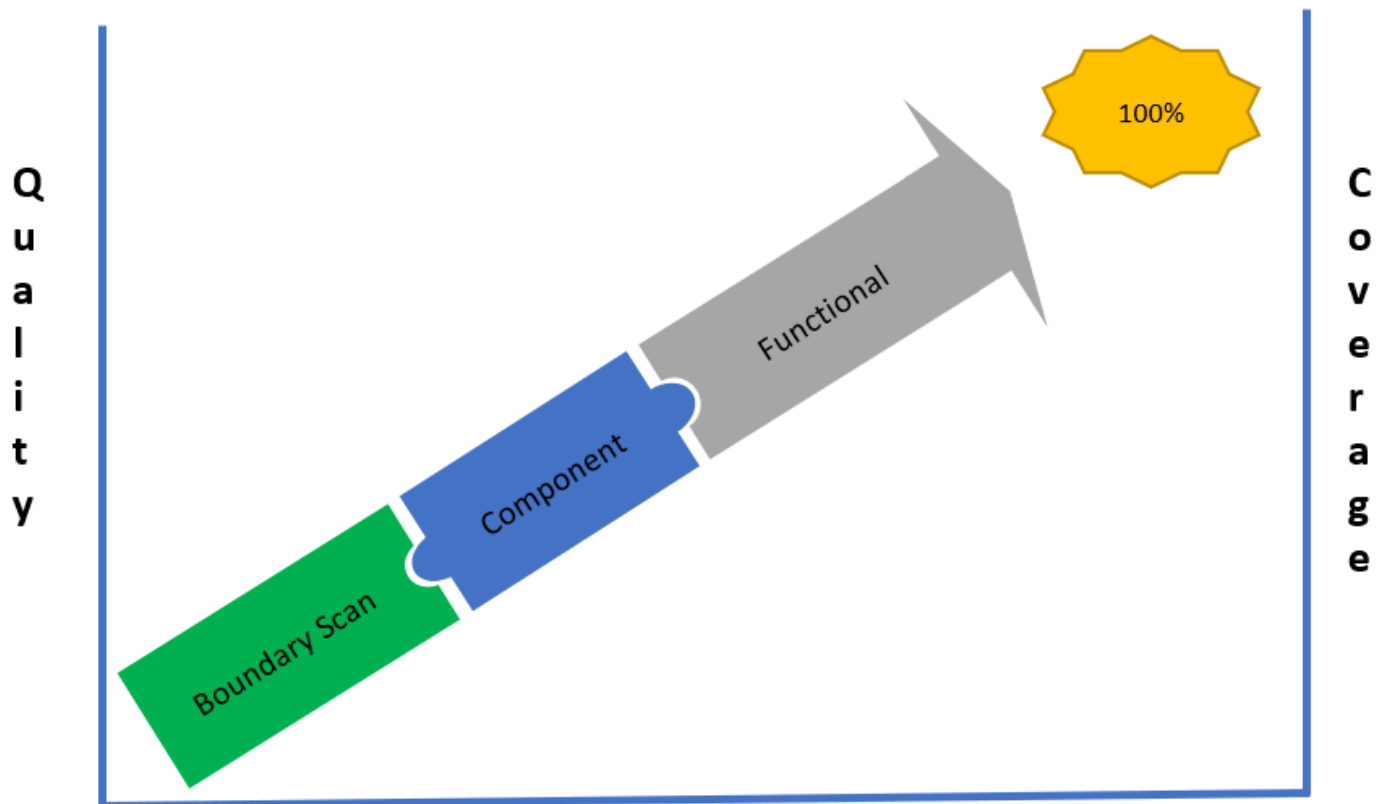
ASSET™

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Michael R. Johnson serves as Product Manager for ScanWorks Boundary Scan Test (BST) for ASSET InterTech. He also serves as manager of ASSET's Application Engineering organization. As Product Manager, Michael is responsible for providing strategic direction to ASSET's ScanWorks Test Platform by listening to customers and working with cross-functional teams to deliver solutions to meet their needs.

Prior to joining ASSET in 2007 as a Sr. Applications Engineer, Michael's background included roles as a Cellular System Engineer with Nortel Networks and a Hardware Design Engineer with Alcatel USA. While at Alcatel USA, Michael's emphasis was printed circuit board design and layout for high-speed digital cross-connect and fiber-optic systems.

Michael earned a Bachelor of Science degree in electrical engineering from Southern University and A&M College located in Baton Rouge, Louisiana, and a Master of Business Administration with an emphasis in strategic leadership from Amberton University located in Garland, Texas.

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Executive Summary

In today's electronics market, the speed and effectiveness of product testing have a significant impact on a product's overall quality, cost, and time-to-market. All printed circuit board (PCB) manufacturers and test engineers would like to have 100% test coverage of their PCBs, but is this level of test coverage achievable? And if so, at what cost? In the manufacturing test environment, time is money, therefore, manufacturers must make decisions on how much of each they are willing to invest to ensure a quality product.

Multiple test methodologies applied to the PCB have traditionally been used to ensure the highest level of test coverage obtainable. With advances in IC technology, test methodologies that provided adequate test coverage in the past have diminished in overall PCB test value. These test methodologies are primarily intrusive in nature. As a result, non-intrusive board test (NBT) methodologies have become increasingly popular. NBT methodologies integrate several, software-driven, test methodologies to restore test coverage lost due to diminished printed circuit board (PCB) physical access and reduce cost where intrusive methods are still used.

Boundary scan test, one of the software driven NBT methodologies, has increased in popularity across the PCB test industry. Boundary scan instrumentation within semiconductor devices is used to verify register operation and perform PCB structural testing. As boundary scan technology has matured, it is now used for device configuration and programing along with device functional testing.

Boundary scan can test and validate a broad range of device types on PCBs, however, there are device types that may be excluded from testing due to complex testing algorithms. Consequently, PCB coverage gaps could exist with some devices going untested. To bridge the test coverage gap, end users develop custom scripts to access these devices to apply functional test algorithms via the boundary scan infrastructure. ScanWorks users can bridge the coverage gap between boundary scan and functional test via its Component action. This action allows for testing of non-boundary scan devices, such as analog to digital converters (ADCs), digital to analog converters (DACs), Ethernet PHYs, LED, switches, clocks, and other non-boundary scan devices through the PCBs boundary scan infrastructure.

Coverage Assessment Methodology

When asked, engineers will say that the goal of a test plan for a PCB is 100% test coverage. When pressed further, they admit 100% test coverage is virtually impossible to achieve. The real goal becomes optimum test coverage, which can be thought of as the maximum test coverage achievable given a set of restraining factors, most often cost and time.

Cost is at the top of the list of restraining factors. Usually, an optimum test strategy boils down to achieving maximum test coverage at an acceptable cost level (Figure 1). Since no one technology can achieve 100% test coverage on its own, optimizing a test plan for a particular PCB consists of assembling the right combination of methods and technologies so costs are minimized, and coverage maximized.

Figure 1: Coverage Optimization

Why should PCB manufactures strive to optimize PCB test coverage? Striving for optimum PCB test coverage is imperative to improving manufacturing yields and product quality, reducing product returns, and enhancing the marketplace competitiveness of the product. The prime reasons for a test strategy are

to find defects, diagnose the cause of the faults, and repair them quickly. Of course, fault data then must be used to constantly improve the processes that produced the PCB and the faults in the first place.

This feedback loop will drive down metrics like defects per million opportunities (DPMO). As an effective test plan causes DPMO to drop, yields on PCBs increase so that a higher percentage of the assembled boards moves from assembly to final system integration. In many cases, achieving an optimized test plan may require adding capital investment in equipment. But this cost should be balanced against the cost-of-test for the life of the product. Amortizing test equipment costs over a products entire life cycle often reveals that the real return on investment can be high and the payback of its procurement cost very rapid.

Along with the cost of additional or incremental test capabilities, there are additional considerations before a test plan can be finalized. For example, what are the capital assets such as test hardware and software that already are in place? Moreover, test equipment that requires a long development cycle might jeopardize the products production schedule. In a manufacturing environment, beat rate, or the rate at which finished products must be produced, usually is of paramount importance. A critical factor in maintaining the necessary beat rate often is production line balancing. In a balanced production line, a PCB will move steadily down the line, avoiding any prolonged stop at any one test station. If a specific defect can be detected at any of several test stations, the station with the shortest test time should be assigned to cover that defect to achieve a better balance.

Product-specific factors also must be considered. The unit volume over the projected life cycle of the product, for example, will affect acceptable yields. High-volume, low-cost assemblies can be more tolerant of poorer manufacturing yields while low-volume, high-cost PCBs require very high yields. Of course, the testability of a design, or how much testability was designed into the PCB, also will determine the test tactics that can be applied to the assembly.

Achieving Optimum Test Coverage

Because every test technology/methodology has a finite limit on the coverage it can provide, optimum test coverage usually is achieved through a combination of several technologies. The strengths and weaknesses that are unique to specific test methodologies steer each technology to a certain role in a PCB manufacturing environment. Broadly speaking, contemporary electronic test performs several distinct functions including process monitoring and structural test, electrical structural test, and functional test (Table 1).

Table 1: Test Functions - Test Technologies/Methodologies

Test Functions	Test Technologies/Methodologies
Process Monitoring and Structural Test	Automated Optical Inspection, Automated X-Ray Inspection, Manual Visual Inspection
Electrical Structrural Testing	In-Circuit Test, Manufacturing Defects Analyzer, Flying Probe Test, Boundary Scan
Functional Board Test	System Mock-Up, Self-Diagnostics, Instrumentation, Simulation, Emulation, Test Executives, Rack-and-Stack, PXI/VXI
Opportunities for Combining Test Methodologies	ICT and JTAG JTAG and Processor Emulation JTAG and Flying Probe Test JTAG and Functional Test

The most prevalent technologies that make up many test plans include automatic optical inspection (AOI), automatic X-ray inspection (AXI), digital multimeters (DMM), manual visual inspection (MVI), in-circuit test (ICT), manufacturing defects analyzers (MDAs), flying probe test (FPT), boundary scan/JTAG test, and processor emulation. Several of these technologies, such as JTAG and ICT, or JTAG and processor emulation also can be combined in one test station, reducing the number of distinct stations and the complexity of the setup. Functional test may require several technologies. System mock-ups, self-diagnosis, instrumentation, simulation, emulation, test executives, and others are methodologies frequently applied in functional test.

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iNEMI PCOLA/SOQ/FAM Framework

"Structural test" is often defined as verification of an assembly process by testing each of its smaller elements and their interconnects. Structural test tools include AOI, AXI, DMM, MDA, ICT, JTAG, FPT, and others. AOI and AXI are inspection tools as opposed to test tools as they use visual technologies. DMM, MDA, ICT, JTAG and FPT use electrical test technologies to perform their functions. Although these technologies are often evaluated in terms of their "shorts and opens" detection capabilities, it's important to consider that they must also verify the "rightness" of the components on a printed circuit assembly.

When discussing "structural test coverage", we look for a way to deterministically express the fault detection capabilities of a test methodology on a given PCB design. The categorization of structural defects for devices and interconnects can be articulated using iNEMI's PCOLA/SOQ approach displayed in the Component Scoring and Interconnect Scoring Guidelines (Table 1 and Table 3).

Table 2: Component Scoring Guidelines

P	Presence	Does the test determine the presence of the part?
C	Correctness	Does the test determine that it's the correct part?
O	Orientation	Is the part oriented properly or is the polarity proper?
L	Live	Is the part electrically functional for basic activity?
A	Alignment	Can the test determine lateral displacement or minor rotation?

Table 3: Interconnect Scoring Guidelines

S	Shorts	On an interconnect, can shorts within a shorting radius be detected?
O	Opens	If there is an open on the pin/trace will there be a test failure?
Q	Quality	Is the quality of the solder, wetting, and general structural integrity of the circuit board sufficient?

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So, the test coverage of a given structural test methodology (which itself consists of one or more structural test tools) can in principle be determined by looking at a PCBs parts and pins and filling in the blanks for PCOLA/SOQ. The higher the number, the higher the test coverage. Appropriate weighting can be added for "critical" devices or interconnects.

Structural test, in and of itself, does not constitute a complete test methodology. It is entirely possible that the PCB is structurally sound, but it does not function. This is of course where functional test comes in. Functional test provides verification that a design will perform its designated function. It is far more subjective than structural test in that it is extremely difficult to verify the complete functionality of a complex electronics system in all conceivable operating conditions.

Functional test methodologies vary substantially from product to product and company to company. For example, on a low-end cell phone, functional test may consist simply of turning the phone on and verifying its ability to receive a call. There may be no structural test applied to a system like this at all. On the other hand, a high-end wireless base station may be subjected to a comprehensive battery of functional tests.

These tests may verify not only that the system is working properly but may also stress it to evaluate its performance under load and its conformance to whatever industry specifications govern its operation. Such performance and conformance tests are primarily applied in a system's design validation at prototype stage, but some OEMs will apply these test technologies in the manufacturing process as well to ensure the utmost in quality. To capture test coverage metrics from functional tests, iNEMI in 2009 introduced the FAM defect categorization in Table 4.

Table 4: Functional Scoring Guidelines

F	Feature	Can presence or absence of a feature be detected?
A	At-speed	Can the pin/interface/feature be tested at min/mid/max speeds?
M	Measurement	Can a measurement be taken that confirms performance to a BER, CRC or another requirement?

So put together, PCOLA/SOQ/FAM represents a comprehensive expression of the amount of coverage obtained through a combination of structural and functional test technologies.

Put another way, PCOLA/SOQ/FAM scoring articulates a test engineer's defect capture probability. Deterministically, any defect which escapes the factory will be due to a test strategy which is incapable of detecting that fault on the affected part(s) and pin(s). Since it is impossible to create a test strategy which will capture every conceivable fault for every possible permutation of temperature, voltage, process, and operating conditions, it's the test engineer's responsibility (and some would say, art) to achieve the maximum test coverage at the lowest possible cost.

Functional test technologies can in fact contribute to the structural PCOLA/SOQ score for a given board design. Hook up, for example, an IP traffic generator/analyzer to a router and you'll probably find out quickly if there's a short circuit anywhere on one of the data lines of the routing silicon, control plane processor, PHYs, or other parts.

Symptoms will of course vary depending on the nature of the defect and the test: maybe there's packet loss, or packet latency is high, or there's lots of jitter. So functional test technologies have the advantage of contributing to both the FAM and the PCOLA/SOQ metrics for test coverage.

But the limitations of conventional functional test lie in diagnostics. As described above, a structural defect may manifest itself in a gross failure in system operation. There is no way that the traffic generator/analyzer can correlate packet loss to for example an open circuit on device U24 pin 87. Its test coverage may be high (which is good – a fault can be discovered by the OEM and not by their customer) but its diagnostic granularity is low (which is bad – the OEM cannot determine the root cause of the failure and take corrective action, which means the board goes into the "bone pile").

In an era of diminishing test coverage from structural test technologies such as ICT, and faced with inadequate diagnostics from traditional functional test, what is a test engineer to do? The answer lies in embedded instrumentation within silicon. A functional test using the Component action technology leverages the embedded instrumentation to perform register tests and exercise non-boundary scan

devices and buses. The low level of such tests can in most cases indict faults to the defective parts, nets and even pins.

Ultimately, embedded instrumentation-based technologies will replace the test access lost by legacy structural-only testers, and at a much lower cost. And, because on-chip instruments can exercise their connections functionally, they provide the bonus of FAM coverage in additional to PCOLA/SOQ. With high test coverage, excellent diagnostics, and lower cost.

Bridging the Gap with the Component Action

Combining boundary scan and functional test address specific aspects of the iNEMI framework. Boundary scan addresses the structural faults that could result during manufacturing but how can functional testing be accomplished during the same session? Functional testing can be accomplished with use of the Component action. The Component action is a general-purpose action that extends functional test coverage to a wide array of non-boundary scan devices. The Component action addresses the functional, at-speed faults that might be seen during actual PCB use.

The advantages of combining the two methods within a test system are:

- Reduction in process steps and simplified product flow
- One-stop for structural and functional testing, and in-system programming
- Saving of factory floor space
- Reduced training requirements for test personnel with a uniform user interface

Though distinct and complementary in purpose and methodology, the two techniques, boundary scan and functional testing, can be combined with great effectiveness. Use of the Component action enables boundary scan to be used as a functional test solution for non-boundary scan devices.

After the boundary scan applications are implemented, the test management software, in this example ScanWorks, would proceed to the Component actions in a pre-determined order and sequence. These Component actions could perform functional tests such as temperature measurements, toggling LEDs, testing edge connectors, verifying the presence of clocks or reading the outputs of ADCs or DACs.

Component Action Facts

The Component action is based on the Test Command Language (Tcl) pronounced "Tickle" language. This language was chosen because of its universal knowledge by engineers. This language is easy to learn. Since Tcl is a compiled and interpreted language, an interpreter and compiler are needed. The Tcl interpreter and compiler are installed with ScanWorks. With the Tk package, also installed with ScanWorks, creation of dialogs and GUIs are capable. These dialogs and GUIs can be used for operator input. All response become a part of the overall report.

Component models define the pins on the target device that require boundary scan access. Tcl models are created based on the operational algorithms of the non-boundary scan devices. Models are reusable from design to design. The Component action uses the Tcl model along with the PCB netlist to access the underlying boundary scan resources.

The Component action creates an environment for easy access to device I/O pins to create functional test of non-boundary scan devices. Any non-boundary scan device that is accessible through a boundary scan device, and has an algorithm that can be modeled from its data sheet through Tcl, is a candidate for functional testing by the Component action. A few built-in base commands are available to the end user. See the model structure below. Some Component action models are provided in <ScanWorks install directory>\Libraries\asset\ComponentModels directory that could be used as-is or as template to create other models. (Figure 2).

```
Modelname.tcl

proc loadComponentActionSupport {} {
  set ::auto_path [linsert $::auto_path 0 $::env(ASSET)\\ComponentActionSupport]
  package require componentActionSupport
}

proc Build {vectorFileName}{
  set returnValue 0
  set f [open $vectorFileName "w"]
  puts $f "VECTOR busName busPins"

  close $f
  return $returnValue
}

proc Run { projectName designName actionName} {
  set returnValue 0
  puts "In the Run procedure"
  loadComponentActionSupport
  itcl::local componentAction ca $projectName $designName $actionName

  <a combination of commands to test the target device>

  < a 0 value is interpreted as a Pass and a non-zero value is interpreted as a Fail>
  return $returnValue
}
```

Figure 2: Component Model Structure

Functional Test Examples

The following are examples demonstrating how the Component action can be utilized for PCB functional verification.

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LED Verification

LEDs and LCD displays can be included as PCB functional test (Figure 3). The proper operation of these devices can be observed by an operator or optical sensing equipment. GUIs can be created using Tk which require operator input to confirm identity and confirm the devices passed. The operator input becomes a part of the overall PCB test report.
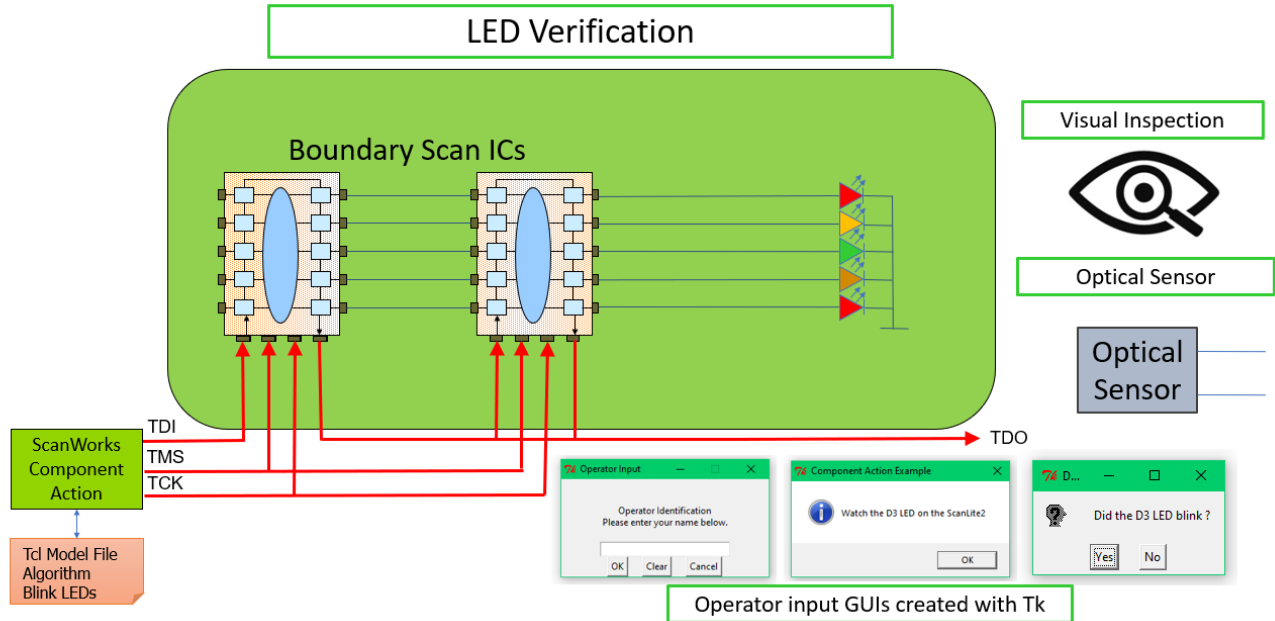

Figure 3: LED Verification

Connector Verification

Opens through a connector can be tested using a Component action (Figure 4). By placing loopback wires on individual pins on the connector, a stimulus can be driven out on one connector pin and captured on another connector pin. If the boundary scan device has bi-directional cells, a stimulus can be driven out of the output cell and captured on its input cell. In both scenarios, the output stimulus driven out must match the input stimulus captured. Diagnostic messages can be implemented within the Component action model script to identify the connector and pin should a short or open be detected.
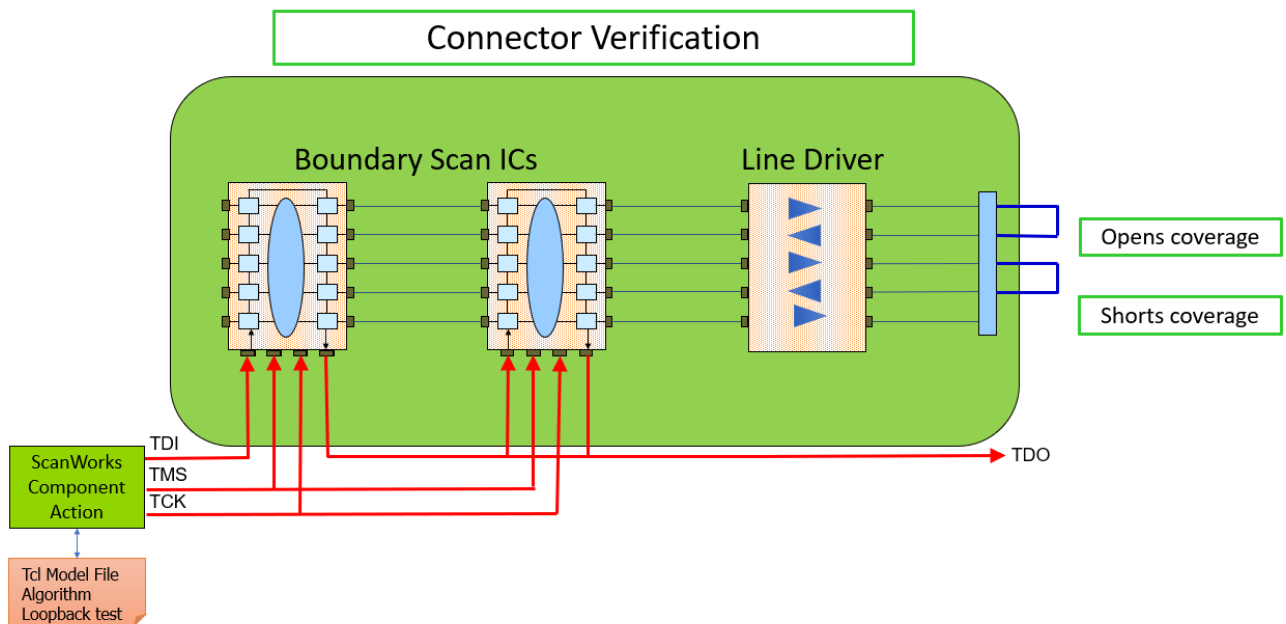

Figure 4: Connector Verification

Clock Verification

Clock signals can be tested with boundary scan as to whether the clock is active or not. Boundary scan cannot measure the actual clock frequency (Figure 5). Using a Component Action with the oscillator as its target, a boundary scan pin connected to the output of an oscillator clock signal samples the output a specific of times. The Component action is written to capture a specific number of signal changes (e.g., transitions from logic high to logic low) within a certain number of loops. If the clock signal does not change states, the model can be designed to display an error message which will be included in the overall Component action report.
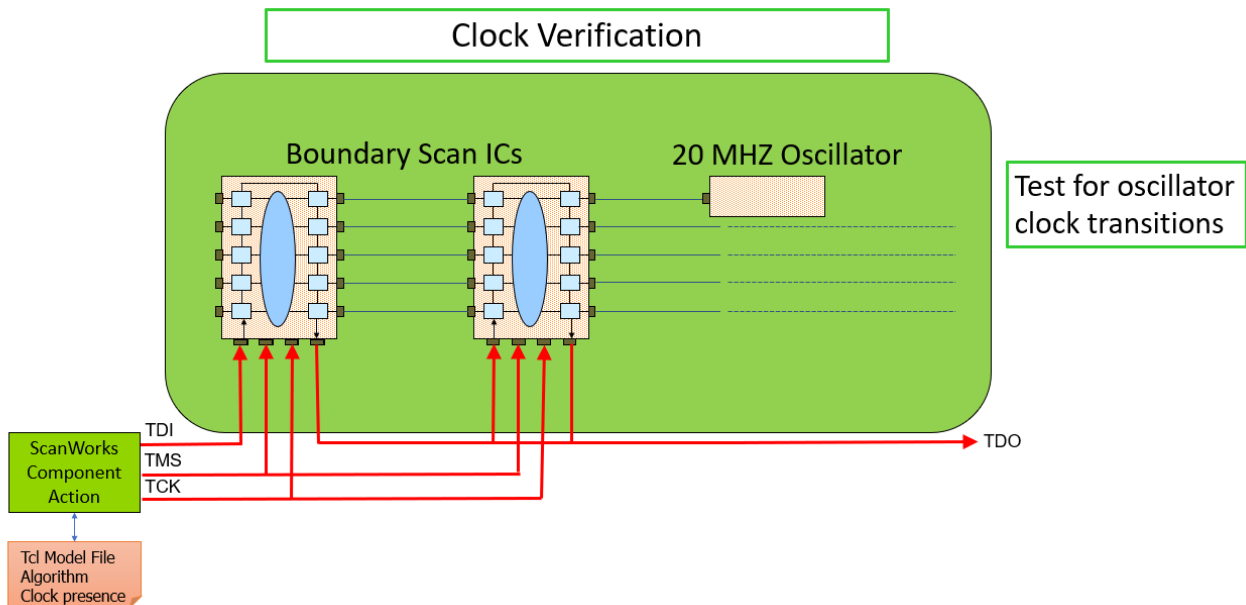

Figure 5: Clock Verification

ADC with Temperature Measure

ADCs can be found on a variety of PCBs across a broad range of industries. ADCs convert a time varying signal into a digital value. In the application pictured, the output of two temperature sensors is measured. The device temperature sensor measures the temperature near device U2. The ambient temperature sensor measures the temperature of the environment in which the PCB is placed. The Component action can be placed in a loop to measure and report the temperature at both locations. Should a pre-determined difference between the device temperature and ambient temperature be reached, a message can be output to the test operator (Figure 6).
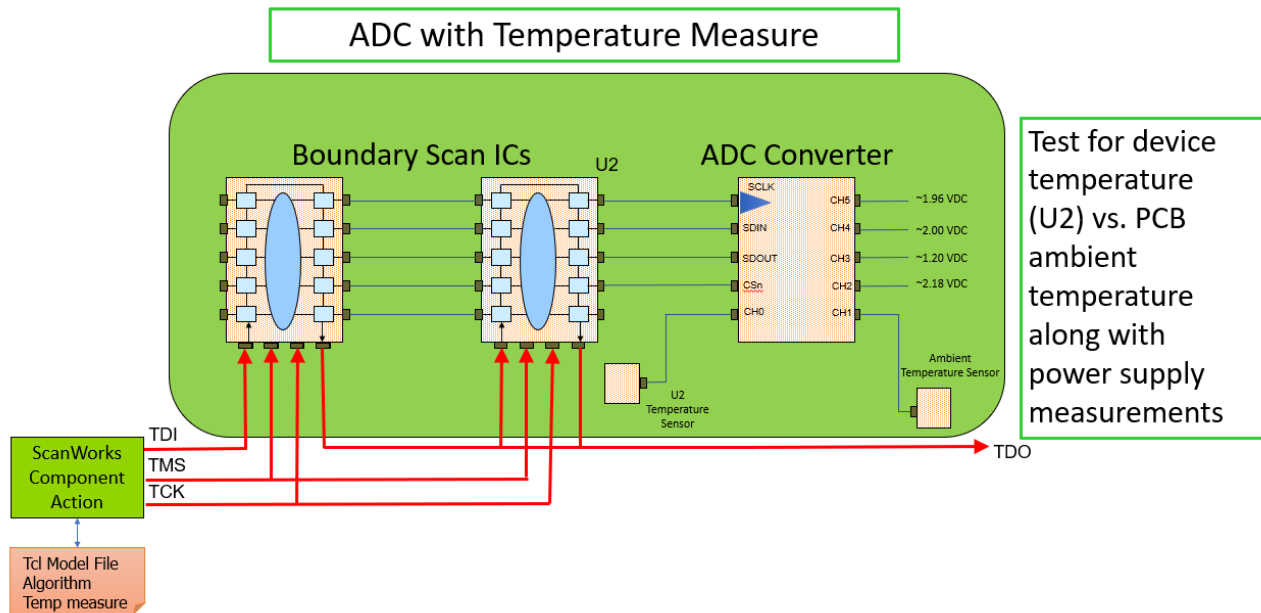

Figure 6: ADC with Temperature Measure

Summary

Bridging the boundary scan and functional test gap using the Component action has many positive results:

- Adding functional testing to areas of the PCB that might have gone untested can uncover defects that may have gone undetected
- One station for structural, programming, and functional testing reduces PCB handling and shortens time-to-market
- Combining boundary scan and functional test reduces the need for large equipment saving factory floor space
- Increased ROI per PCB reduces overall PCB manufacturing cost
- Failing devices are identified during manufacturing where the cost to repair is lower as compared to latter production phases or at product release
- Functional test actions can be implemented through 3rd party applications such as LabVIEW, TestStand, along with others
- Using a well-known test language, Tcl/Tk, engineers are able develop models targeting non-boundary scan devices
- ASSET provides a library of Component models for use as-is or as templates for model development so it's easy to get started

All test engineers want to increase PCB test coverage. Squeezing out that last ounce of test coverage can mean the difference between a quality product that performs flawlessly with no defects and a mediocre product with many flaws creating dissatisfied customers. Utilizing the power of boundary scan and the Component action for functional device functional test can achieve these results.

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