Real Insight from Code to Silicon

SourcePoint™ ScanWorks®

In-System Fast Flash Programming Technologies

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Project Manager for:

ScanWorks FPGA-Flash Programming
ScanWorks Processor-based Fast Programming
ScanWorks Embedded Diagnostics
SourcePoint Intel/AMD Debugger

June 29, 2021

Agenda

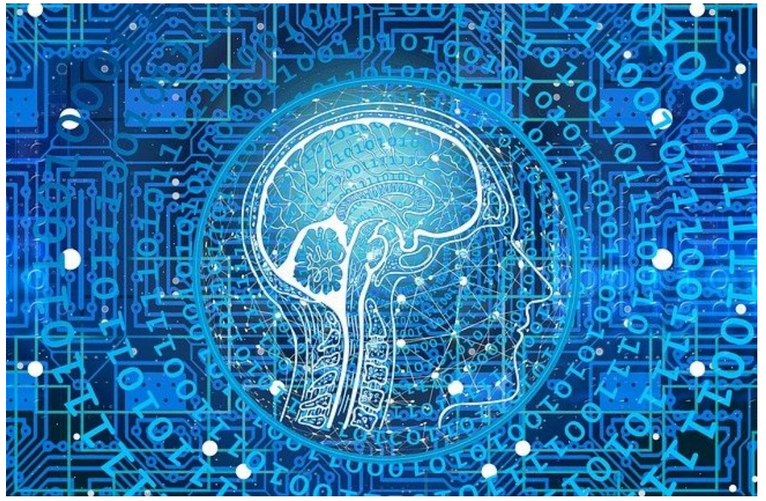
- Offboard vs. Onboard
- Technology Trends
- ScanWorks Addressing the Trends
  - Technology Trends
  - SoC Trends
  - FPGA Trends
- ScanWorks Programming Toolbox
  - Boundary-Scan Flash
  - Processor-based Flash
  - FPGA-based Flash
  - Controller-based Flash
- ScanWorks Programming Methods
  - Programming Method Considerations
  - Speed Comparisons
- Demo
  - Zedboard
    - BST
    - PFx
    - FFP
- Questions

Offboard vs. Onboard

- Offboard (preprogramming)
  - Inventory management
  - Engineering Change Orders (ECO)
  - Software updates
  - Device shortages
- Onboard (in-system programming)
  - No Inventory management issue
    - Preprogramming
    - Device Inventory shortage
  - ECO minimal impact
  - Software updates expected
  - UUT design dictates
    - Manufacturing beat rate
    - Speed of programming possible

Technology Trends

- Market Trends
  - Design starts
    - Artificial Intelligence
    - 5G
    - Defense - towards FPGAs for Cyber Security issues
    - Automated Driving Solutions (ADS)
    - Hyperscale Data Centers (HDC)
  - Domain-specific architectures (DSA)
  - Adaptive Computing
  - Prototyping



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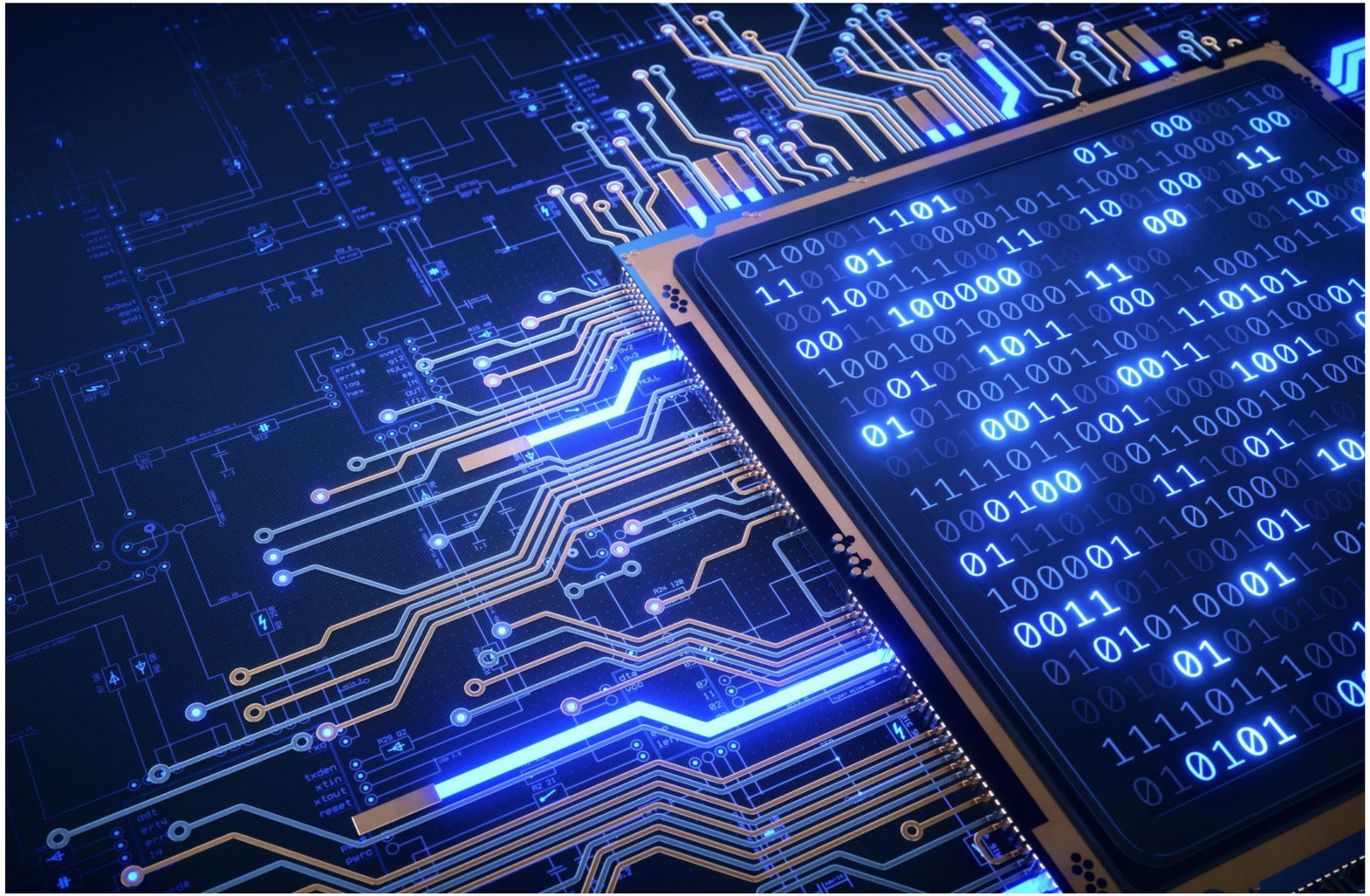
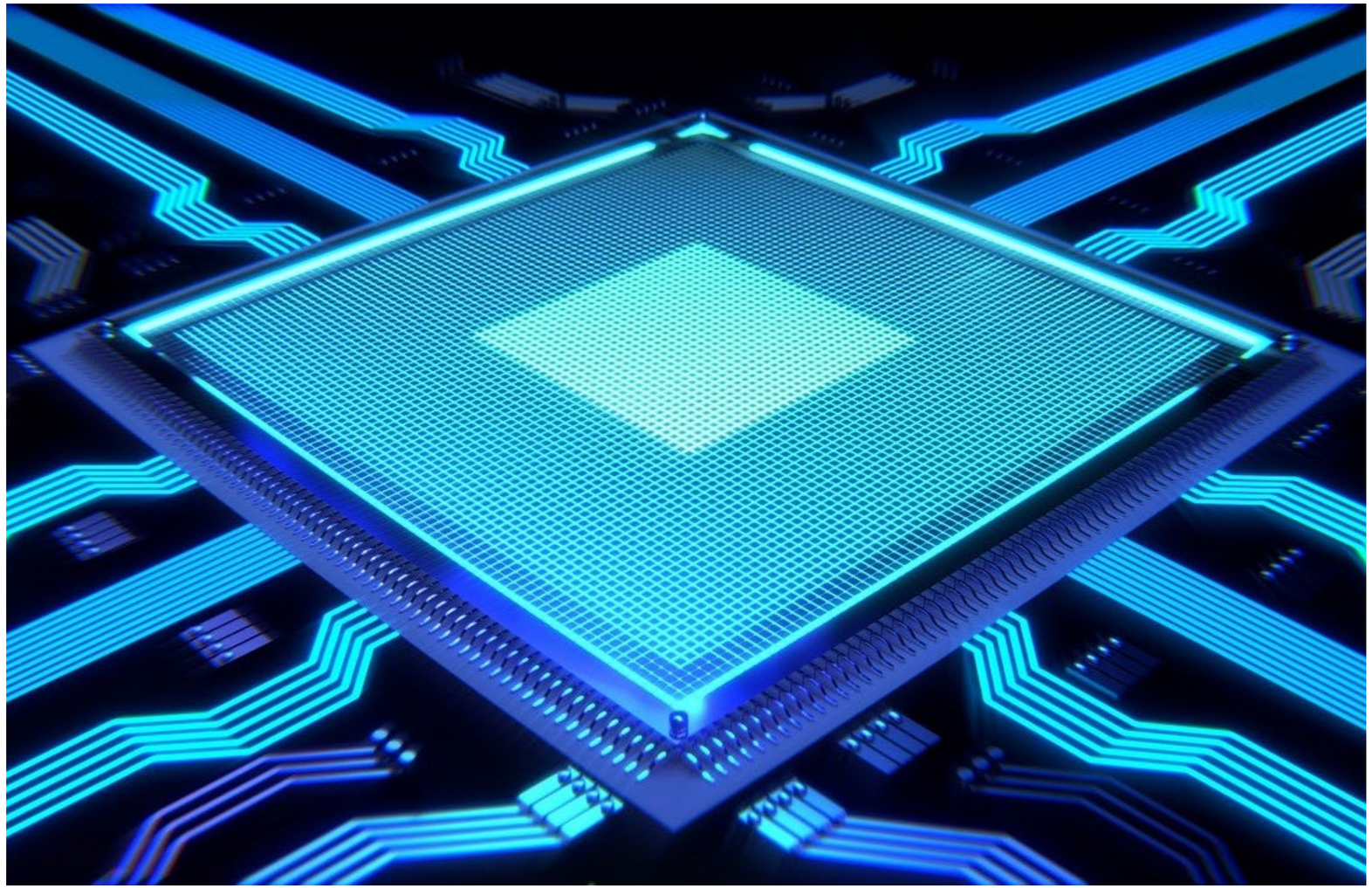
SoC Trends

- Multi-core
  - Homogenous
  - Heterogenous
- Additional cores
  - FPGA
  - GPU
  - Embedded Controllers
- Flash expansion
  - G-bit SPI support
  - SDMMC/eMMC
  - NAND



FPGA Technology Trends



- FPGA Complexity Growth
  - 9 Million System Logic Cells
  - 2,072 User IO Cells
  - 80 28G Transceivers
  - UltraRAM
  - High Bandwidth Memory (HBM)
- Power consumption
- Adaptability curves

Programming Methods

Customer Design Dictates Fast Flash Programming methods possible.

Programming Methods Consideration

Where is the flash device connected SoC, FPGA, Processor or JTAG only?

For the **SoC** that has both a processor core and FPGA core, is the flash device connected to processor core or to the FPGA fabric?

For the **FPGA** is there a system clock?

- System clock should run faster than sclk
- Instrument for Configuration SPI require special notation for pin assignment.

What is the **BST** chain clock rate? Slowest device clock rate in the chain determines the chain clock rate.

How large is the image?

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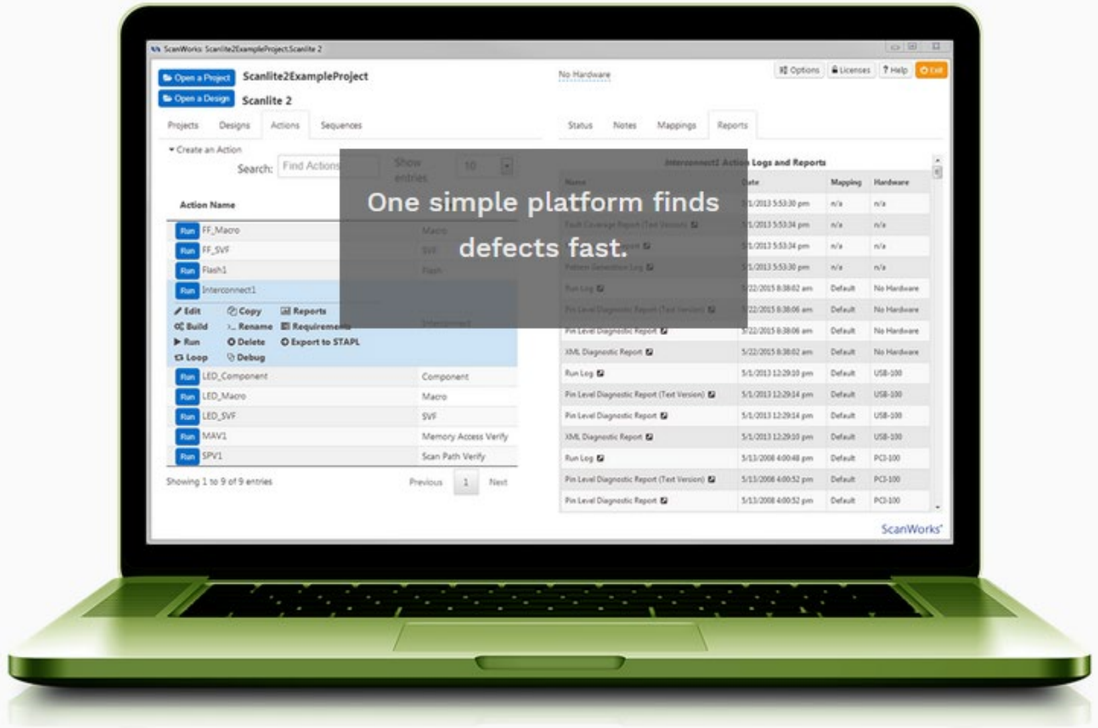
Programming Toolbox

ScanWorks

- Boundary-Scan Test (BST)
- Processor-based Fast Programming (PFP)
- FPGA-based Fast Programming (FFP)

ScanWorks Boundary-Scan Test (BST)

- Design to simplify the test complexity
  - Automated
  - Model-based
  - Incremental test
- Programming support via JTAG
  - SPI, QSPI, OSPI
  - I2C, NAND, NOR
  - eMMC



Board
Structural Defect Detection
Opens/Short
Interconnect

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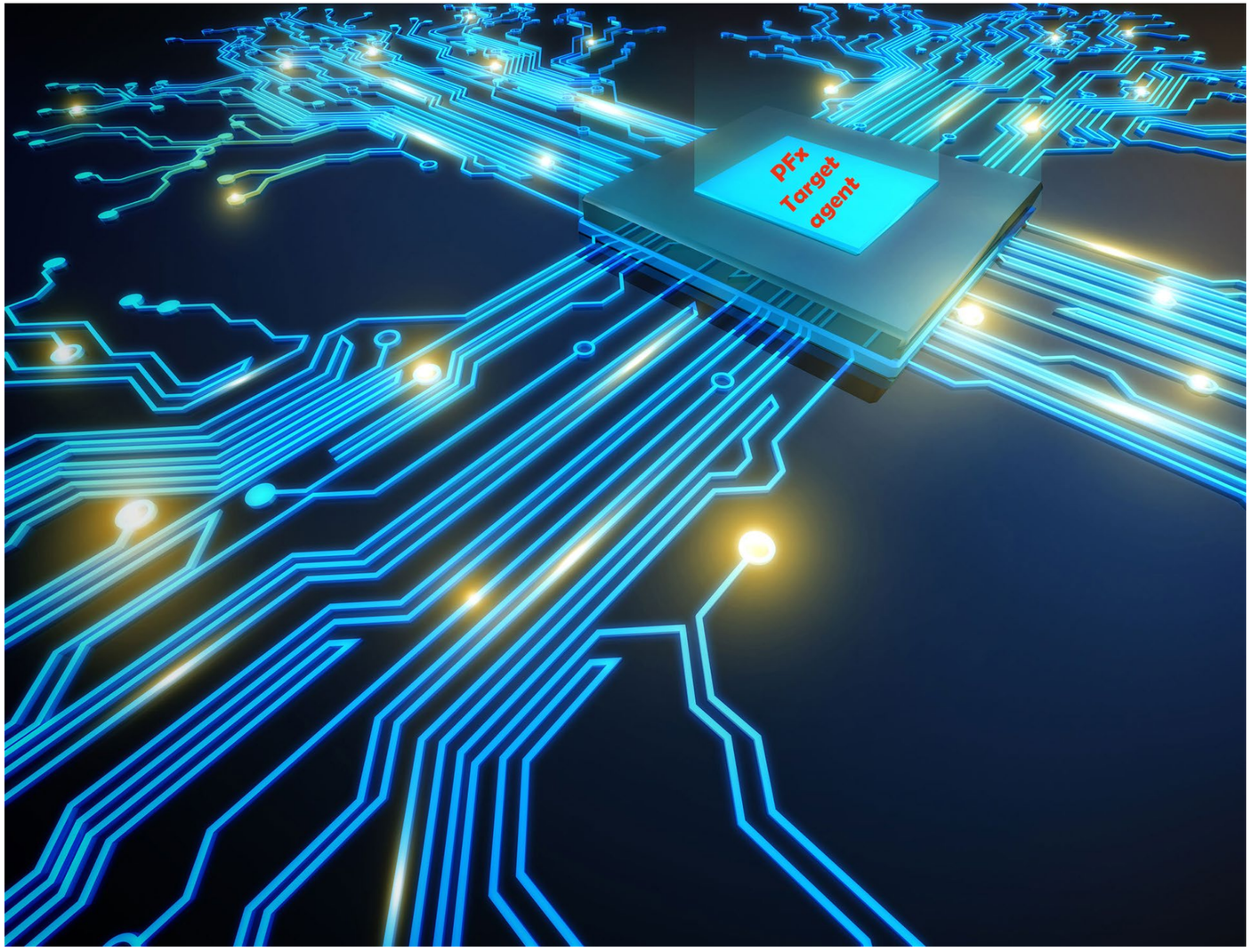
PFx Product Family

- PFx
  - PFP – Processor-based Fast Programming
    - Fast programming (MB per second) a single solution for prototype and production
  - PFT – Processor-based Functional Test
    - At-speed functional test coupled with structural
  - PFTDDR – Processor-based Functional Test for DDR
    - DDR Test and Tune - Testing at GB per second speeds
      - Zynq-7000 tuning supported
      - UltraScale microcode

PFP- Processor-based Fast Programming

- PFP is a software target agent designed for programming at device speed
- Provides in-target, in-system programming.
- Eliminating costly pre-programmed inventory
- Programming at MBytes per sec

Improved Productivity
and
Improved Manufacturing beat-rate



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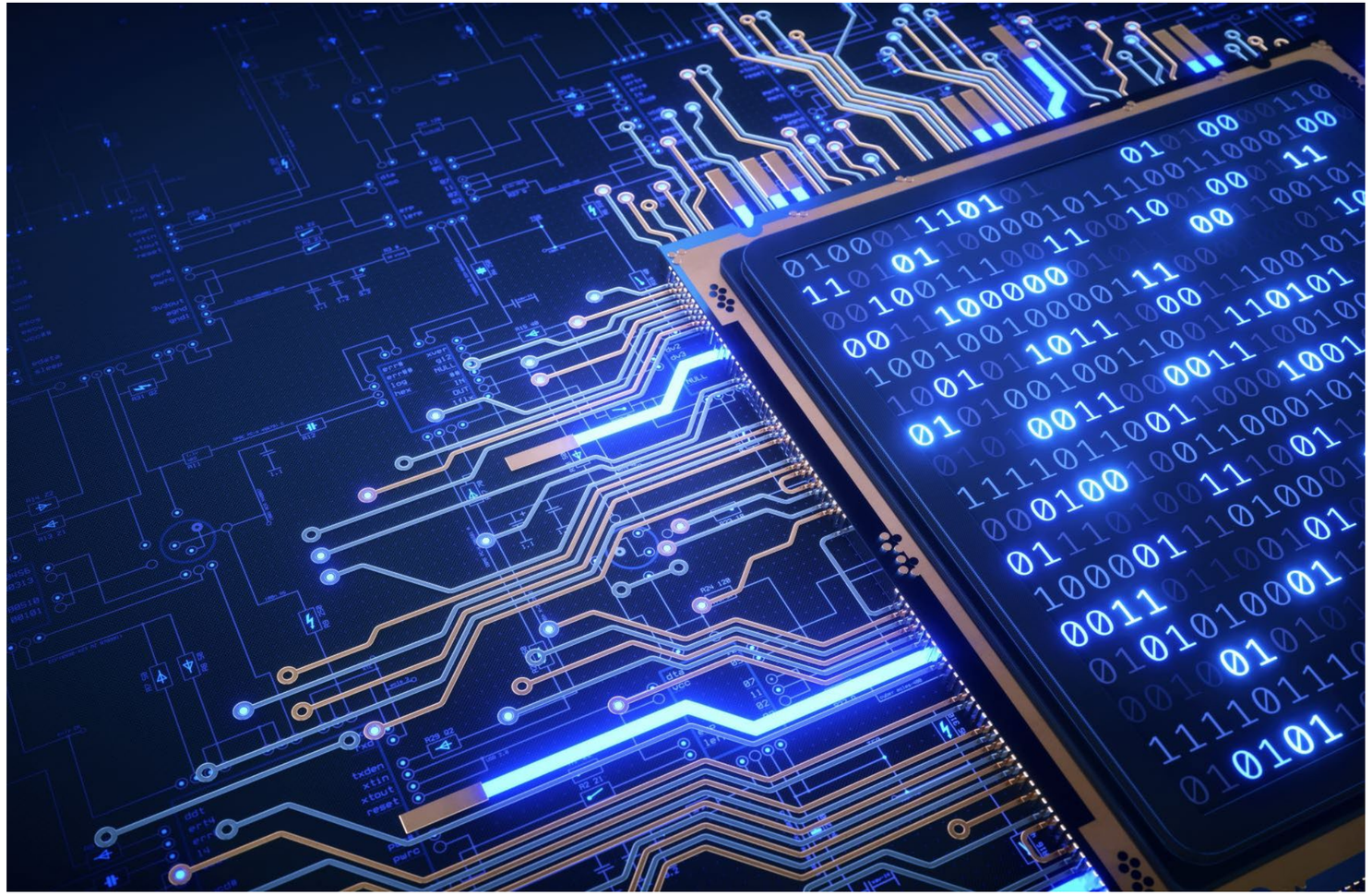
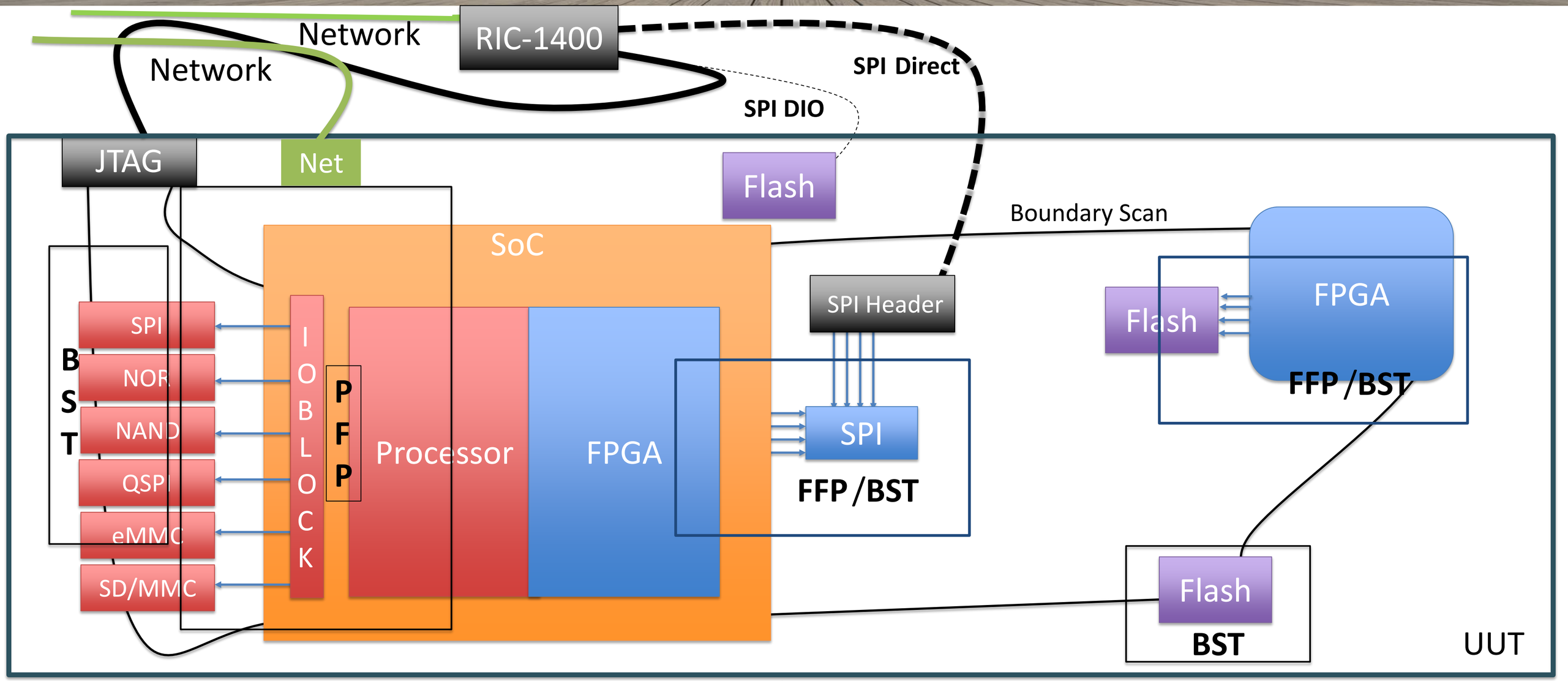
ScanWorks FPGA-based Fast Programming (FFP)

- In-system programming
- Downloadable IP to shorten the programming time



Where the Technologies Apply



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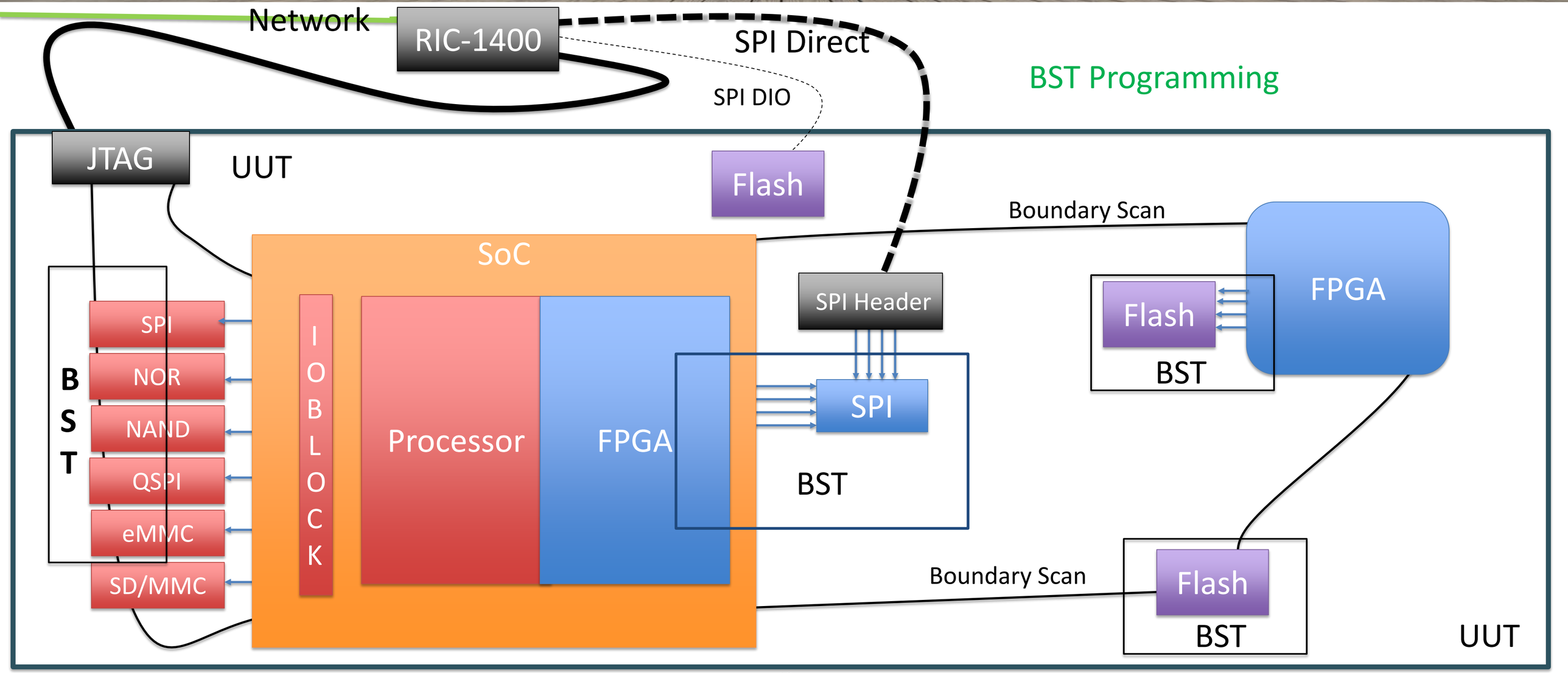
ScanWorks BST Programming Support



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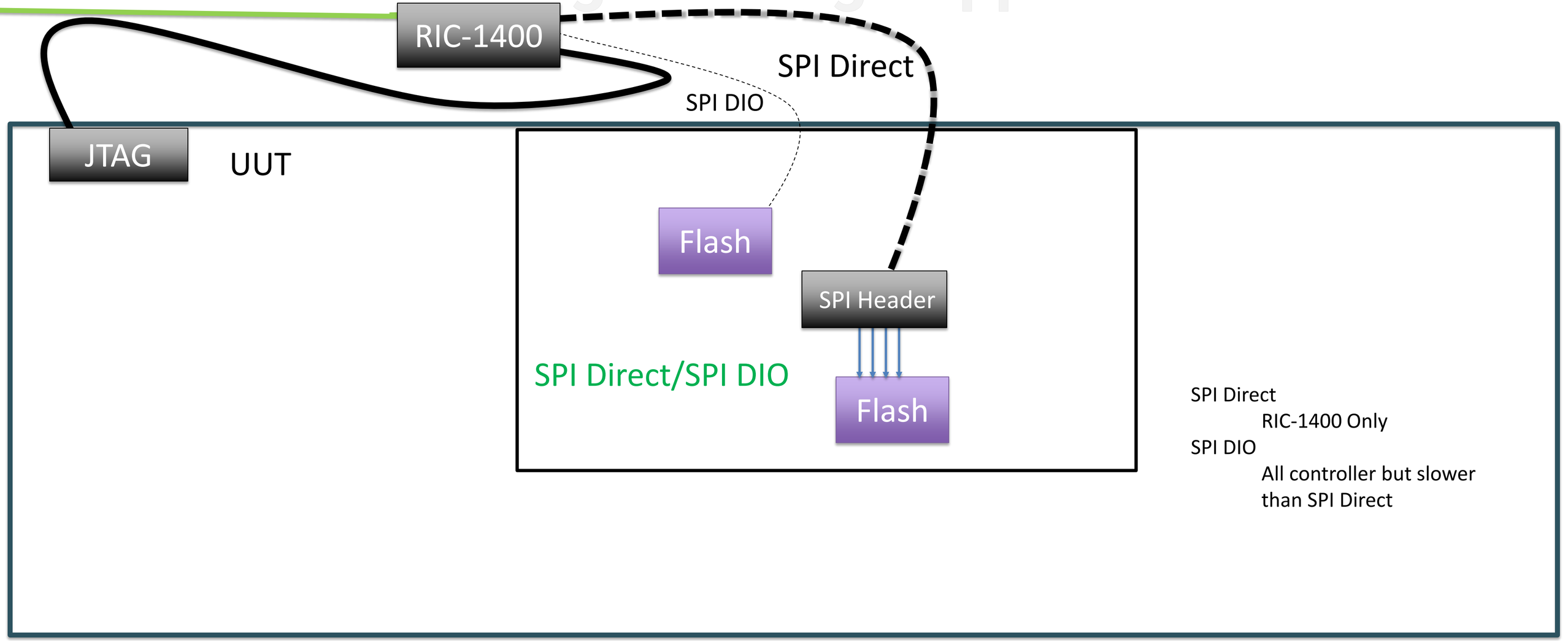
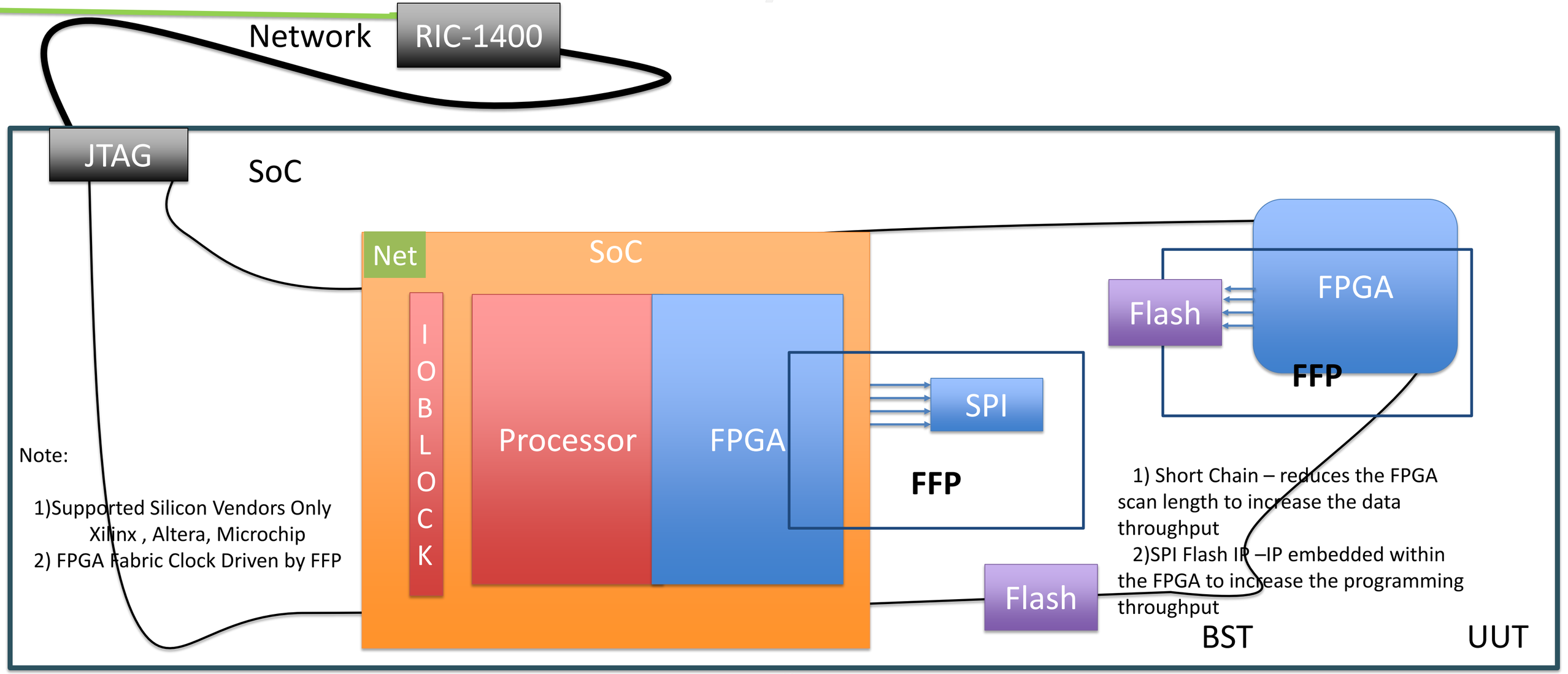
ScanWorks SPI DIO and SPI Direct Programming Support



SPI Direct
RIC-1400 Only
SPI DIO
All controller but slower than SPI Direct

ScanWorks FPGA Flash Programming (FFP) Short Chain/ SPI Flash IP

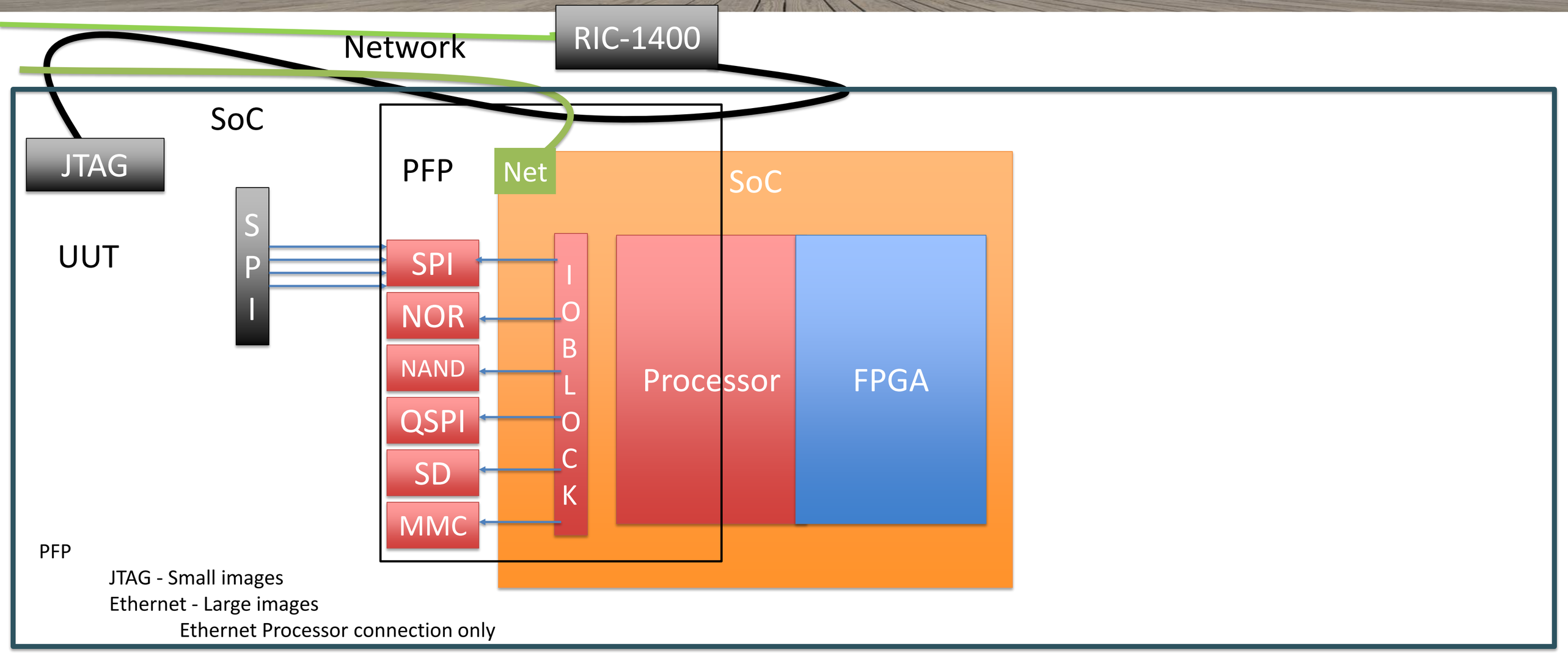


Note:

1)Supported Silicon Vendors Only
Xilinx , Altera, Microchip
2) FPGA Fabric Clock Driven by FFP

1) Short Chain – reduces the FPGA scan length to increase the data throughput
2)SPI Flash IP –IP embedded within the FPGA to increase the programming throughput

ScanWorks Processor-based Fast Programming



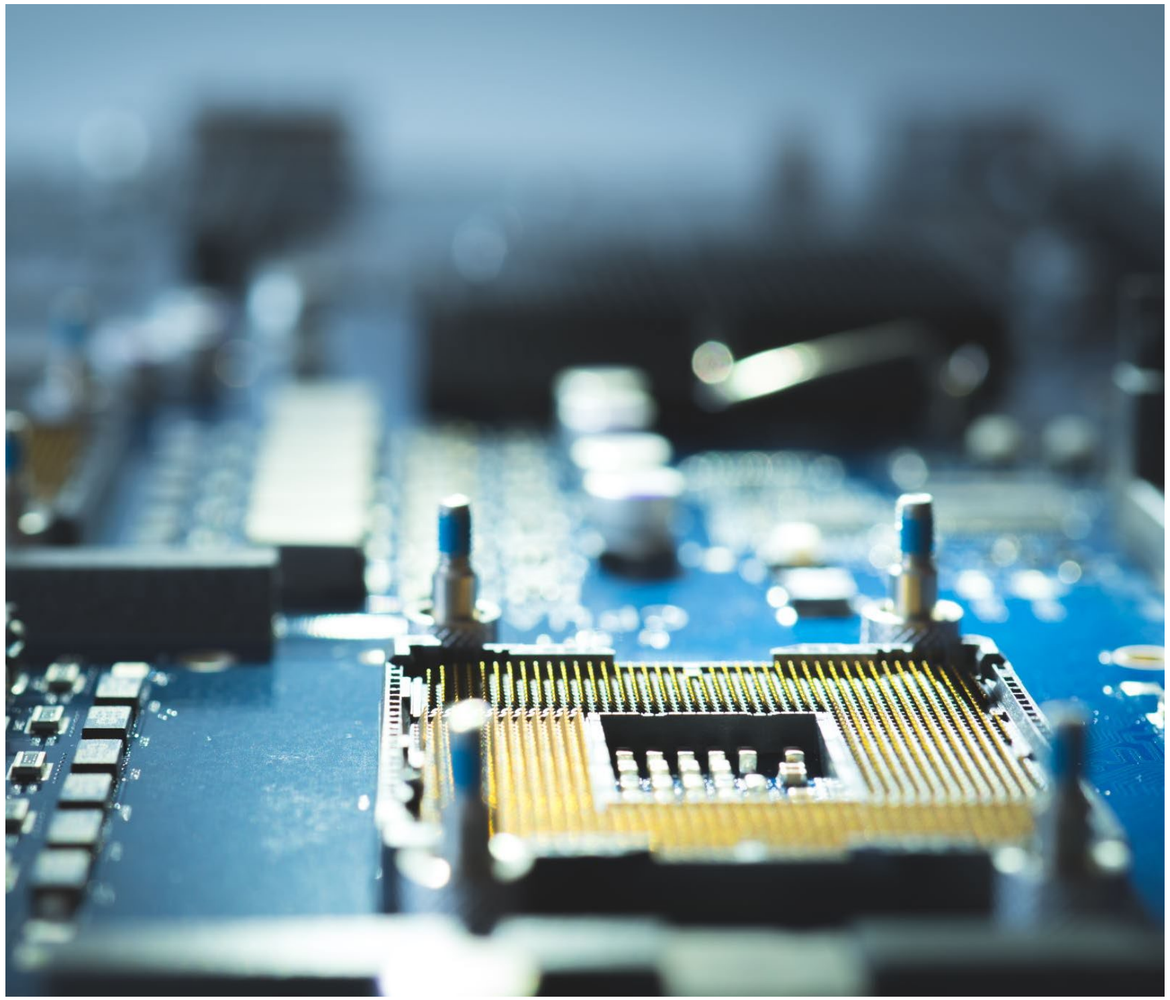
PFP

JTAG - Small images

Ethernet - Large images

Ethernet Processor connection only

Programming Methods Consideration



- BST
  - SoC boundary scan
    - NAND, NOR, SPI, QSPI, eMCC
  - Connected to JTAG enable device
- SPI DIO
  - GPIO control
- SoC – Processor System or FPGA Fabric
  - If Processor – PFP
    - NAND, NOR, SPI, QSPI, SD/MMC, eMMC
    - Ethernet data download
  - If Programmable Logic – FFP
- FPGA Standalone
  - FFP
- SPI Direct – RIC-1400
  - Flash Header access

ScanWorks Programming Speed Technology Comparison

Access Method	TCK	SoC Clock	FPGA Clock	Programming File Size	Erase/Program/ Verify Time	Improvement	Constraints
Boundary-Scan Chain	12 MHz	NA	NA	1 MB	35 minutes (2100 seconds)	-	UUT JTAG Clock Rate /BST Register
Short Chain	12 MHz	NA		1 MB	4 minutes (240 seconds)	~9x	Supported FPGA Families
SPI DIO	45 MHz	NA	NA	1 MB	2 minutes 5 seconds	17x	SPI Header
PFx Programming	30Mhz	800 MHz	NA	1MB	11 seconds	190x	UUT JTAG Clock Rate
PFx Programming Via Ethernet	30Mz	800 MHz	NA	1 MB	2.4 seconds	78x	Supported SoC Only
FPGA-based SPI Flash Programming	30 MHZ	100 MHz	100 MHz	1 MB	2.3 seconds	91x	Supported FPGA Families
SPI Direct	10 MHz	100 MHz	100 MHz	1 MB	2.3 seconds	91x	RIC-1400 and SPI Header

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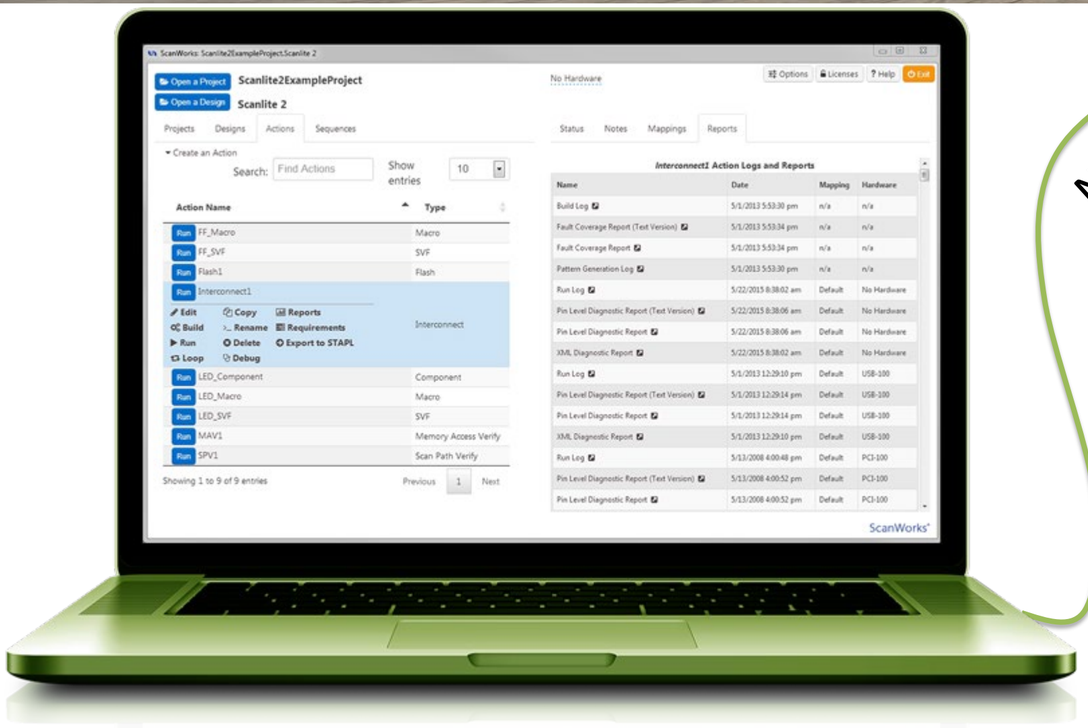
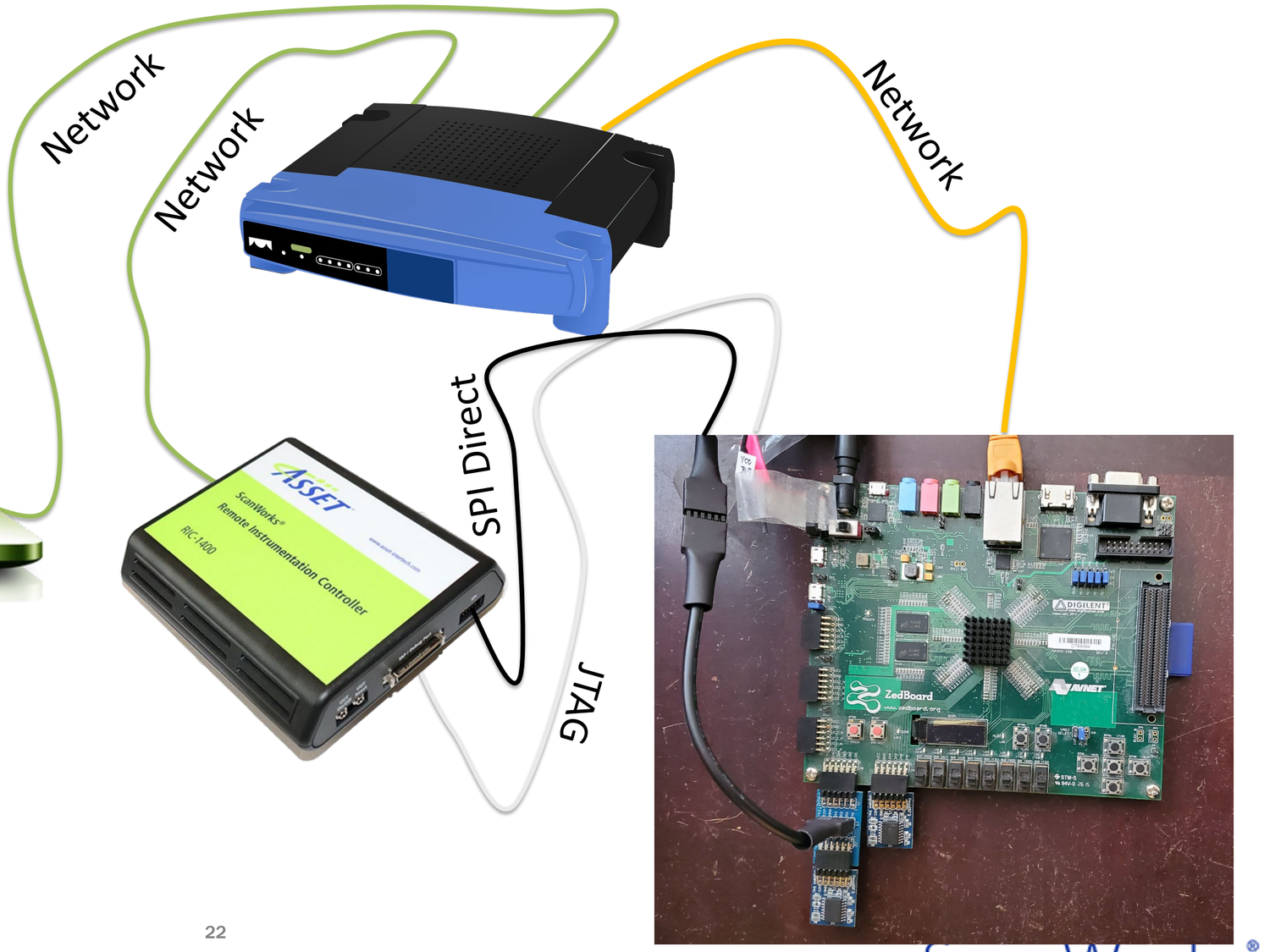
ScanWorks Demo Configuration





ScanWorks RIC-1400

SPI Direct

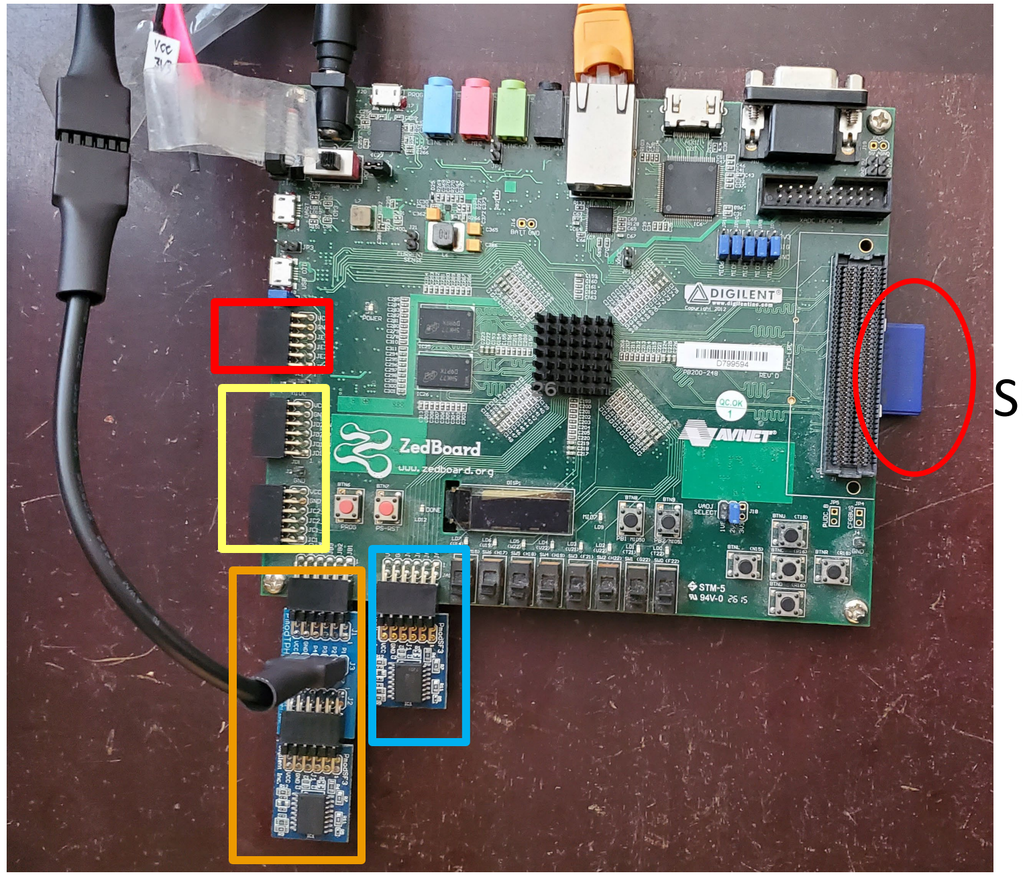
Zedboard Zynq-7000

PS- PMOD

PL- PMOD

PL-PMOD 32MB SPI

PL-PMOD DIO SPI

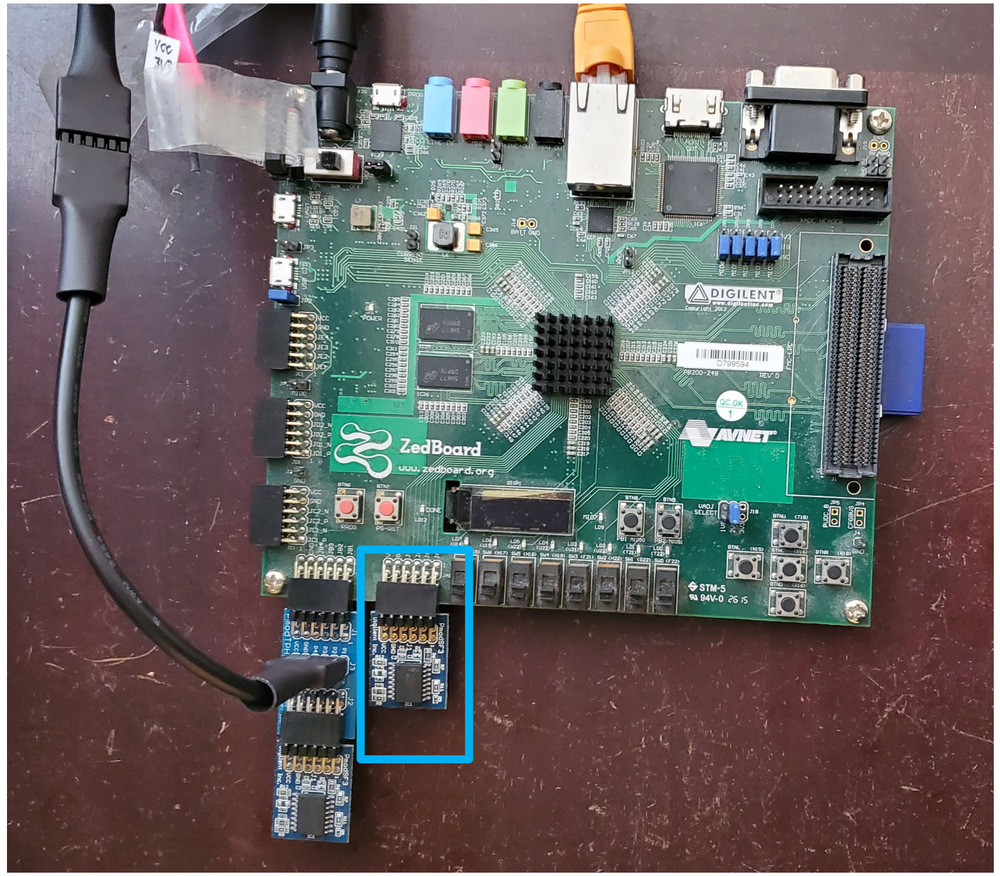


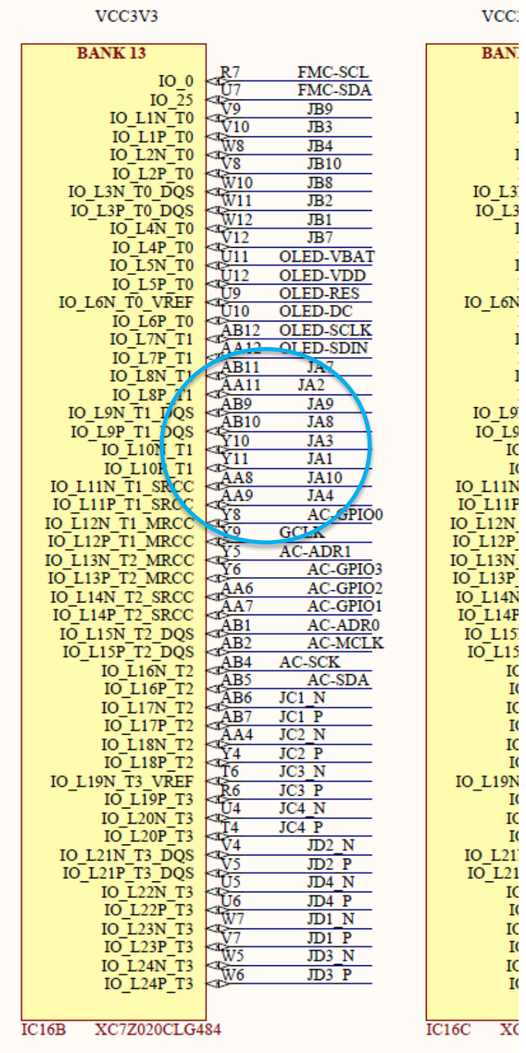
SD Card

Zedboard Zynq-7000

PL-PMOD 32MB SPI

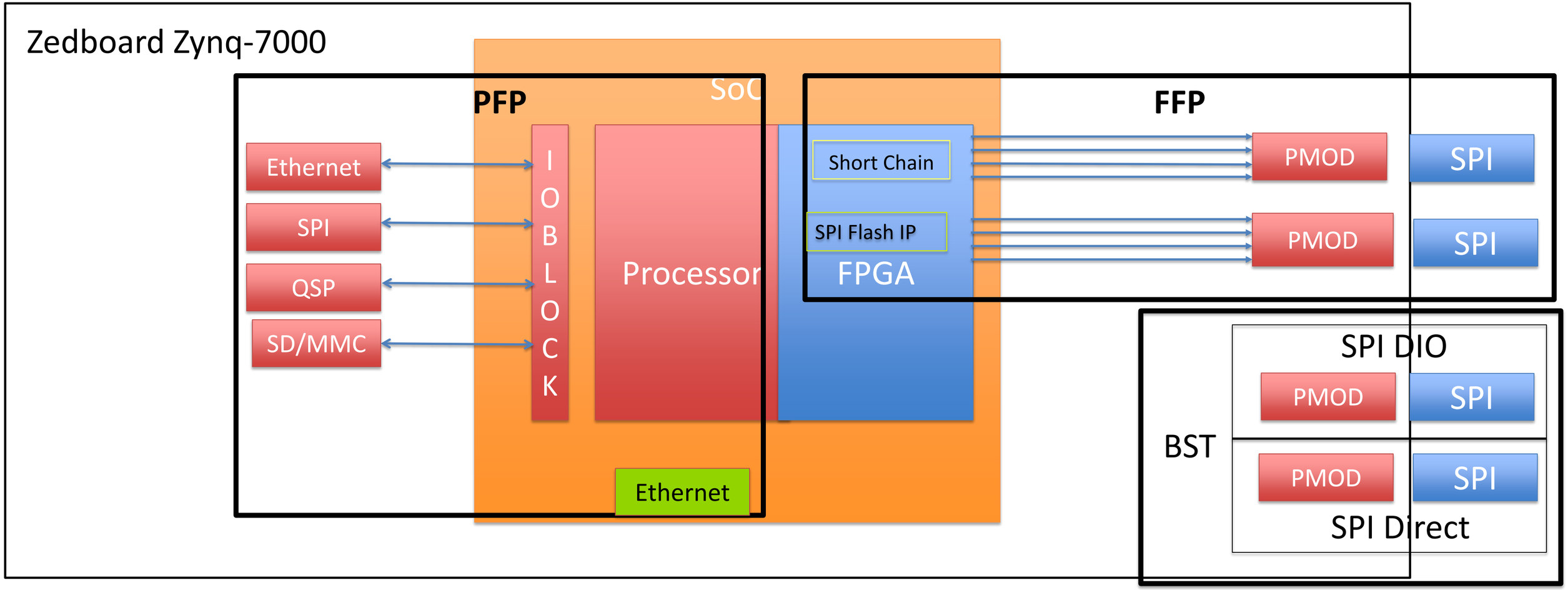
Port Direction	Port Name	FPGA Pin
INPUT	sysclk	Y9
INPUT	miso	Y10
OUTPUT	DO_pin[2]	
OUTPUT	DO_pin[1]	
OUTPUT	DO_pin[0]	
OUTPUT	mosi	AA11
OUTPUT	sclk	Y11
OUTPUT	ssel	AA9





ScanWorks Programming Demo

ScanWorks Zedboard Programming Coverage



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ScanWorks Programming Speed Technology Comparison Zedboard – XC7Z020

Access Method	TCK	SoC Clock	FPGA Clock	Programming File Size	Program Time	Improvement	Constraints
Boundary-Scan Chain	30 MHz	NA	NA	1 MB	10.5 minutes (638 seconds)	-	UUT JTAG Clock Rate /BST Register
Short Chain	30 MHz	NA	NA	1 MB	2 minutes (119 seconds)	5.3x	Supported FPGA Families
SPI DIO	30 MHz	NA	NA	1MB	1.3 minutes (80 seconds	8x	UUT JTAG Clock Rate /BST Register
PFx Programming Via JTAG	30 MHz	800 MHz	NA	1MB	8.7 seconds	74x	Supported SoC Only
FPGA-based SPI Flash Programming	30 MHz	NA	100 MHz	1 MB	3.4 seconds	185x	Supported FPGA Families
PFx Programming Via Ethernet	30 MHz	800 MHz	NA	1 MB	2.4 seconds	262x	Supported SoC Only
SPI Direct	30MHz	NA	?	1MB	1.2 seconds	525x	RIC-1400 Only UUT SPI Header

Recap

ScanWorks Addressing Technology Trends

- We demonstrated 7 different ScanWorks actions to address the challenges of increased technology complexity, expansive software growth, and all accomplished via in-system programming with greater programming performance.
- The UUT design will ultimately determine the speed at which the devices can be programmed, and which programming technology is best suited.
- These solutions will save time in development and in production.
- Lower costs can be achieved with ScanWorks onboard solutions than offboard solutions.

Resources

- BST
  - https://www.asset-intertech.com/products/scanworks/scanworks-boundary-scan-test/
- FFP
  - https://www.asset-intertech.com/products/scanworks/scanworks-fpga-based-fast-programming/
- PFP
  - https://www.asset-intertech.com/products/scanworks/scanworks-fast-flash-programming/

Questions and Contact Informaion

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