Real Insight from Code to Silicon

SourcePoint ScanWorks®

In-System Fast Flash Programming Technologies

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Project Manager for:

ScanWorks FPGA-Flash Programming ScanWorks Processor-based Fast Programmin ScanWorks Embedded Diagnostics SourcePoint Intel/AMD Debugger June 29, 2021

Agenda

Offboard vs. Onboard	 Dem
Technology Trends	- 7
ScanWorks Addressing the Trends	
 Technology Trends SoC Trends FPGA Trends ScanWorks Programming Toolbox 	Que
 Boundary-Scan Flash Processor-based Flash FPGA-based Flash Controller-based Flash 	

- ScanWorks Programming Methods
 - Programming Method Considerations
 - Speed Comparisons

SourcePoint[™] Platform for Software Debug and Trace



- 10
- edboard
- BST
- PFx
- FFP
- stions



Offboard vs. Onboard

- Offboard (preprogramming)
 - Inventory management
 - Engineering Change Orders (ECO)
 - Software updates
 - **Device shortages**

- No Inventory management issue
 - ECO minimal impact Software updates expected
 - UUT design dictates



Onboard (in-system programming)

- Preprogramming
- Device Inventory shortage

- Manufacturing beat rate
- Speed of programming possible



Technology Trends

- Market Trends
 - Design starts
 - Artificial Intelligence
 - 5G
 - Defense towards **FPGAs for Cyber** Security issues
 - Automated Driving Solutions (ADS)
 - Hyperscale Data Centers (HDC)
 - Domain-specific architectures (DSA)
 - Adaptive Computing
 - Prototyping











ScanWo

Soc Trends

- Multi-core
 - Homogenous
 - Heterogenous
- Additional cores
 - FPGA
 - GPU
 - Embedded Controllers
- Flash expansion
 - G-bit SPI support
 - SDMMC/eMMC
 - NAND





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FPGA Technology Trends





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FPGA Complexity Growth

- 9 Million System Logic Cells
- 2,072 User IO Cells
- 80 28G Transceivers
- UltraRAM
- High Bandwidth Memory (HBM)

Power consumption Adaptability curves



Programming Methods

Customer Design Dictates Fast Flash Programming methods possible.



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Programming Methods Consideration

Where is the flash device connected SoC, FPGA, Processor or JTAG only?

For the **SoC** that has both a processor core and FPGA core, is the flash device connected to processor core or to the FPGA fabric?

For the **FPGA** is there a system clock? System clock should run faster than sclk Instrument for Configuration SPI require special notation for pin assignment.

What is the **BST** chain clock rate? Slowest device clock rate in the chain determines the chain clock rate.

How large is the image?





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Programming Toolbox

ScanWorks

Boundary-Scan Test (BST) Processor-based Fast Programming (PFP) FPGA-based Fast Programming (FFP)



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ScanWorks Boundary-Scan Test (BST)

- Design to simplify the test complexity
 - Automated
 - Model-based
 - Incremental test
 - Programming support via JTAG
 - SPI, QSPI, OSPI
 - I2C, NAND, NOR
 - eMMC





Board Structural Defect Detection Opens/Short Interconnect

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PFx Product Family

PFx PFP – Processor-based Fast Programming • Fast programming (MB per second) a single solution for prototype and production PFT – Processor-based Functional Test At-speed functional test coupled with structural PFTDDR – Processor-based Functional Test for DDR DDR Test and Tune - Testing at GB per second speeds Zynq-7000 tuning supported

UltraScale microcode







PFP- Processor-based Fast Programming

- PFP is a software target agent designed for programming at device speed
- Provides in-target, in-system programming.
- Eliminating costly preprogrammed inventory
- Programming at MBytes per sec

Improved Productivity and Improved Manufacturing beatrate







ScanWorks FPGA-based Fast Programming (FFP)

 In-system programming
 Downloadable IP to shorten the programming time





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Where the Technologies Apply





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SPI Direct RIC-1400 Only SPI DIO All controller but slower than SPI Direct





Platform for Software Debug and Trace



ScanWorks Processor-based Fast Programming







Programming Methods Consideration



- BST
- SPI DIO

 - Fabric
 - - **FFP**



SoC boundary scan NAND, NÓR, SPI, QSPI, eMCC Connected to JTAG enable device

GPIO control

SoC – Processor System or FPGA

If Processor – PFP NAND, NOR, SPI, QSPI, SD/MMC, eMMC Ethernet data download If Programmable Logic – FFP **FPGA Standalone**

SPI Direct – RIC-1400 Flash Header access



ScanWorks Programming Speed Technology Comparison

Access Method	ТСК	SoC Clock	FPGA Clock	Programming File Size	Erase/Program/ Verify Time	Improvement	Constraints
Boundary-Scan Chain	12 MHz	NA	NA	1 MB	<mark>35 minutes</mark> (2100 seconds)	-	UUT JTAG Clock Rate /BST Register
Short Chain	12 MHz	NA		1 MB	<mark>4 minutes</mark> (240 seconds)	~9x	Supported FPGA Families
SPI DIO	45 MHz	NA	NA	1 MB	2 minutes 5 seconds	17x	SPI Header
PFx Programming	30Mhz	800 MHz	NA	1MB	11 seconds	190x	UUT JTAG Clock Rate
PFx Programming Via Ethernet	30Mz	800 MHz	NA	1 MB	2.4 seconds	78x	Supported SoC Only
FPGA-based SPI Flash Programming	30 MHZ	100 MHz	100 MHz	1 MB	2.3 seconds	91x	Supported FPGA Families
SPI Direct	10 MHz	100 MHz	100 MHz	1 MB	2.3 seconds	91x	RIC-1400 and SPI Header

SourcePoint

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ScanWorks Demo Configuration

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Open a Project Scanlite2ExampleProject		No Hardware	释 Options	E License	s ? Help	O Epit
Open a Design Scanlite 2						
Projects Designs Actions Sequences		Status Notes Mappings Re	ports			
Create an Action						
Search: Find Actions	Show 10	InterconnectI A	ction Logs and Report	5		- 6
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Action Name	🕈 Туре 🔅	Build Log 🖬	5/1/2013 5:53:30 pm	n/a	n/a	
Ran FF_Macro	Macro	Fault Coverage Report (Text Version)	5/1/2013 5:53:34 pm	n/a	n/a	
Run FF_SVF	SVF	Fault Coverage Report 😰	5/1/2013 5:53:34 pm	n/a	n/a	
Run Flash1	Flash	Pattern Generation Log 😫	5/1/2013 5:53:30 pm	n/a	n/a	
Run Interconnect1		Run Log 😡	5/22/2015 8:38:02 am	Default	No Hardware	
/ Edit Copy @ Reports		Pin Level Disgnostic Report (Text Version)	5/22/2015 8:38:06 am	Default	No Hardware	
OC Build >_ Rename III Requirements	Interconnect	Pin Level Diagnostic Report	5/22/2015 8:38:06 am	Default	No Hardware	
13 Loop & Debug		XMI, Diagnostic Report 😰	5/22/2015 8:38:02 am	Default	No Hardware	
Run LED_Component	Component	Run Log 😫	5/1/2013 12:29:10 pm	Default	U58-100	
Run LED_Macro	Macro	Pin Level Diagnostic Report (Text Version)	5/1/2013 12:29:14 pm	Default	USB-100	
Run LED_SVF	SVF	Pin Level Diagnostic Report	5/1/2013 12:29:14 pm	Default	USB-300	
Ran MAV1	Memory Access Verity	XML Diagnostic Report 😰	5/1/2013 12:29:10 pm	Default	U58-100	
Run SPV1	Scan Path Verify	Run Log 🖬	5/13/2008 4:00:48 pm	Default	PCI-100	
showing 1 to 9 of 9 entries	Previous 1 Next	Pin Level Diagnostic Report (Text Version)	5/13/2008 4:00:52 pm	Default	PCI-100	
		Pin Level Disgnostic Report	5/13/2008 4:00:52 pm	Default	PCI-100	

Network Network SPI Direct ASSET



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Platform for Embedded Inst

ScanWorks RIC-1400





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Zedboard Zynq-7000

PS- PMOD

PL- PMOD

PL-PMOD 32MB SPI

PL-PMOD DIO SPI









Zedboard Zynq-7000

PL-PMOD 32MB SPI

Port Direction	Port Name	FPGA Pin
INPUT	sysclk	Y9
INPUT	miso	Y10
OUTPUT	DO_pin[2]	
OUTPUT	DO_pin[1]	
OUTPUT	DO_pin[0]	
OUTPUT	mosi	AA11
OUTPUT	sclk	Y11
OUTPUT	ssel	AA9





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VCC3V3			VCC
BANK 13]		BAN
10.0	R7	FMC-SCL	
10_0	07	FMC-SDA	
IO_23	V9	JB9	
IO_LIN_IO	V10	JB3	
10_LIP_10	W8	JB4	
10_L2N_10	V8	JB10	
10_L2P_10	W10	JB8	10.1
10_L3N_10_DQS	W11	JB 2	10_L3
IO_L3P_T0_DQS	[≪] W12	JB1	IO_L
IO_L4N_10	V12	JB7	
IO_L4P_T0	U11	OLED-VBAT	
IO_L5N_T0	<10112	OLED-VDD	
IO_L5P_T0	10	OLED-RES	
IO_L6N_T0_VREF		OLED-DC	IO_L6N
IO_L6P_T0	AB12	OLED SCLK	
IO_L7N_T1		OLED-SCER	
IO_L7P_T1	APII	Dog	
IO_L8N_T1		IA2	
IO L8P 71	AAII ADO	JAZ	
IO L9N T1 DQS		JA9	IO L9
IO L9P TI DOS	ABIU	JAS	IOL
		JA3	_I
IO L101 T1		JAI	I
IO L11N T1 SRCC	AA8	JA10	IO L11N
IO L11P T1 SRCC	AA9	JA4	IO L111
IO L12N T1 MRCC	<u>128</u>	AC GPIO0	IO L12N
IO L12P T1 MRCC	0	GCLA	IO L12P
IO L13N T2 MRCC		AC-ADR1	IO L13N
IO L13P T2 MRCC	A YO	AC-GPIO3	IO L13P
IO L14N T2 SRCC	AA6	AC-GPIO2	IO 1.14N
IO L14P T2 SRCC	AA/	AC-GPIO1	IO L14
IO LISN T2 DOS	AB1	AC-ADR0	IO 1.15
IO LISP T2 DOS	AB2	AC-MCLK	IO L1
IO LIGN T2	AB4	AC-SCK	10_21
IO_L16P_T2	AB5	AC-SDA	I
IO 117N T2	AB6	JC1_N	T
IO_L17R_12	AB7	JC1_P	I
IO L 19N T2	AA4	JC2_N	T
IO_LISIV_12	¥4	JC2_P	T
IO I ION TO VIEF	T 6	JC3_N	IO I 103
IO_LI9N_IS_VKEF	R6	JC3 P	10_1191
10_L19F_13	<u>U</u> 4	JC4 N	1
IO_L20N_I3		JC4 P	10
10_L20P_13	V4	JD2 N	10 101
10_L21N_13_DQS	V5	JD2 P	10_L21
10_L21P_13_DQS	U5	JD4 N	10_12
10_L22N_T3	U6	JD4 P	I
10_L22P_T3	W7	JD1 N	I
IO_L23N_T3	V7	JD1 P	I
IO_L23P_T3	W5	ID3 N	I
IO_L24N_T3	W6	TD3 P	I
IO_L24P_T3		325 1	I
16B XC7Z020CLG4	84		IC16C X

ScanWorks® Platform for Embedded Instruments



ScanWorks Programming Demo





ScanWorks Zedboard Programming Coverage





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ScanWorks Programming Speed Technology Comparison Zedboard – XC7Z020

 Access Method	ТСК	SoC Clock	FPGA Clock	Programming File Size	Program Time	Improvement	Constraints
Boundary-Scan Chain	30 MHz	NA	NA	1 MB	<mark>10.5</mark> minutes (638 seconds)	-	UUT JTAG Clock Rate /BST Register
Short Chain	30 MHz	NA	NA	1 MB	<mark>2 minutes</mark> (119 seconds)	5.3x	Supported FPGA Families
SPI DIO	30 MHz	NA	NA	1MB	<mark>1.3 minutes</mark> (80 seconds	8x	UUT JTAG Clock Rate /BST Register
PFx Programming Via JTAG	30 MHz	800 MHz	NA	1MB	8.7 seconds	74x	Supported SoC Only
FPGA-based SPI Flash Programming	30 MHz	NA	100 MHz	1 MB	3.4 seconds	185x	Supported FPGA Families
PFx Programming Via Ethernet	30 MHz	800 MHz	NA	1 MB	2.4 seconds	262x	Supported SoC Only
SPI Direct	30MHz	NA	?	1MB	1.2 seconds	525x	RIC-1400 Only UUT SPI Header

Platform for Software Debug and Trace

ScanWorks Platform for Embedded Instruments

Recap

ScanWorks Addressing Technology Trends

- We demonstrated 7 different ScanWorks actions to address the challenges of increased technology complexity, expansive software growth, and all accomplished via in-system programming with greater programming performance.
- The UUT design will ultimately determine the speed at which the devices can be programmed, and which programming technology is best suited.
- These solutions will save time in development and in production.
- Lower costs can be achieved with ScanWorks onboard solutions than offboard solutions.





Resources

BST

- https://www.asset-intertech.com/products/scanworks/scanworksboundary-scan-test/
- FFP
 - https://www.asset-intertech.com/products/scanworks/scanworks-fpga-<u>based-fast-programming/</u>
- PFP
 - https://www.asset-intertech.com/products/scanworks/scanworks-fast-<u>flash-programming/</u>







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