Real Insight from Code to Silicon

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Embedded JTAG/Boundary Scan for Built-In Self-Test

Michael R. Johnson
ScanWorks BST Product Manager/Support Manager
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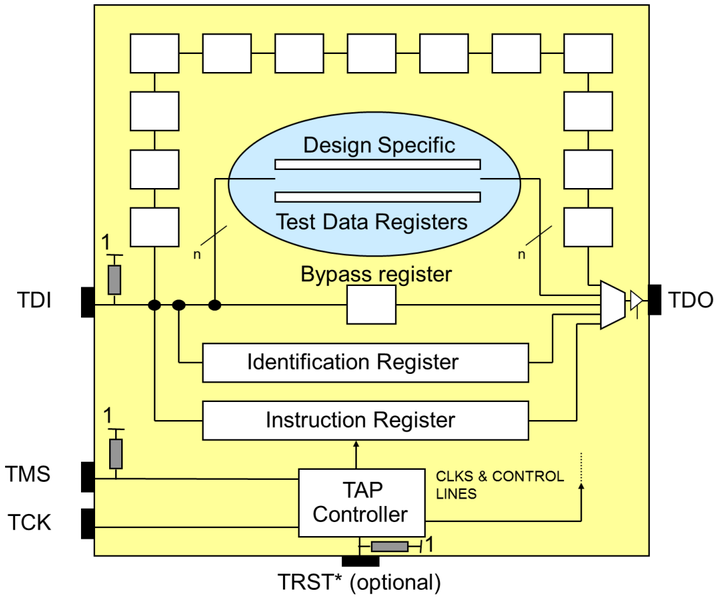
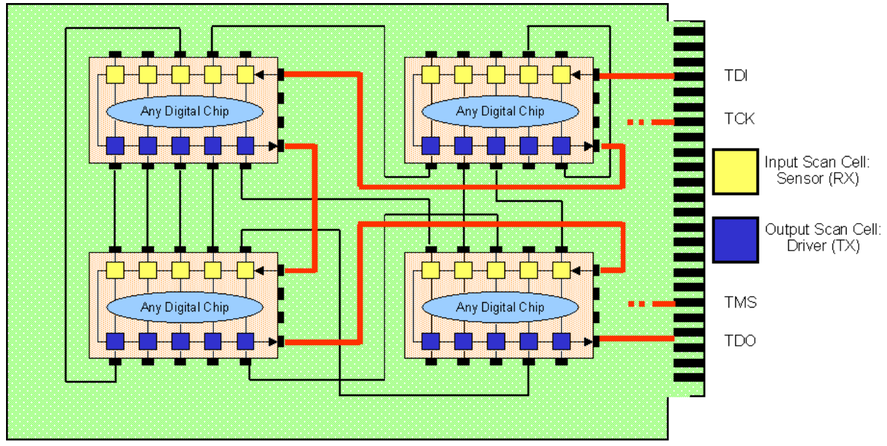
Agenda

- JTAG/Boundary Scan Overview
- ScanWorks Embedded Diagnostics (SED) for Test
- SED for Test Overview
- SED for Test Actions
- SED for Test Value
- SED for Test Demonstration
- SED for Test Block Diagram and Footprint
- Summary

JTAG/Boundary Scan Overview

- JTAG/boundary scan is a static, vector-based test technology implemented through on-chip embedded instruments within commercial silicon
- Performs shorts/opens/stuck-at fault testing on PCBs with diagnostics to the device and net/pin level
- Useable throughout the entire lifecycle of a product
- A proven, mature test and programming technology





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ScanWorks Embedded Diagnostics (SED) for Test

- JTAG/boundary scan is typically used “locally” for PCB test development, production and system debug
- An external PC uses a dedicated hardware controller to test and program PCBs in development, production or perform debug on the benchtop
- Since JTAG/boundary scan is software that leverages on-chip embedded logic, it is possible to port that application directly onto the PCB itself
- SED for Test eliminates the need for hardware, cables, and fixturing for JTAG/boundary-scan testing
- SED for Test creates a “remote” JTAG/boundary-scan test and programming application

JTAG/Boundary-Scan Test Software

ASSET PCIe-410 HW controller

PCB

Embedded JTAG/Boundary-Scan Test software resides within an FPGA/SoC or Service Processor

ScanWorks Embedded Diagnostics (SED) for Test

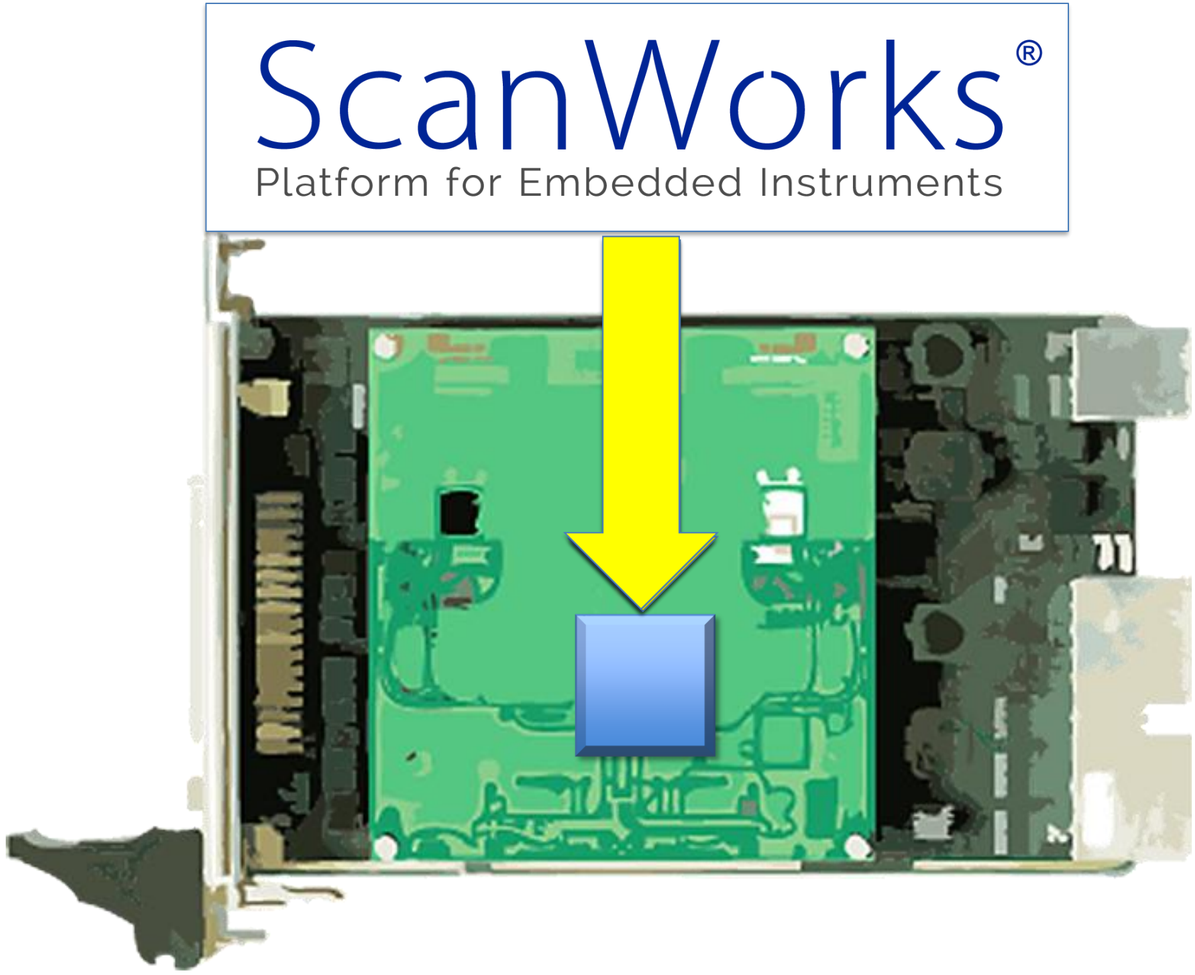
- ScanWorks Embedded Diagnostics (SED) for Test is a tool strategy that supports JTAG/boundary-scan testing and device programming capabilities embedded directly on an FPGA/SoC or service processor on a PCB
- SED for Test is applicable to a variety of industries and technologies where in situ, real time diagnostic data collection is valuable

SED for Test Actions

- Scan Path Verify (SPV)
  - Boundary Scan device validation
- Interconnect
  - Structural testing for shorts/opens/stuck-at faults to the device and net/pin level
- Memory Access Verify (MAV)
  - Structural and functional memory device testing

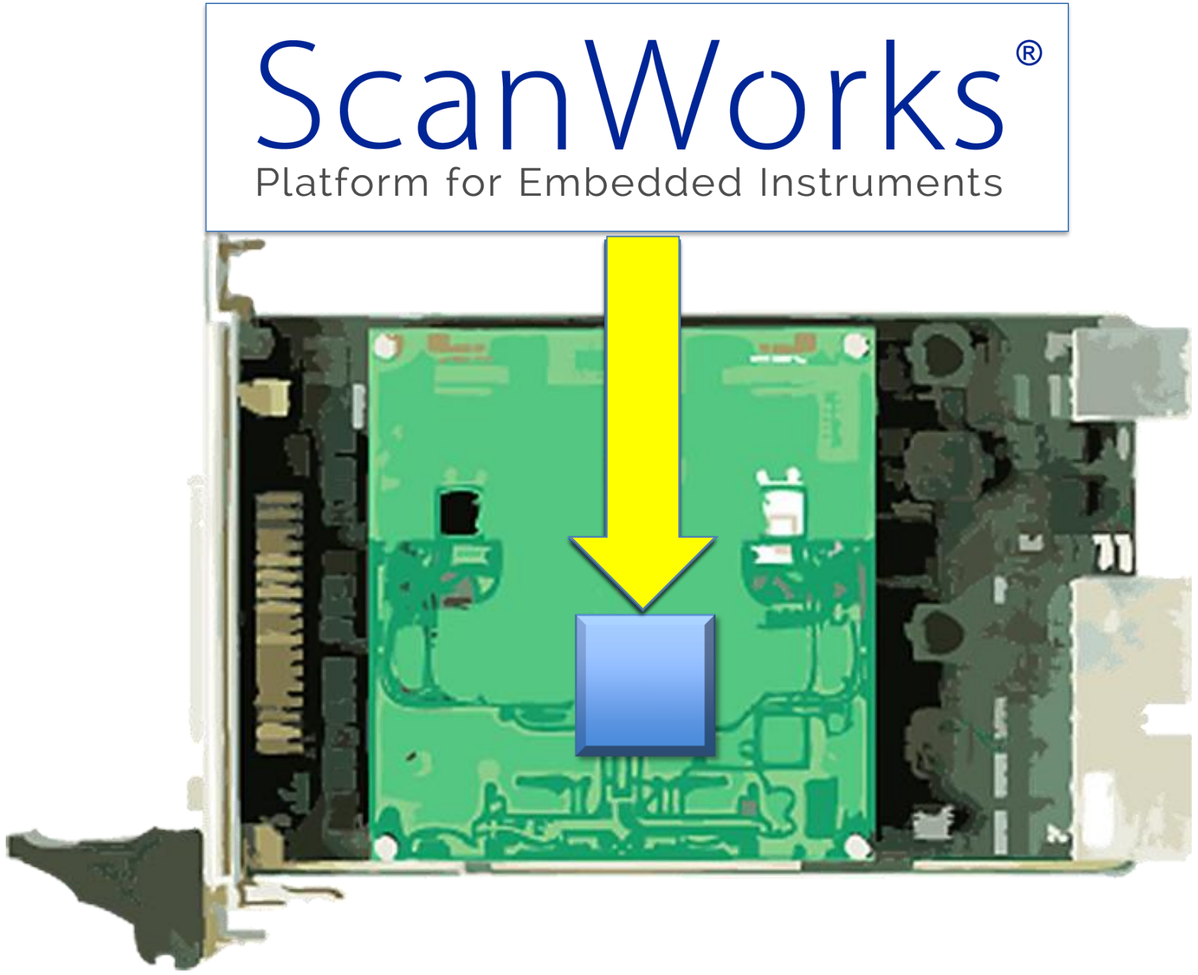
SED for Test Value

- SED for Test can be executed remotely and in situ with diagnostic data gathered in real time
- Can be executed as part of Built-In Self-Test (BIST), Power-On Self-Test (POST), system audits, and operational measurements
- Requires only that the elements of the PCB that implement SED for Test power up and be operational
- SED for Test is completely out of band
- Can be used in implementing System JTAG (SJTAG – use of boundary scan within complex multi-board systems)



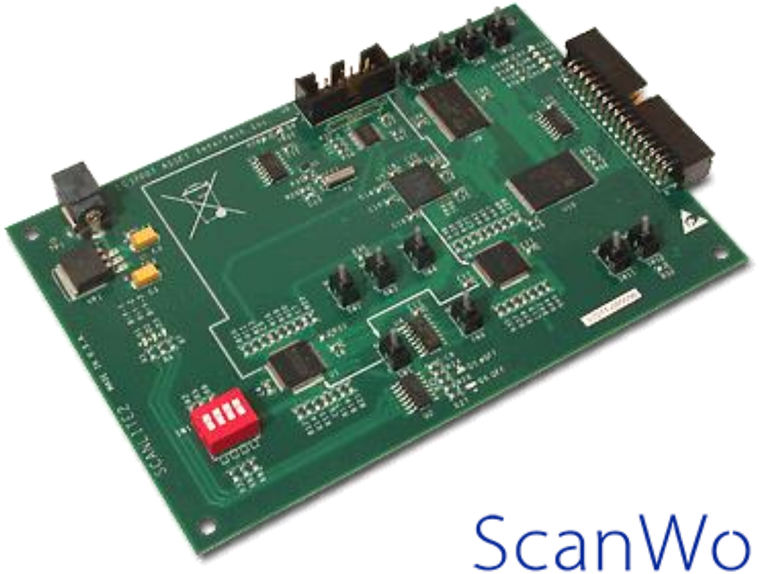
SED for Test Value

- SED for Test provides a level of diagnostic granularity not usually found via in-system functional tests
- The same ScanWorks PCB tests used in production can be reused in situ and during repair
- Data can be uploaded into a ScanWorks benchtop system for diagnostic processing and reporting
- Addresses intermittent faults and “No Fault Found” (NFF) issues



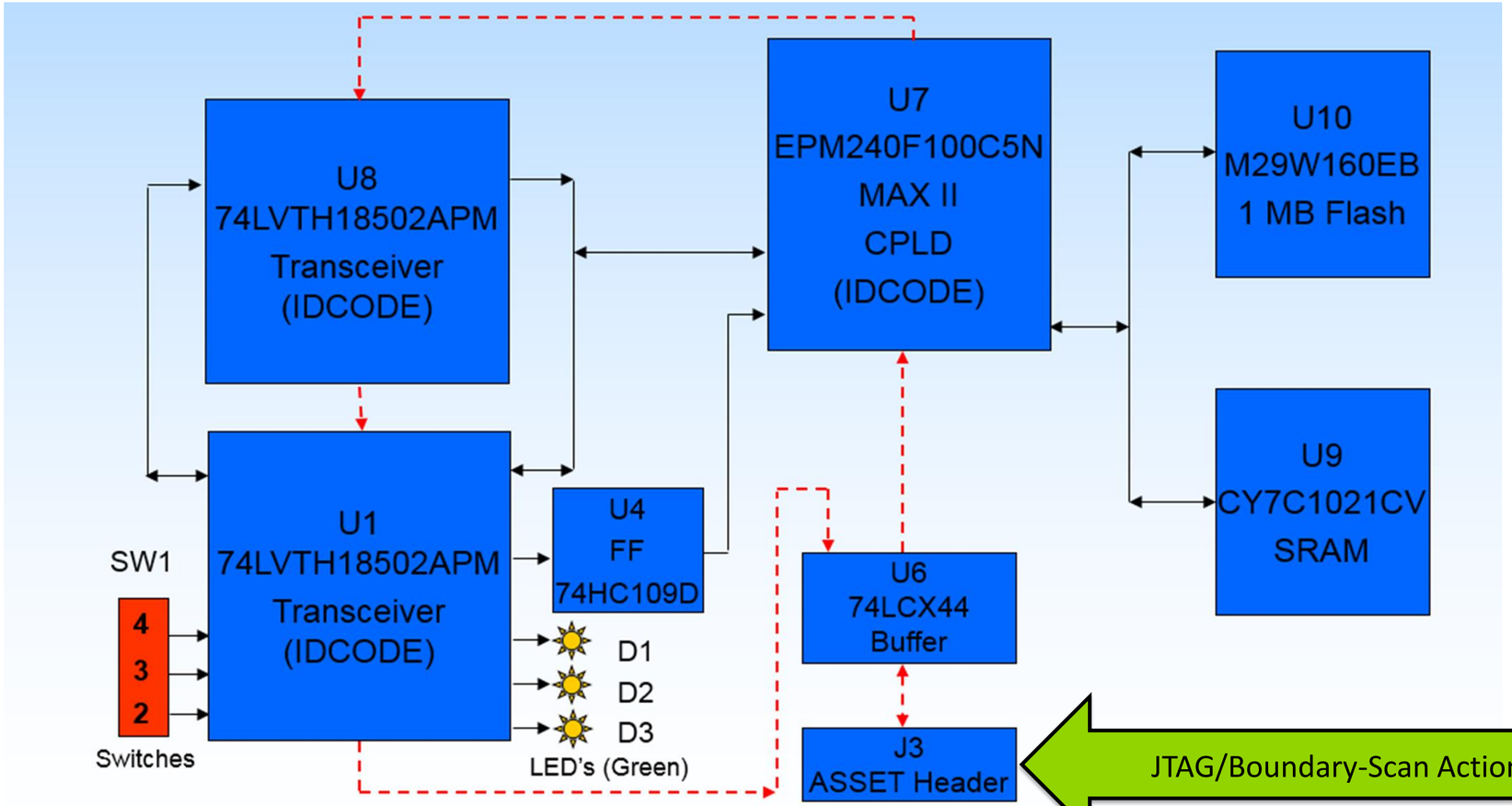
SED for Test Demonstration

- SED Host - Altera Cyclone V SoC
  - Dual Arm® Cortex®-A9 MPCore™ System On Chip (SoC) Cyclone® V SE FPGA
  - VxWorks Real-time operating system (RTOS)
  - Host for the embedded ScanWorks SEDPlayer which runs embedded JTAG/boundary-scan actions
  - Action results are stored in memory for retrieval
- Target - ScanLite2
  - 3 JTAG/boundary-scan devices
  - Target for JTAG/boundary-scan actions run by the SEDPlayer
  - Switches for fault simulation



SED for Test Demonstration

Target
ScanLite2



Embed SEDPlayer and ScanWorks actions

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Ethernet

Upload action results

SED Host
Cyclone® V SoC
Arm® Cortex® A9

Embedded ScanWorks Action Player and Actions

ScanWorks® Platform for Embedded Instruments

Serial

Run ScanWorks actions

Once the SEDPlayer and actions have been embedded, invoking the SEDPlayer, running actions, and storing results can be automated by a script or program.

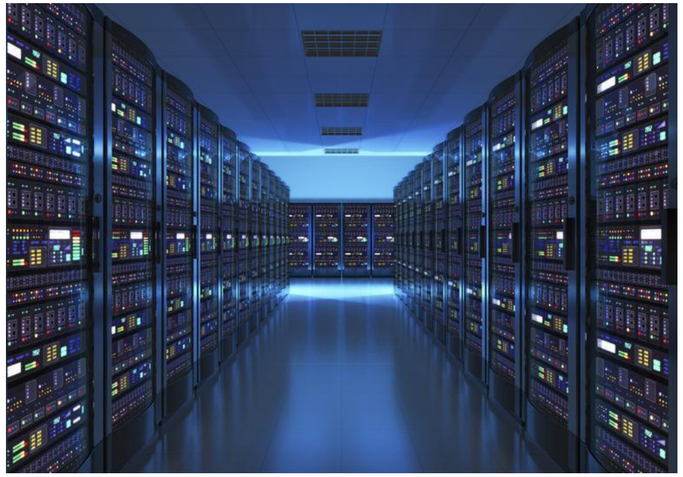
JTAG/Boundary-Scan Actions & Results

Ethernet and serial interfaces are not needed for a typical SED application (required to facilitate the demonstration).

SED for Test Demonstration

Fault Switch	Default Setting	Fault Setting	Fault Type
SW2	Norm	SA0	2 Drivers, 1 Receiver
SW3	Norm	SA0	1 Driver, 2 Receivers - Open
SW4	Norm	SA0	2 Drivers, 2 Receivers – 1 Pin Fail
SW5	Norm	SA0	TDO/TDI Error
SW6	Norm	SA1	Flip Flop Error
SW7	Norm	SA0	Memory – D0
SW8	Norm	Bridge	Flash Interconnect Fail
SW9	Norm	SA0	Memory – D1
SW10	Norm	Bridge	Address Fault
SW11	Norm	SA0	Short
SW12	Norm	Open	1 Driver, 1 Receiver
Data Switch	**Default Setting**		**Data Type**
SW1 (1-4)	Off	On	3- Bits of Test Stimulus Data for U1 and LED's

SED for Test Demonstration



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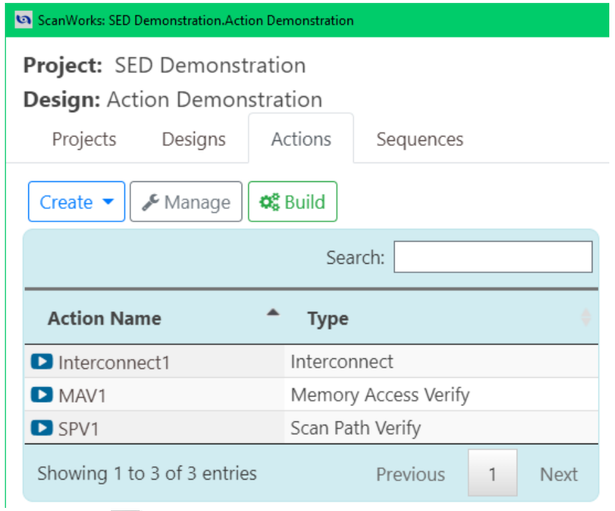
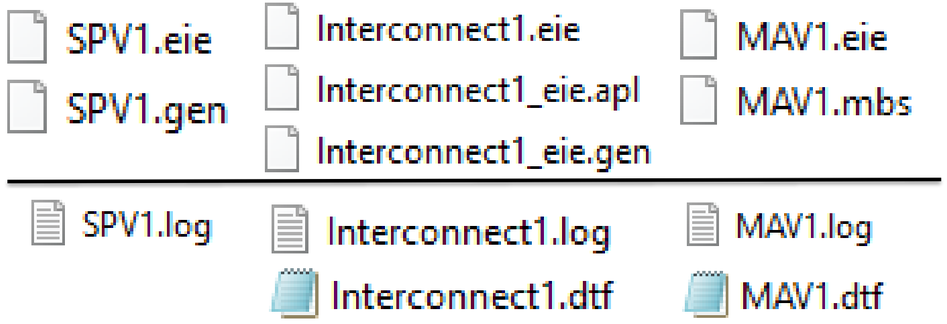
SED for Test Demonstration

- A ScanWorks project and design was created to test the target
- Files transferred to the SoC (aside from the SEDPlayer.vxe) were generated during the normal ScanWorks test development process
  - .eie, .gen, _eie.gen, _eie.apl, .mbs
- Files transferred from the SoC to ScanWorks were generated during the normal action run process
  - .log, .dtf
- The number at the end of the SEDPlayer command tells it which action to run
  - SPV = 1, Interconnect = 2, MAV = 3
- VxWorks was the operating system on the SoC but this could be any other operating system or RTOS; or SED for Test could even be implemented on a processor running without an operating system





VxWorks

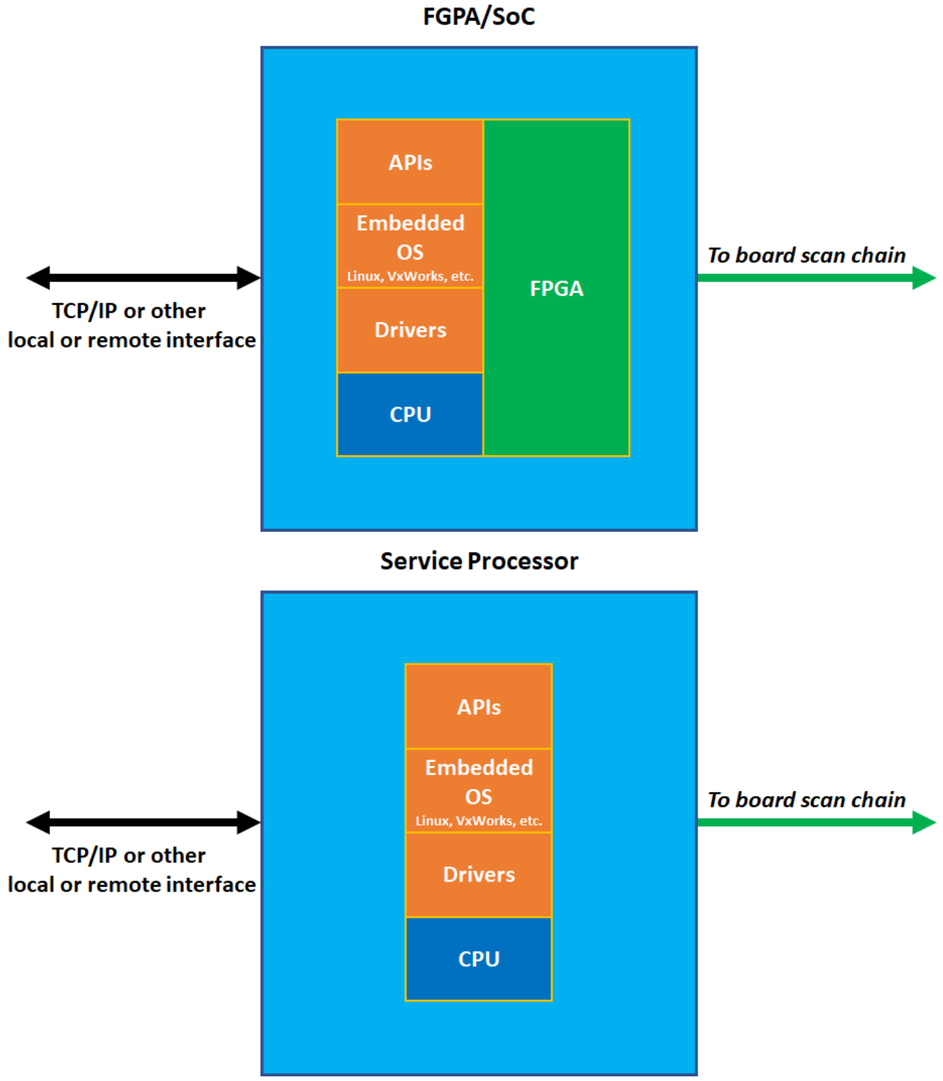
Linux

freeRTOS

Zephyr™

SED for Test Block Diagram and Footprint

- The resources required for the TAP Controller IP are small when compared to today's FPGAs
  - Uses < 4,000 Lookup Tables (LUTs)
  - Uses less than < 75kb memory
- Action players run on the CPU
  - Occupies < 2MB flash footprint
- Action data
  - Occupies ~ 300kB (typical) to >~1MB (for large designs)



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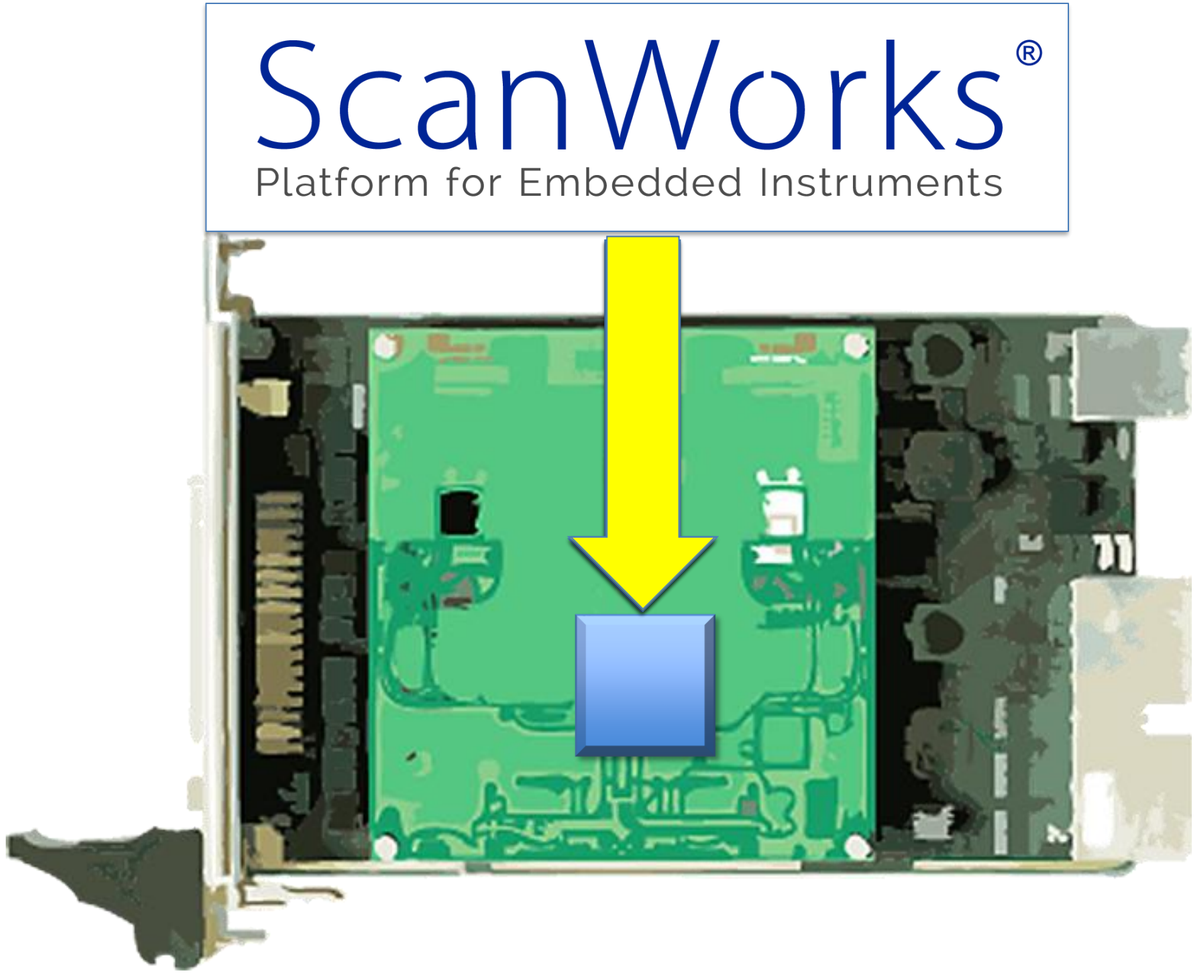
Summary

- SED for Test embeds JTAG/boundary-scan test capabilities directly on a PCB
- Creates a powerful BIST without external hardware that can be used throughout the entire lifecycle of the PCB
- Can be executed as part of a POST or system audit, in situ, with data collected in real time
- Action diagnostic results can be uploaded and processed by a benchtop ScanWorks system
- Addresses intermittent faults and “No Fault Found” (NFF) issues



For More Information

- Go to our blog, Embedded JTAG for Built-In Self Test, https://www.asset-intertech.com/resources/blog/2018/04/embedded-jtag-for-built-in-self-test/
- Download our eBook, Embedded JTAG for Boundary-Scan Test, https://www.asset-intertech.com/resources/eresources/embedded-jtag-boundary-scan-test/
- View our webinar, Embedded @Scale JTAG-based Debug of x86 Servers, https://www.asset-intertech.com/resources/blog/2021/03/webinar-embedded-scale-jtag-based-debug-of-x86-servers/

Questions and Contact Information

Contact Information:

Michael R. Johnson

7161 Bishop Rd. Ste. 250

Plano, TX. 75024

mjohnson@asset-intertech.com

www.asset-intertech.com

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