Embedded JTAG/Boundary Scan for Built-In Self-Test

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Agenda

- JTAG/Boundary Scan Overview
- ScanWorks Embedded Diagnostics (SED) for Test
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- SED for Test Actions
- SED for Test Value
- SED for Test Demonstration
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- Summary
JTAG/Boundary Scan Overview

- JTAG/boundary scan is a static, vector-based test technology implemented through on-chip embedded instruments within commercial silicon
- Performs shorts/opens/stuck-at fault testing on PCBs with diagnostics to the device and net/pin level
- Useable throughout the entire lifecycle of a product
- A proven, mature test and programming technology
JTAG/boundary scan is typically used “locally” for PCB test development, production and system debug.

An external PC uses a dedicated hardware controller to test and program PCBs in development, production or perform debug on the benchtop.

Since JTAG/boundary scan is software that leverages on-chip embedded logic, it is possible to port that application directly onto the PCB itself.

SED for Test eliminates the need for hardware, cables, and fixturing for JTAG/boundary-scan testing.

SED for Test creates a “remote” JTAG/boundary-scan test and programming application.
ScanWorks Embedded Diagnostics (SED) for Test

- ScanWorks Embedded Diagnostics (SED) for Test is a tool strategy that supports JTAG/boundary-scan testing and device programming capabilities embedded directly on an FPGA/SoC or service processor on a PCB.
- SED for Test is applicable to a variety of industries and technologies where in situ, real time diagnostic data collection is valuable.
Likes and Reposts

Scan Path Verify (SPV)
- Boundary Scan device validation
- Interconnect
- Structural testing for shorts/opens/stuck-at faults to the device and net/pin level

Memory Access Verify (MAV)
- Structural and functional memory device testing
SED for Test Value

- SED for Test can be executed remotely and in situ with diagnostic data gathered in real time
- Can be executed as part of Built-In Self-Test (BIST), Power-On Self-Test (POST), system audits, and operational measurements
- Requires only that the elements of the PCB that implement SED for Test power up and be operational
- SED for Test is completely out of band
- Can be used in implementing System JTAG (SJTAG – use of boundary scan within complex multi-board systems)
SED for Test provides a level of diagnostic granularity not usually found via in-system functional tests.

The same ScanWorks PCB tests used in production can be reused in situ and during repair.

Data can be uploaded into a ScanWorks benchtop system for diagnostic processing and reporting.

Addresses intermittent faults and “No Fault Found” (NFF) issues.
SED for Test Demonstration

- **SED Host - Altera Cyclone V SoC**
  - Dual Arm® Cortex®-A9 MPCore™ System On Chip (SoC) Cyclone® V SE FPGA
  - VxWorks Real-time operating system (RTOS)
  - Host for the embedded ScanWorks SEDPlayer which runs embedded JTAG/boundary-scan actions
  - Action results are stored in memory for retrieval

- **Target - ScanLite2**
  - 3 JTAG/boundary-scan devices
  - Target for JTAG/boundary-scan actions run by the SEDPlayer
  - Switches for fault simulation
Once the SEDPlayer and actions have been embedded, invoking the SEDPlayer, running actions, and storing results can be automated by a script or program. Ethernet and serial interfaces are not needed for a typical SED application (required to facilitate the demonstration).
## SED for Test Demonstration

<table>
<thead>
<tr>
<th>Fault Switch</th>
<th>Default Setting</th>
<th>Fault Setting</th>
<th>Fault Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW2</td>
<td>Norm</td>
<td>SA0</td>
<td>2 Drivers, 1 Receiver</td>
</tr>
<tr>
<td>SW3</td>
<td>Norm</td>
<td>SA0</td>
<td>1 Driver, 2 Receivers - Open</td>
</tr>
<tr>
<td>SW4</td>
<td>Norm</td>
<td>SA0</td>
<td>2 Drivers, 2 Receivers – 1 Pin Fail</td>
</tr>
<tr>
<td>SW5</td>
<td>Norm</td>
<td>SA0</td>
<td>TDO/TDI Error</td>
</tr>
<tr>
<td>SW6</td>
<td>Norm</td>
<td>SA1</td>
<td>Flip Flop Error</td>
</tr>
<tr>
<td>SW7</td>
<td>Norm</td>
<td>SA0</td>
<td>Memory – D0</td>
</tr>
<tr>
<td>SW8</td>
<td>Norm</td>
<td>Bridge</td>
<td>Flash Interconnect Fail</td>
</tr>
<tr>
<td>SW9</td>
<td>Norm</td>
<td>SA0</td>
<td>Memory – D1</td>
</tr>
<tr>
<td>SW10</td>
<td>Norm</td>
<td>Bridge</td>
<td>Address Fault</td>
</tr>
<tr>
<td>SW11</td>
<td>Norm</td>
<td>SA0</td>
<td>Short</td>
</tr>
<tr>
<td>SW12</td>
<td>Norm</td>
<td>Open</td>
<td>1 Driver, 1 Receiver</td>
</tr>
</tbody>
</table>

### Data Switch

<table>
<thead>
<tr>
<th>Data Type</th>
<th>Default Setting</th>
<th>Data Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1 (1-4)</td>
<td>Off</td>
<td>On</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3- Bits of Test Stimulus Data for U1 and LED’s</td>
</tr>
</tbody>
</table>
SED for Test Demonstration
A ScanWorks project and design was created to test the target.

Files transferred to the SoC (aside from the SEDPlayer.vxe) were generated during the normal ScanWorks test development process:
- .eie, .gen, _eie.gen, _eie.apl, .mbs

Files transferred from the SoC to ScanWorks were generated during the normal action run process:
- .log, .dtf

The number at the end of the SEDPlayer command tells it which action to run:
- SPV = 1, Interconnect = 2, MAV = 3

VxWorks was the operating system on the SoC but this could be any other operating system or RTOS; or SED for Test could even be implemented on a processor running without an operating system.
The resources required for the TAP Controller IP are small when compared to today’s FPGAs

- Uses < 4,000 Lookup Tables (LUTs)
- Uses less than < 75kb memory
- Action players run on the CPU
- Occupies < 2MB flash footprint
- Action data
  - Occupies ~ 300kB (typical) to >~1MB (for large designs)
Summary

- SED for Test embeds JTAG/boundary-scan test capabilities directly on a PCB
- Creates a powerful BIST without external hardware that can be used throughout the entire lifecycle of the PCB
- Can be executed as part of a POST or system audit, in situ, with data collected in real time
- Action diagnostic results can be uploaded and processed by a benchtop ScanWorks system
- Addresses intermittent faults and “No Fault Found” (NFF) issues
For More Information

- View our webinar, Embedded @Scale JTAG-based Debug of x86 Servers, [https://www.asset-intertech.com/resources/blog/2021/03/webinar-embedded-scale-jtag-based-debug-of-x86-servers/](https://www.asset-intertech.com/resources/blog/2021/03/webinar-embedded-scale-jtag-based-debug-of-x86-servers/)
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