Real Insight from Code to Silicon

SourcePoint® ScanWorks®

Squeezing Out More Test Coverage: Bridging the Gap Between Boundary Scan and Functional Test

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Agenda

- Test Coverage Considerations
- Coverage Assessment Methodology
- iNEMI PCOLA/SOQ/FAM Framework
- Bridging the Gap with the Component Action
- Functional Test with the Component Action
- Component Action Facts
- Component Model Structure
- Component Model Base Commands
- Functional Test Examples
- Demonstration
- Summary

Test Coverage Considerations

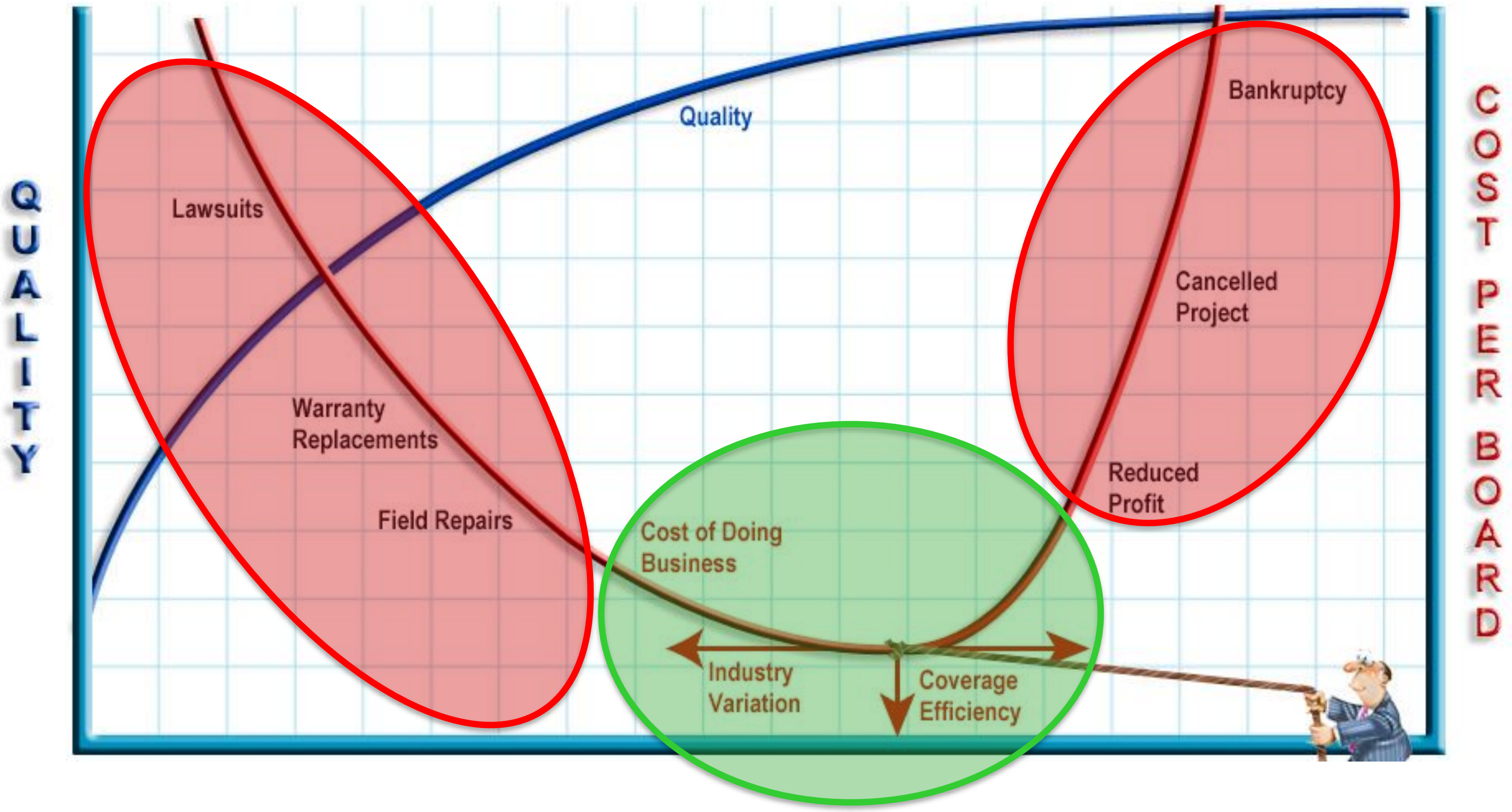
- Every PCB manufacturer would like to have 100% test coverage of their PCBs, but is this achievable?
- In manufacturing and test environments, time is money; PCB manufacturers must decide how much of each they are willing to invest to ensure a quality product
- PCB manufacturers must decide what percentage of PCB rejects and returns are acceptable due to reduced or untested areas of the PCB
- Each PCB manufacturer must decide what determines maximum test coverage for their product

Coverage Assessment Methodology

- When asked, engineers will say the goal of a PCB test plan is 100% coverage
- Achieving maximum test coverage is an iterative process with coverage being improved with each “turn” or redesign of the PCB
- Following design for test (DFT) guidelines during PCB design and layout produces maximum coverage

Coverage Assessment Methodology

- Coverage that is too low will result in warranty returns and high cost of product replacements in the field
- Coverage that is too high becomes expensive and can affect a product's total cost, driving up price and making it uncompetitive in the market
- The goal becomes achieving optimum test coverage (i.e., best coverage achievable given those restraining factors)



Coverage Optimization

SourcePoint® Platform for Software Debug and Trace

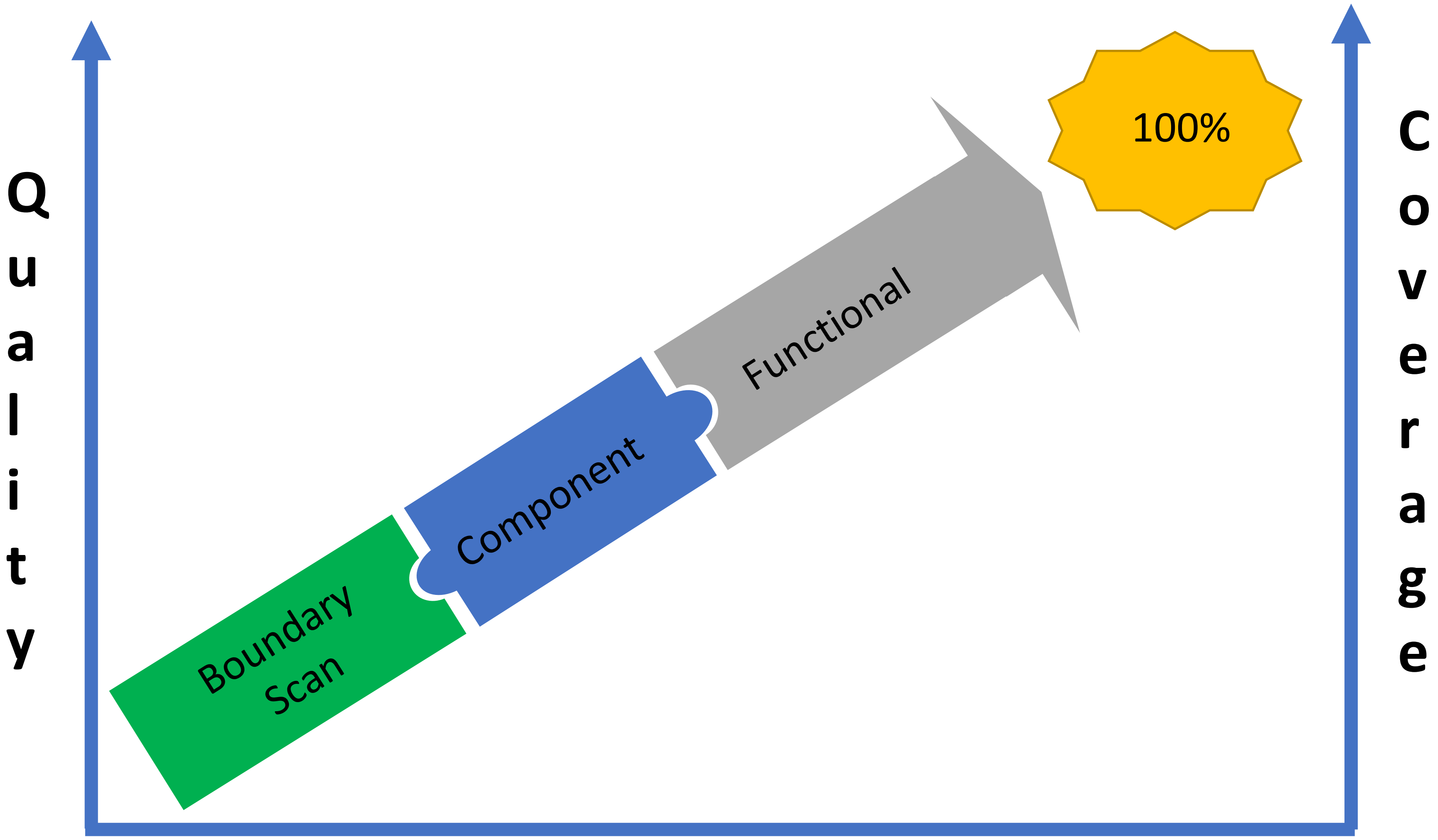
ScanWorks® Platform for Embedded Instruments

iNEMI PCOLA/SOQ/FAM Framework

Structural Devices	P	Presence	**PCOLA** tests are tests that verify the **P**resence of a chip in a socket or at a board location; that it is the **C**orrect chip; and is **O**riented correctly; receives power and is **L**ive; and is **A**ligned correctly	Boundary Scan Tests and External Equipment (ICT, X-Ray) and Visual Inspection
	C	Correctness		
	O	Orientation		
	L	Live		
	A	Alignment		
Structural Connections	S	Shorts	**SOQ** tests are tests that verify the connections/signals to the chip to be free of **S**horts and **O**pens; and can assess the **Q**uality of the connection's solder joints	Boundary Scan Interconnect Test and X-Ray
	O	Opens		
	Q	Quality		
Functional Connections	F	Features	**FAM** tests are tests that can operate or verify a **F**eature of the chip; can be applied **A**t-speed; and that allow a **M**easurement to be taken	Functional Tests
	A	At-Speed		
	M	Measurement		

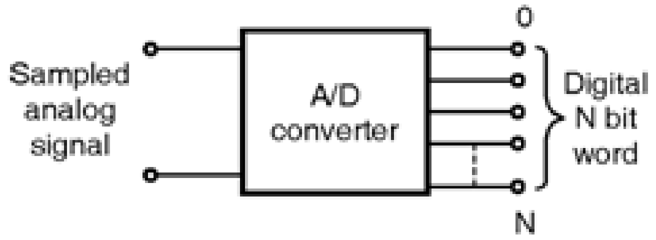
Bridging the Gap with the Component Action

- PCB functional test coverage can be realized by using boundary scan
- The ScanWorks Component Action can “bridge the gap” between boundary scan and functional test to enhance PCB test coverage

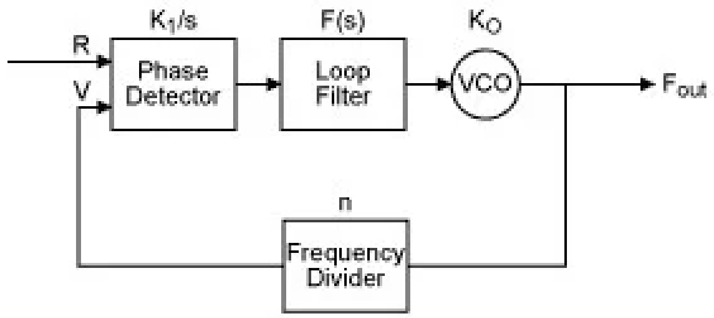


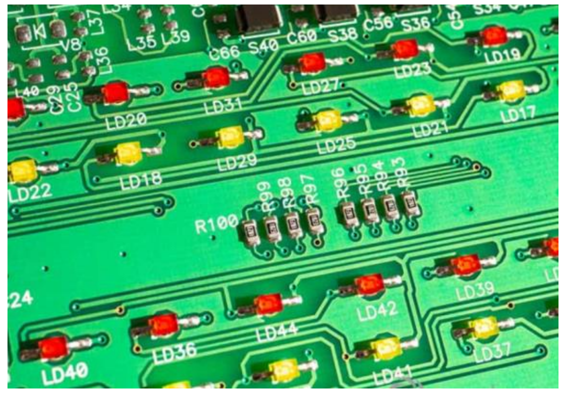
Functional Test with the Component Action

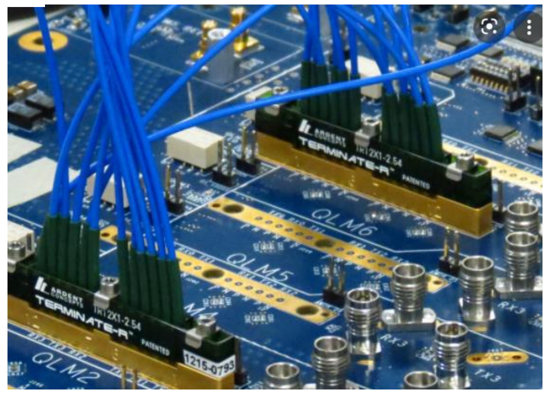
- The ScanWorks Component action is a general-purpose action that extends functional test coverage to a wide array of non-boundary scan devices
- ADCs/DACs
- Oscillators, clocks, PLLs
- LEDs
- Connectors
- I2Cs
- Ethernet PHYs
- Switches
- System monitors

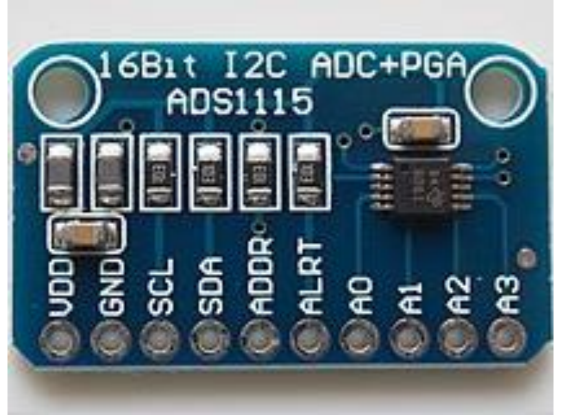


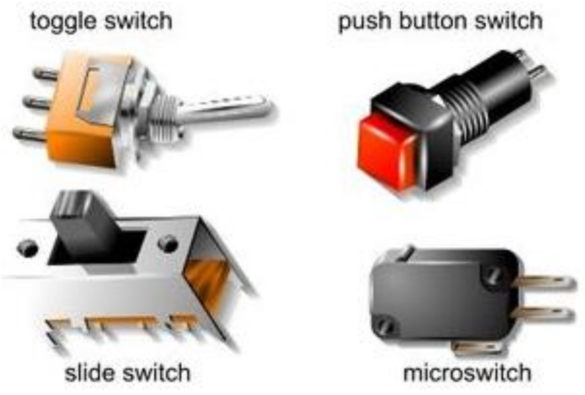
Digital
N bit
word
D/A
converter
Sampled
analog
signal

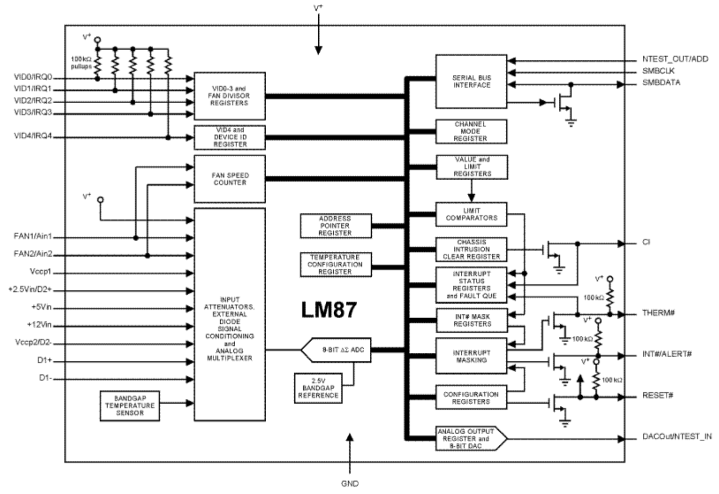






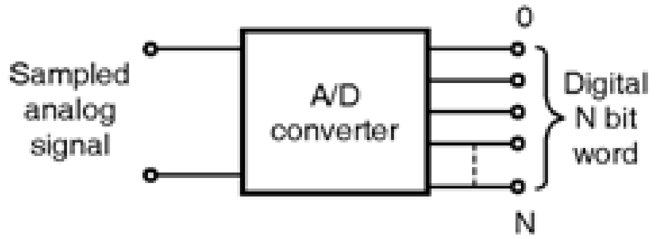


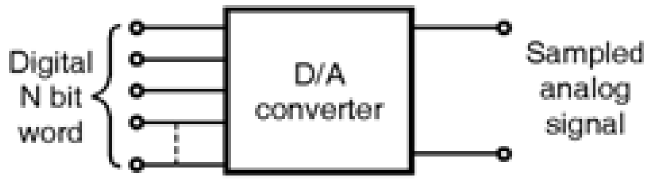


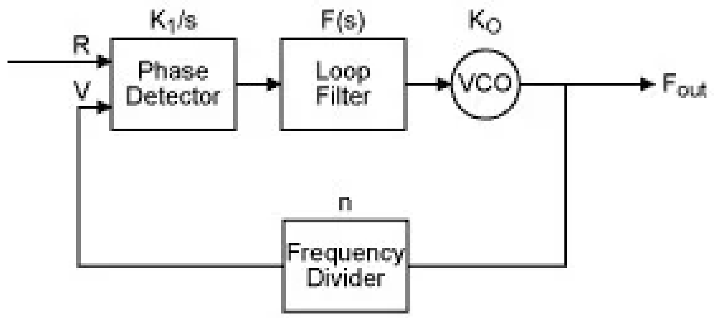


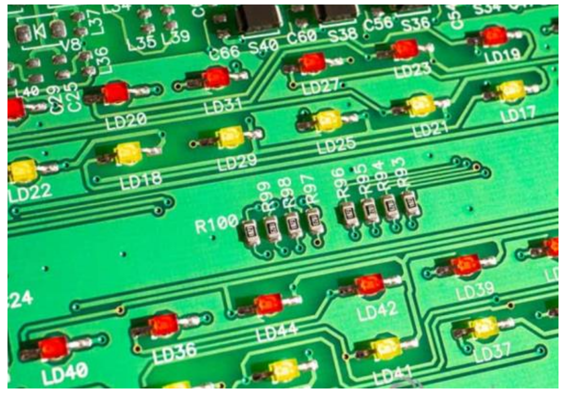
Functional Test with the Component Action

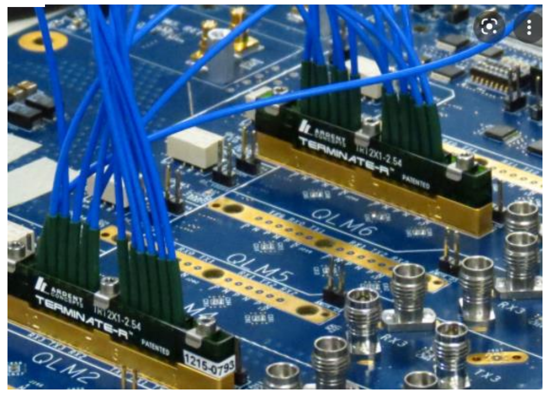
- The Component action uses the Tool Command Language (Tcl or Tickle) programming language along with a PCBs existing boundary scan resources to access non-boundary scan devices
- Any non-boundary scan device with boundary scan access, and an algorithm that can be modeled from its data sheet through Tcl, is a candidate for functional testing by the Component action

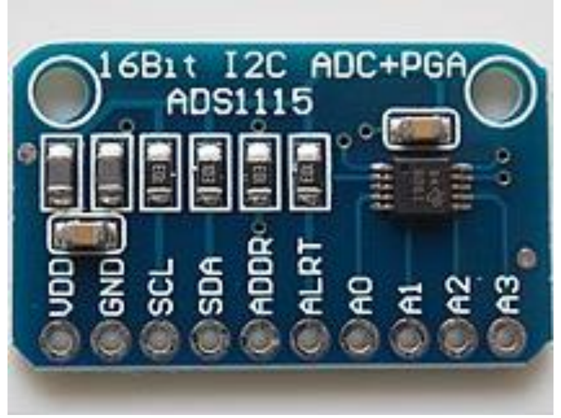


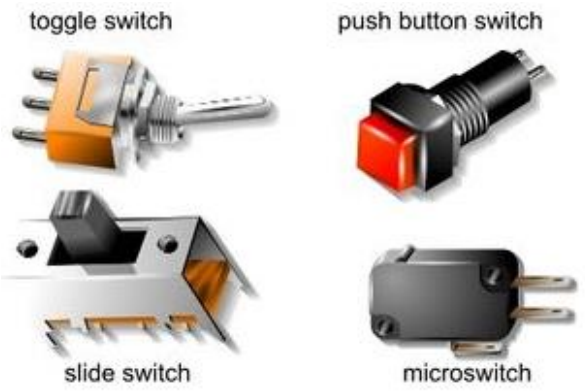


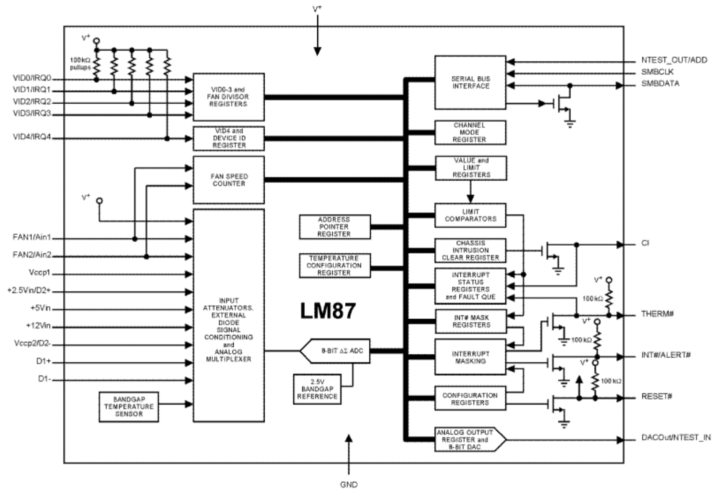






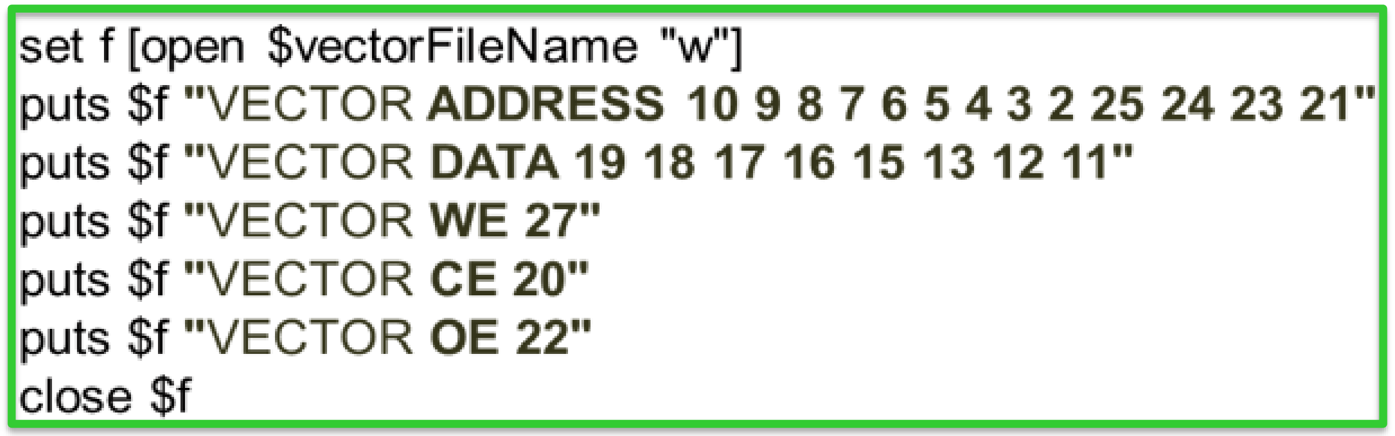




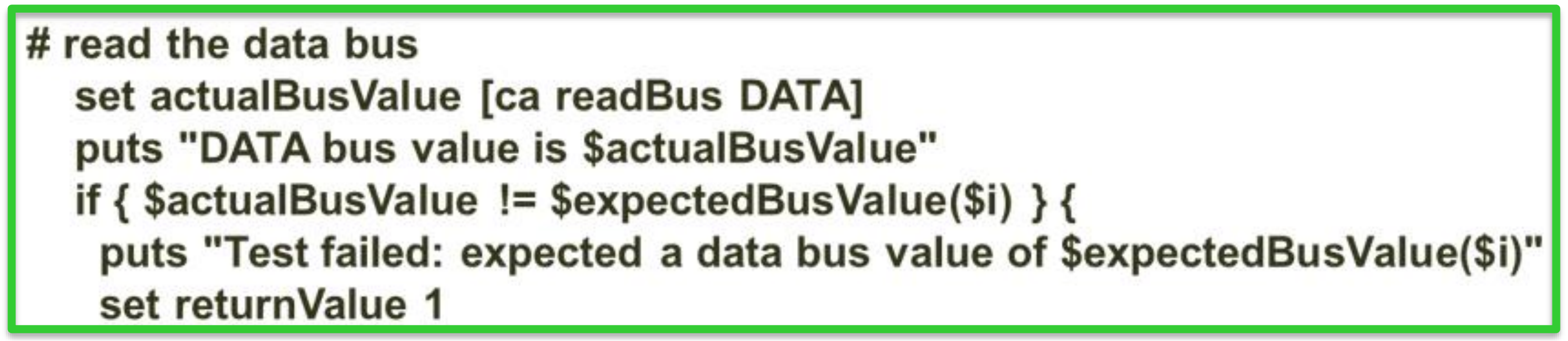


Component Action Facts

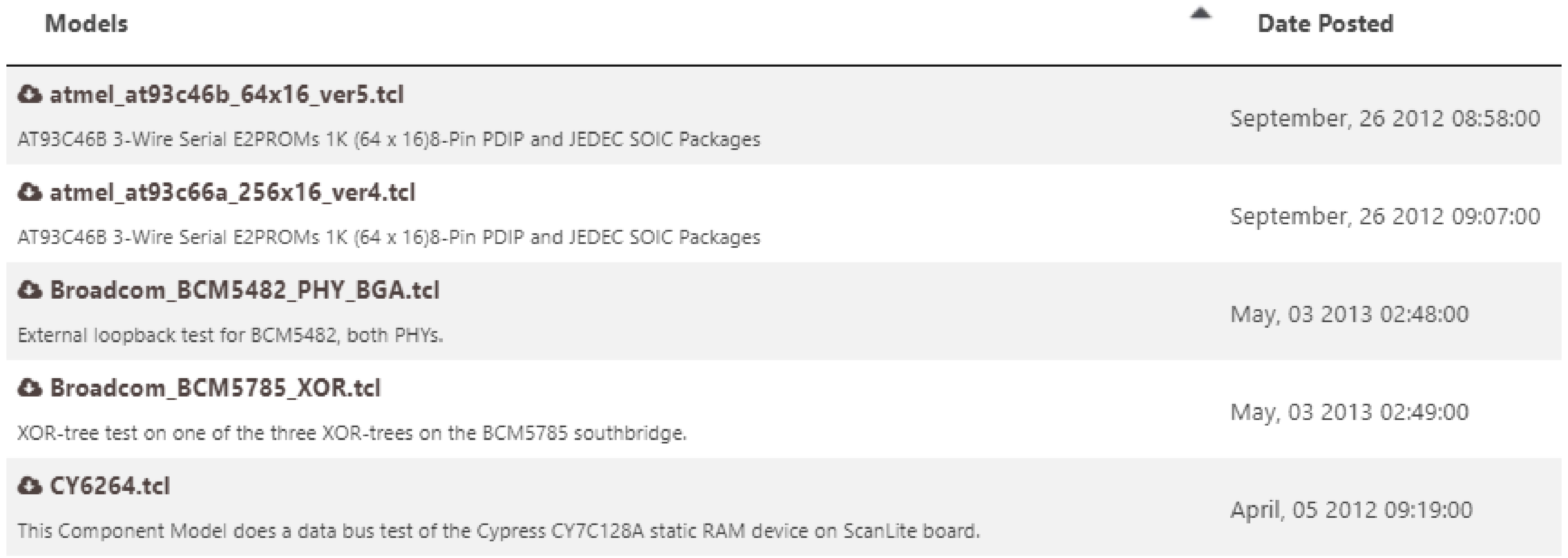
- The Tcl interpreter is included in ScanWorks
- The Tk package is also included in ScanWorks for creation of dialogs and GUIs
- Component models define the pins on the target device that require boundary scan access
- Component models are based on the operational algorithms of the non-boundary scan devices
- Component models are available for download from the ScanWorks Model Library for use as-is or as templates for model development



```
set f [open $vectorFileName "w"]
puts $f "VECTOR ADDRESS 10 9 8 7 6 5 4 3 2 25 24 23 21"
puts $f "VECTOR DATA 19 18 17 16 15 13 12 11"
puts $f "VECTOR WE 27"
puts $f "VECTOR CE 20"
puts $f "VECTOR OE 22"
close $f
```



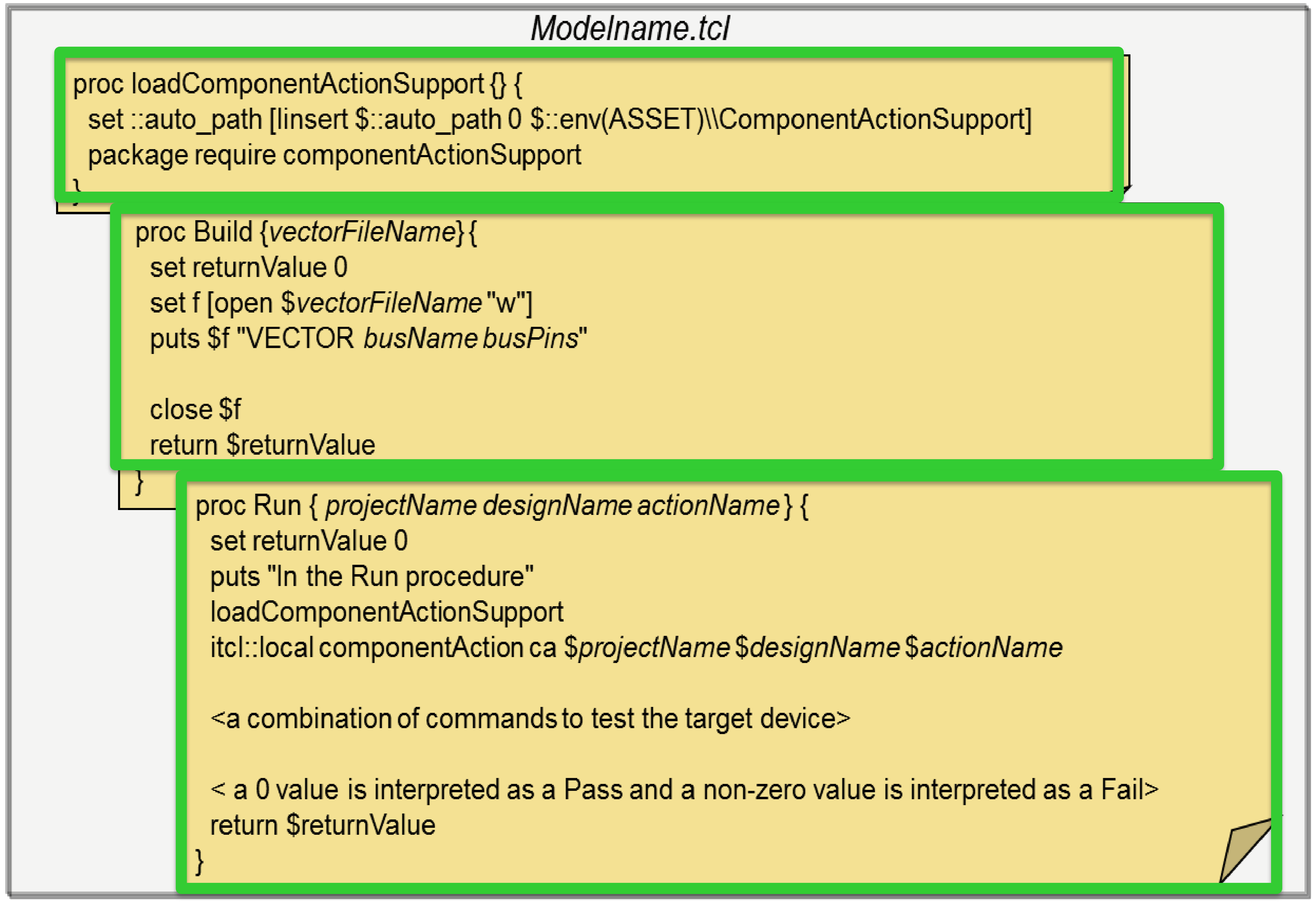
```
# read the data bus
   set actualBusValue [ca readBus DATA]
   puts "DATA bus value is $actualBusValue"
   if { $actualBusValue != $expectedBusValue($i) } {
     puts "Test failed: expected a data bus value of $expectedBusValue($i)"
     set returnValue 1
```



Models	Date Posted
atmel_at93c46b_64x16_ver5.tcl AT93C46B 3-Wire Serial E2PROMs 1K (64 x 16)8-Pin PDIP and JEDEC SOIC Packages	September, 26 2012 08:58:00
atmel_at93c66a_256x16_ver4.tcl AT93C46B 3-Wire Serial E2PROMs 1K (64 x 16)8-Pin PDIP and JEDEC SOIC Packages	September, 26 2012 09:07:00
Broadcom_BCM5482_PHY_BGA.tcl External loopback test for BCM5482, both PHYs.	May, 03 2013 02:48:00
Broadcom_BCM5785_XOR.tcl XOR-tree test on one of the three XOR-trees on the BCM5785 southbridge.	May, 03 2013 02:49:00
CY6264.tcl This Component Model does a data bus test of the Cypress CY7C128A static RAM device on ScanLite board.	April, 05 2012 09:19:00

Component Model Structure

- The Proc loadComponentActionSupport procedure loads all of the necessary ASSET Component Action classes when the action is run
- Pins on the target non-boundary scan device to be functionally tested are listed in the proc Build procedure
  - This information is used along with UUT netlist to find access to the target non-boundary scan device
- The proc Run procedure defines the algorithm necessary to functionally test the target non-boundary scan device
  - Uses the buses defined in the proc Build and the user-supplied commands to communicate with the target non-boundary scan device



Modelname.tcl

```
proc loadComponentActionSupport {} {
  set ::auto_path [linsert $::auto_path 0 $::env(ASSET)\\ComponentActionSupport]
  package require componentActionSupport
}
```

```
proc Build {vectorFileName}{
  set returnValue 0
  set f [open $vectorFileName "w"]
  puts $f "VECTOR busName busPins"

  close $f
  return $returnValue
}
```

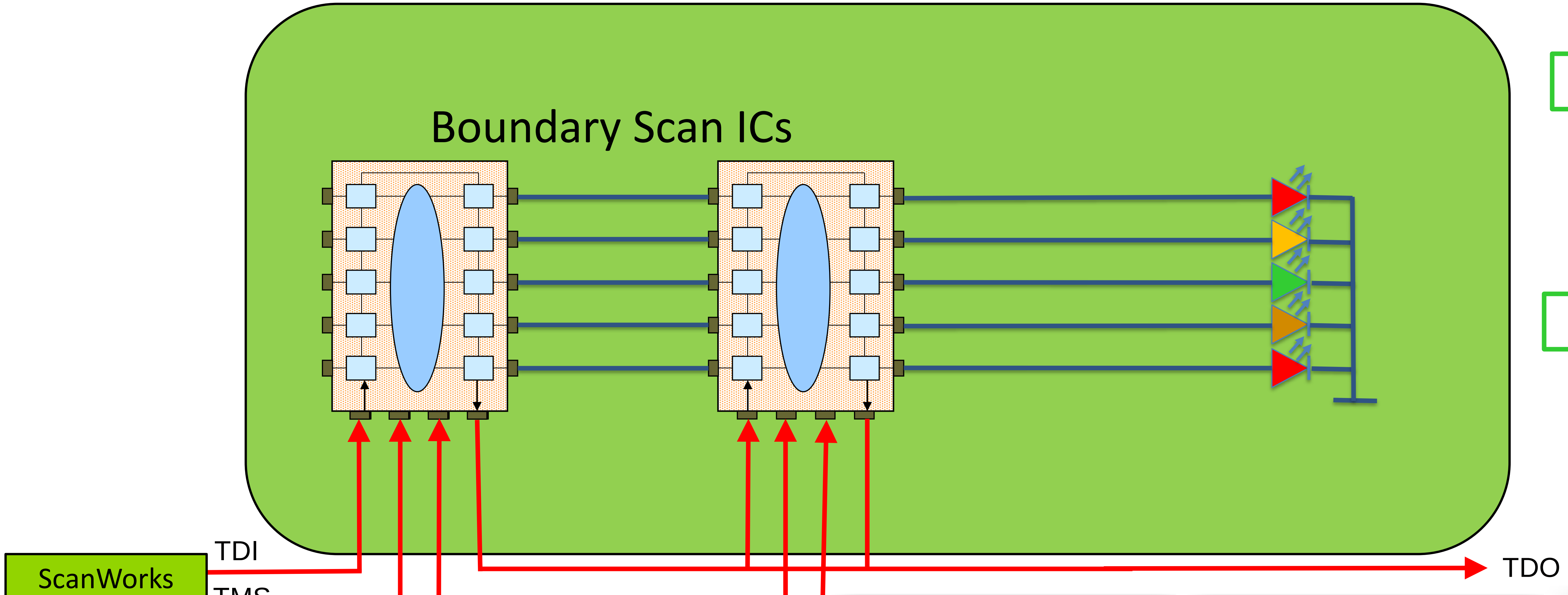
```
proc Run { projectName designName actionName } {
  set returnValue 0
  puts "In the Run procedure"
  loadComponentActionSupport
  itcl::local componentAction ca $projectName $designName $actionName

  <a combination of commands to test the target device>

  < a 0 value is interpreted as a Pass and a non-zero value is interpreted as a Fail>
  return $returnValue
}
```

Component Model Base Commands

- Command: setBus
  - Sets the TDI buffer for the boundary scan cells used to access the pins of the non-Boundary Scan device
- Command: disableBus
  - If possible, disables the boundary scan driver cells used to drive the pins
- Command: DRScan
  - Performs a DR scan to scan in the contents of the TDI buffer and captures the data in the TDO buffer that is scanned out
- Command: readBus
  - Performs a DR scan and reads the data from the TDO buffer for the bus pin
- See the documentation “Using Component Actions” at c:\scanworks\doc for more information

Functional Test Example

LED Verification



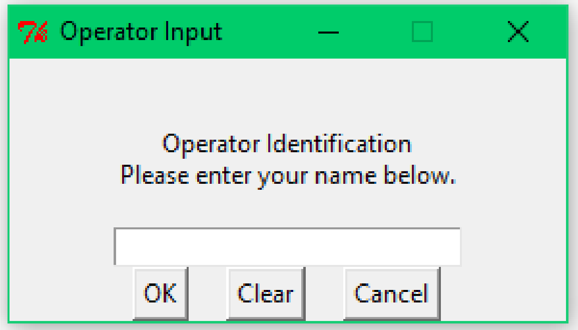
ScanWorks Component Action

Tcl Model File
Algorithm
Blink LEDs

Visual Inspection

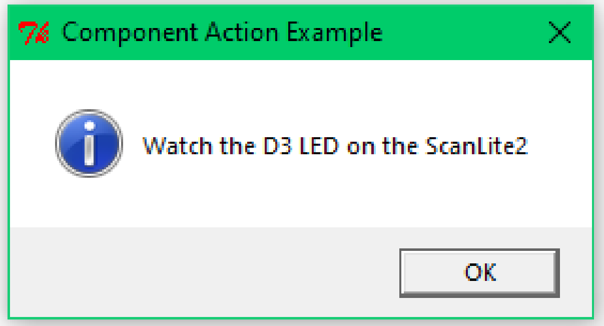
Optical Sensor

Optical Sensor



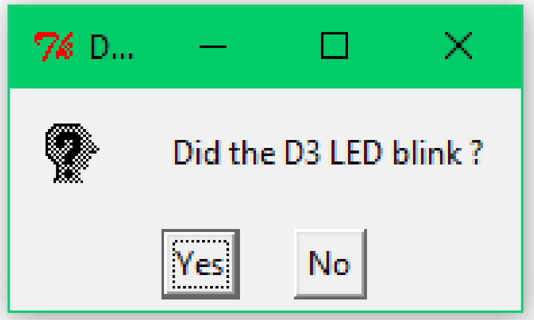
Operator Input

Operator Identification
Please enter your name below.



Component Action Example

Watch the D3 LED on the ScanLite2



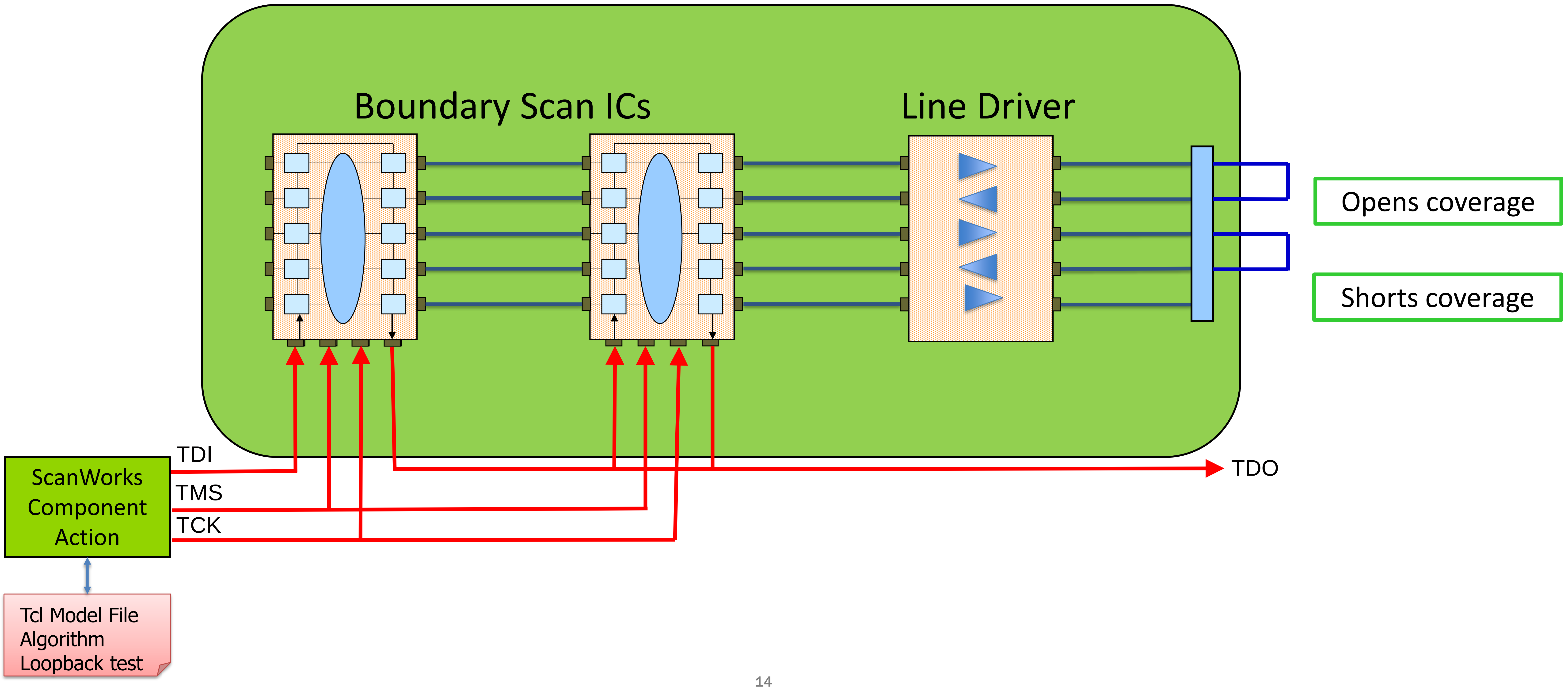
D...

Did the D3 LED blink ?

Operator input GUIs created with Tk

Functional Test Example

Connector Verification



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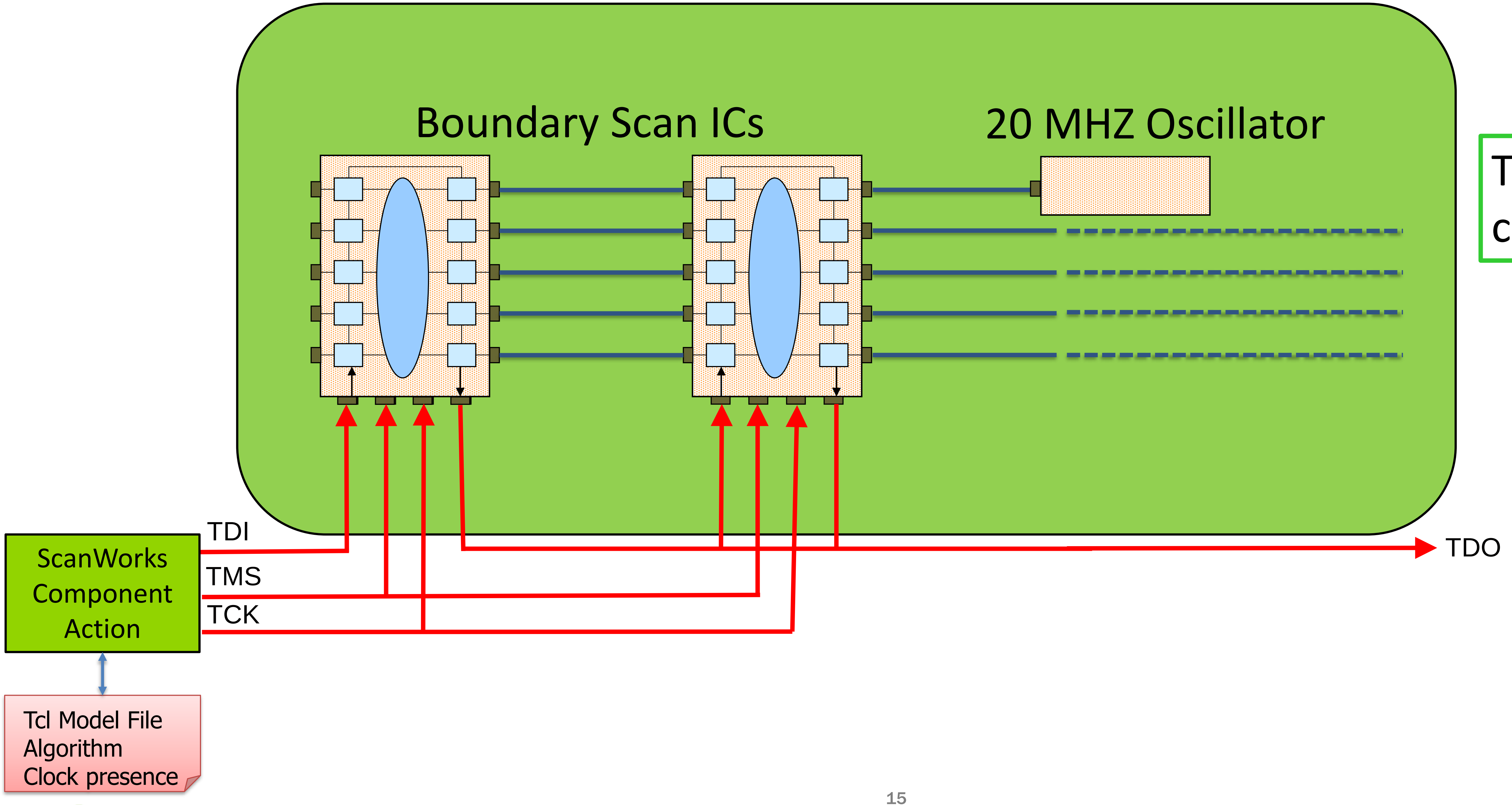
Functional Test Example

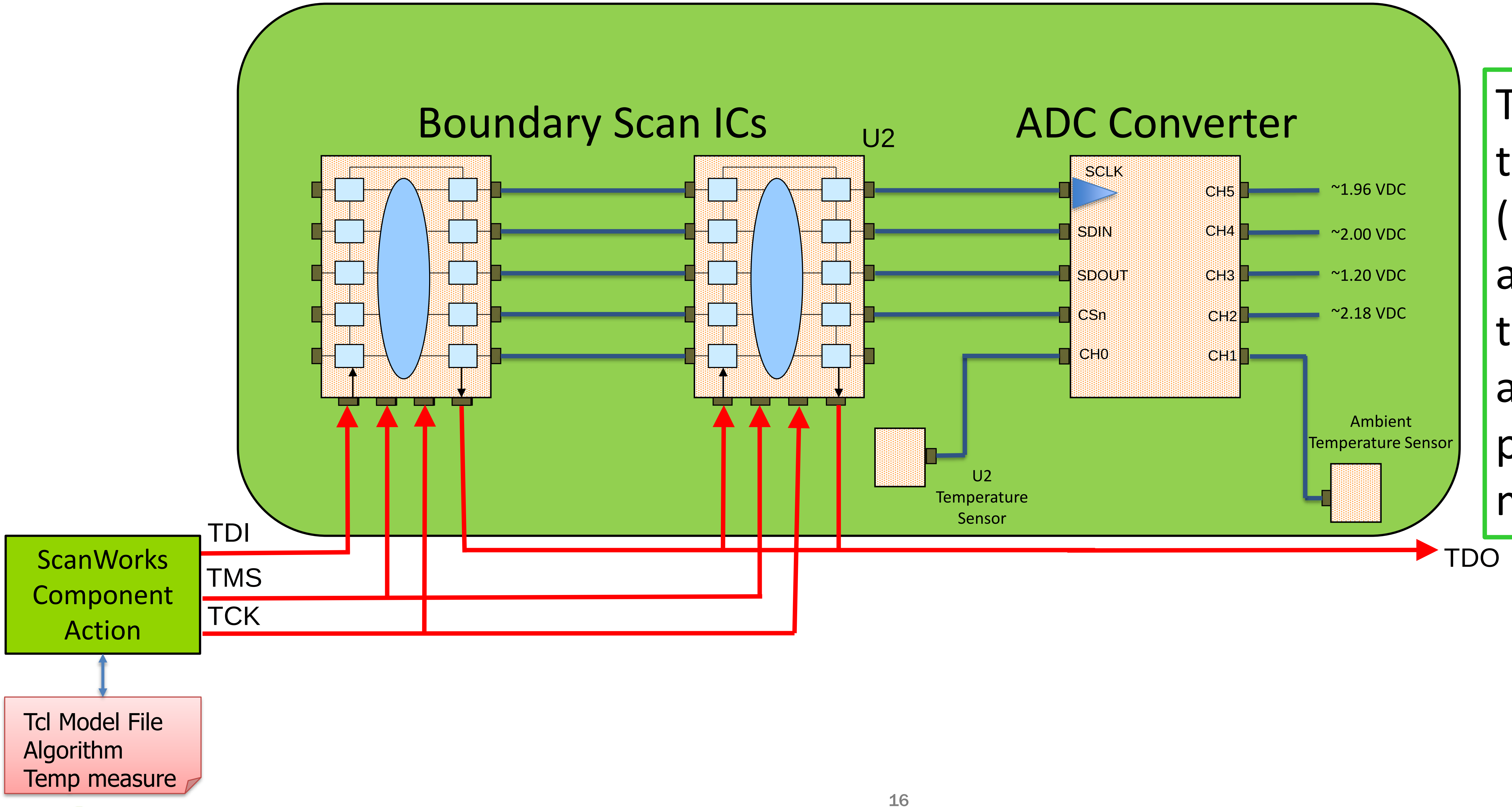
Clock Verification



Test for oscillator clock transitions

Functional Test Example

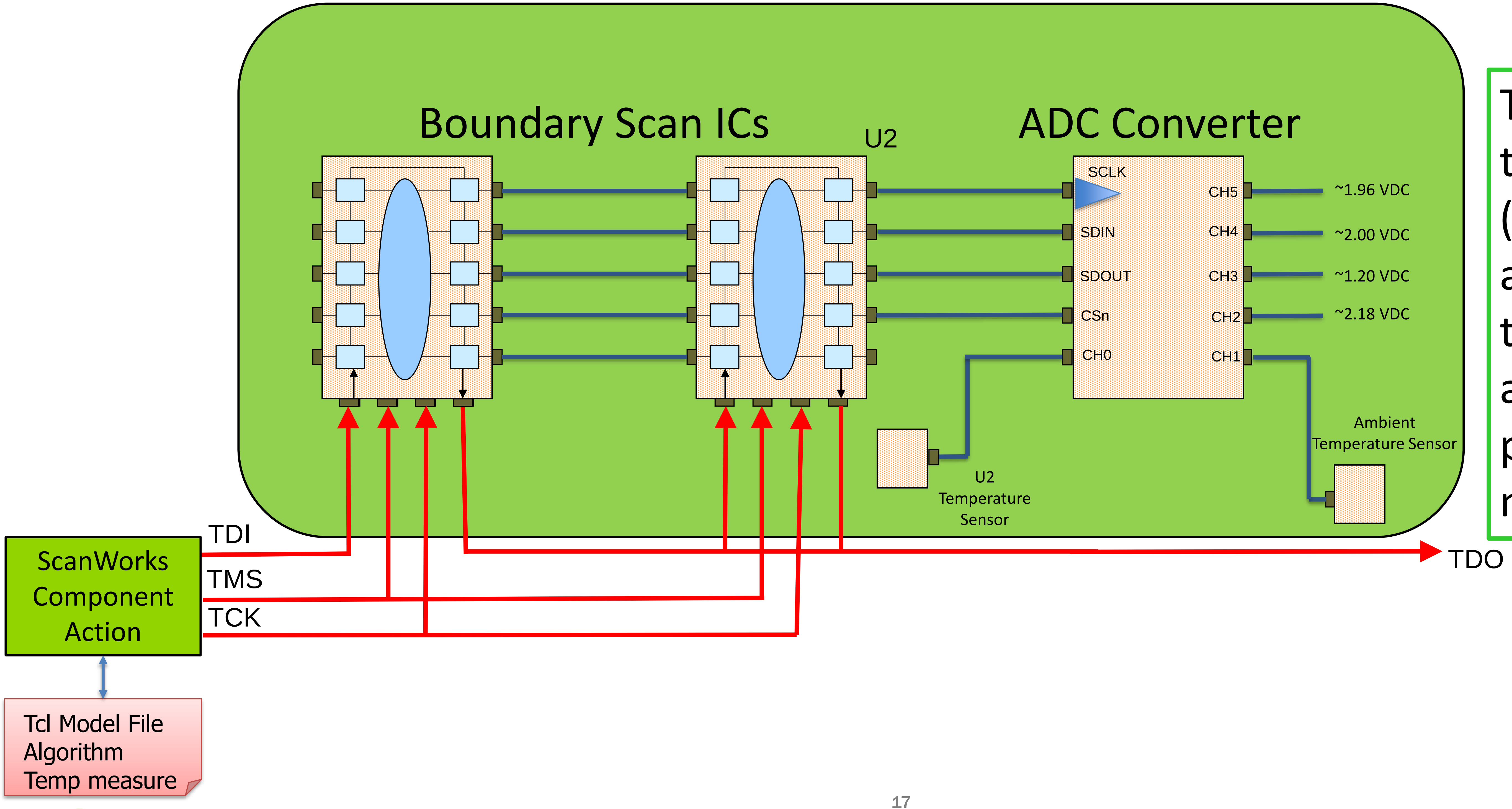
ADC with Temperature Measure



Test for device temperature (U2) vs. PCB ambient temperature along with power supply measurements

Demonstration

ADC with Temperature Measure

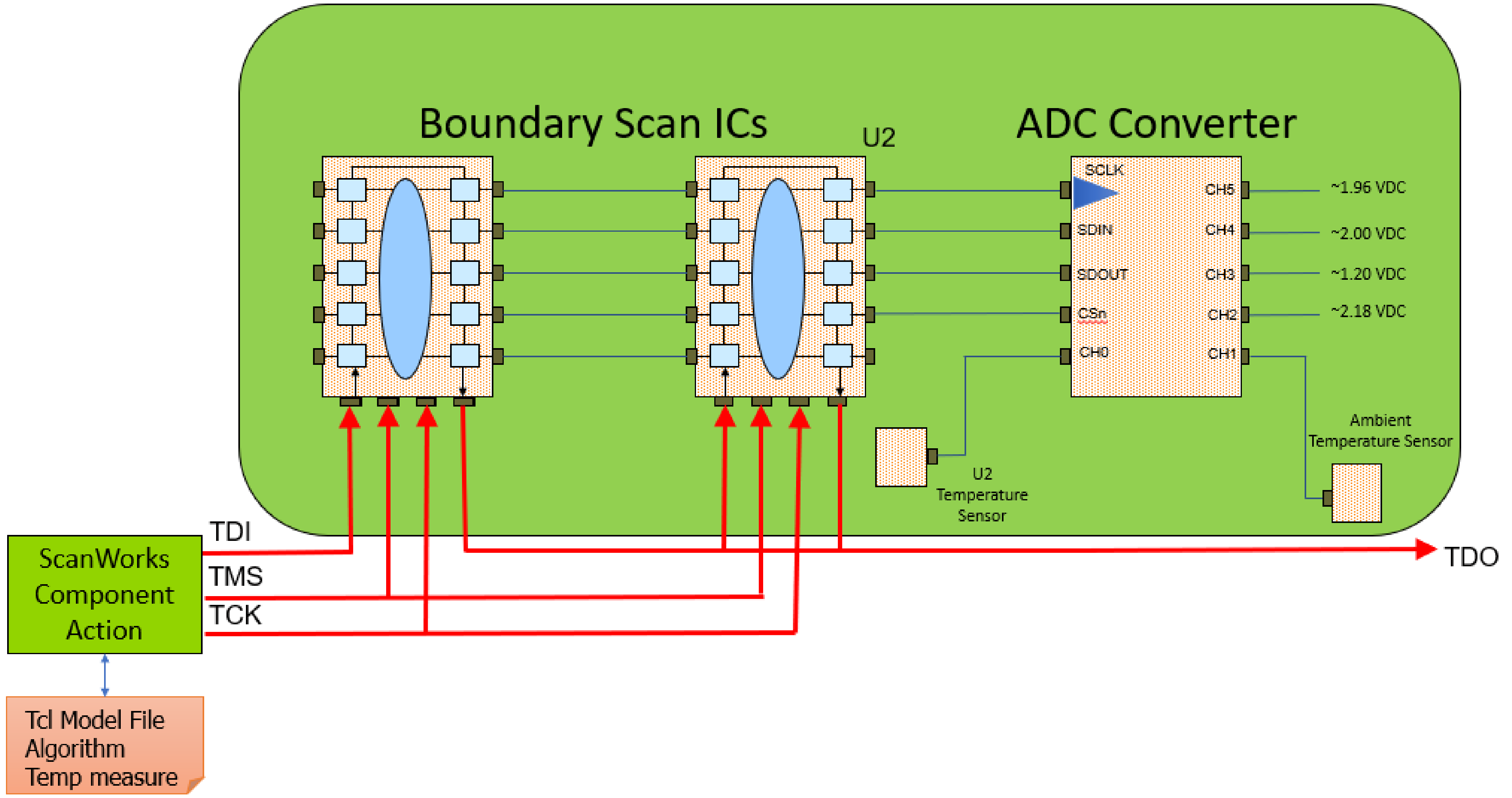


Test for device temperature (U2) vs. PCB ambient temperature along with power supply measurements

Summary

- Bridging the boundary scan and functional test gap with the Component action has many positive results
  - Adds functional testing to areas of the PCB that might have gone untested
  - One station for structural, programming and functional testing reduces PCB handling and manufacturing cost
  - Reduces need for large equipment saving factory floor space
- Failing devices can be identified during manufacturing where the cost to repair is lower as compared to latter production phases or at product release
- Functional test can be implemented through 3rd party applications such as LabVIEW, TestStand, along with boundary scan test
- ASSET provides a library of Component models for use as-is or as templates for model development so it’s easy to get started

ADC with Temperature Measure



For More Information

- Go to our blog, Structural versus Functional Test, and Test Coverage versus Diagnostics, https://www.asset-intertech.com/resources/blog/2010/12/structural-versus-functional-test/
- Download our eBook, Embedded JTAG for Boundary-Scan Test, https://www.asset-intertech.com/resources/eresources/embedded-jtag-boundary-scan-test/
- View our webinar, Onboard Fast Flash Programming Technology Innovations - Addressing Offboard Challenges, https://www.asset-intertech.com/resources/videos/webinar-recording-onboard-fast-flash-programming-technology-innovations-addressing-offboard-challenges/

Questions and Contact Information

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