Real Insight from Code to Silicon

SourcePoint™ ScanWorks®

In-System Fast Flash Programming Technologies

Larry Osborn

Project Manager for:
ScanWorks FPGA-Flash Programming
ScanWorks Processor-based Fast Programming
ScanWorks Embedded Diagnostics
SourcePoint Intel/AMD Debugger

June 29, 2021
Offboard vs. Onboard
Technology Trends
ScanWorks Addressing the Trends
  Technology Trends
  SoC Trends
  FPGA Trends
ScanWorks Programming Toolbox
  Boundary-Scan Flash
  Processor-based Flash
  FPGA-based Flash
  Controller-based Flash
ScanWorks Programming Methods
  Programming Method Considerations
  Speed Comparisons

Demo
  Zedboard
    BST
    PFx
    FFP
Questions
Offboard (preprogramming)
- Inventory management
- Engineering Change Orders (ECO)
- Software updates
- Device shortages

Onboard (in-system programming)
- No Inventory management issue
  - Preprogramming
  - Device Inventory shortage
- ECO minimal impact
- Software updates expected
- UUT design dictates
  - Manufacturing beat rate
  - Speed of programming possible
Market Trends
- Design starts
  - Artificial Intelligence
  - 5G
  - Defense - towards FPGAs for Cyber Security issues
- Automated Driving Solutions (ADS)
- Hyperscale Data Centers (HDC)
- Domain-specific architectures (DSA)
- Adaptive Computing
- Prototyping
SoC Trends

- Multi-core
  - Homogenous
  - Heterogenous
- Additional cores
  - FPGA
  - GPU
  - Embedded Controllers
- Flash expansion
  - G-bit SPI support
  - SDMMC/eMMC
  - NAND
FPGA Technology Trends

- FPGA Complexity Growth
  - 9 Million System Logic Cells
  - 2,072 User IO Cells
  - 80 28G Transceivers
  - UltraRAM
  - High Bandwidth Memory (HBM)
- Power consumption
- Adaptability curves
Customer Design Dictates
Fast Flash Programming methods possible.
Where is the flash device connected SoC, FPGA, Processor or JTAG only?

For the **SoC** that has both a processor core and FPGA core, is the flash device connected to processor core or to the FPGA fabric?

For the **FPGA** is there a system clock?
   System clock should run faster than sclk
   Instrument for Configuration SPI require special notation for pin assignment.

What is the **BST** chain clock rate? Slowest device clock rate in the chain determines the chain clock rate.

How large is the image?
ScanWorks

Boundary-Scan Test (BST)
Processor-based Fast Programming (PFP)
FPGA-based Fast Programming (FFP)
ScanWorks Boundary-Scan Test (BST)

- Design to simplify the test complexity
  - Automated
  - Model-based
  - Incremental test

- Programming support via JTAG
  - SPI, QSPI, OSPI
  - I2C, NAND, NOR
  - eMMC
PFx Product Family

- **PFx**
  - **PFP** – Processor-based Fast Programming
    - Fast programming (MB per second) a single solution for prototype and production
  - **PFT** – Processor-based Functional Test
    - At-speed functional test coupled with structural
  - **PFTDDR** – Processor-based Functional Test for DDR
    - DDR Test and Tune - Testing at GB per second speeds
      - Zynq-7000 tuning supported
      - UltraScale microcode
PFP is a software target agent designed for programming at device speed.

- Provides in-target, in-system programming.
- Eliminating costly pre-programmed inventory.
- Programming at MBytes per sec.

Improved Productivity and Improved Manufacturing beat-rate.
ScanWorks FPGA-based Fast Programming (FFP)

- In-system programming
- Downloadable IP to shorten the programming time
Where the Technologies Apply

- JTAG
- Network
- RIC-1400
- SPI Direct
- SPI DIO
- SPI Header
- Processor
- FPGA
- SoC
- Flash
- Boundary Scan
- SPI
- BST
- FFP
- FFP/BST
- UUT
- Network
ScanWorks BST Programming Support

Network

RIC-1400

SPI Direct

SPI DIO

BST Programming

JTAG

UUT

SoC

Processor

FPGA

SPI Header

SPI

BST

Flash

FPGA

Flash

Boundary Scan

BST

UUT

BST

SPI Direct

FPGA

Flash

Boundary Scan

BST

UUT

BST

Flash

© 2021, ASSET InterTech, Inc.
ScanWorks SPI DIO and SPI Direct Programming Support

- JTAG
- UUT

- SPI Direct
  - RIC-1400 Only
- SPI DIO
  - All controller but slower than SPI Direct

- SPI Direct/SPI DIO
  - SPI Header
  - Flash
1) Short Chain – reduces the FPGA scan length to increase the data throughput

2) SPI Flash IP – IP embedded within the FPGA to increase the programming throughput

Note:
1) Supported Silicon Vendors Only: Xilinx, Altera, Microchip
2) FPGA Fabric Clock Driven by FFP
ScanWorks Processor-based Fast Programming

SoC

PFP

JTAG

UUT

SPI

NOR

NAND

QSPI

SD

MMC

JTAG - Small images

Ethernet - Large images

Ethernet Processor connection only

Processor

FPGA

RIC-1400

Network

SourcePoint

ScanWorks

© 2021, ASSET InterTech, Inc.
Programming Methods Consideration

- BST
  - SoC boundary scan
    - NAND, NOR, SPI, QSPI, eMCC
    - Connected to JTAG enable device
  - SPI DIO
    - GPIO control
- SoC – Processor System or FPGA Fabric
  - If Processor – PFP
    - NAND, NOR, SPI, QSPI, SD/MMC, eMMC
    - Ethernet data download
  - If Programmable Logic – FFP
- FPGA Standalone
  - FFP
- SPI Direct – RIC-1400
  - Flash Header access
# ScanWorks Programming Speed Technology Comparison

<table>
<thead>
<tr>
<th>Access Method</th>
<th>TCK</th>
<th>SoC Clock</th>
<th>FPGA Clock</th>
<th>Programming File Size</th>
<th>Erase/Program/Verify Time</th>
<th>Improvement</th>
<th>Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boundary-Scan Chain</td>
<td>12 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td><strong>35 minutes</strong> (2100 seconds)</td>
<td>-</td>
<td>UUT JTAG Clock Rate /BST Register</td>
</tr>
<tr>
<td>Short Chain</td>
<td>12 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td><strong>4 minutes</strong> (240 seconds)</td>
<td>~9x</td>
<td>Supported FPGA Families</td>
</tr>
<tr>
<td>SPI DIO</td>
<td>45 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td>2 minutes 5 seconds</td>
<td>17x</td>
<td>SPI Header</td>
</tr>
<tr>
<td>PFx Programming</td>
<td>30Mhz</td>
<td>800 MHz</td>
<td>NA</td>
<td>1MB</td>
<td>11 seconds</td>
<td>190x</td>
<td>UUT JTAG Clock Rate</td>
</tr>
<tr>
<td>PFx Programming Via Ethernet</td>
<td>30Mz</td>
<td>800 MHz</td>
<td>NA</td>
<td>1 MB</td>
<td>2.4 seconds</td>
<td>78x</td>
<td>Supported SoC Only</td>
</tr>
<tr>
<td>SPI Flash Programming</td>
<td>30 MHZ</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>1 MB</td>
<td>2.3 seconds</td>
<td>91x</td>
<td>Supported FPGA Families</td>
</tr>
<tr>
<td>SPI Direct</td>
<td>10 MHz</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>1 MB</td>
<td>2.3 seconds</td>
<td>91x</td>
<td>RIC-1400 and SPI Header</td>
</tr>
</tbody>
</table>
PL-PMOD 32MB SPI
ScanWorks Programming Demo
# ScanWorks Programming Speed Technology Comparison

## Zedboard – XC7Z020

<table>
<thead>
<tr>
<th>Access Method</th>
<th>TCK</th>
<th>SoC Clock</th>
<th>FPGA Clock</th>
<th>Programming File Size</th>
<th>Program Time</th>
<th>Improvement</th>
<th>Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boundary-Scan Chain</td>
<td>30 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td>10.5 minutes</td>
<td></td>
<td>UUT JTAG Clock Rate / BST Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(638 seconds)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Short Chain</td>
<td>30 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td>2 minutes</td>
<td>5.3x</td>
<td>Supported FPGA Families</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(119 seconds)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPI DIO</td>
<td>30 MHz</td>
<td>NA</td>
<td>NA</td>
<td>1 MB</td>
<td>1.3 minutes</td>
<td>8x</td>
<td>UUT JTAG Clock Rate / BST Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(80 seconds)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PFx Programming Via JTAG</td>
<td>30 MHz</td>
<td>800 MHz</td>
<td>NA</td>
<td>1MB</td>
<td>8.7 seconds</td>
<td>74x</td>
<td>Supported SoC Only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FPGA-based SPI Flash Programming</td>
<td>30 MHz</td>
<td>NA</td>
<td>100 MHz</td>
<td>1 MB</td>
<td>3.4 seconds</td>
<td>185x</td>
<td>Supported FPGA Families</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PFx Programming Via Ethernet</td>
<td>30 MHz</td>
<td>800 MHz</td>
<td>NA</td>
<td>1 MB</td>
<td>2.4 seconds</td>
<td>262x</td>
<td>Supported SoC Only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPI Direct</td>
<td>30 MHz</td>
<td>NA</td>
<td>?</td>
<td>1 MB</td>
<td>1.2 seconds</td>
<td>525x</td>
<td>RIC-1400 Only UUT SPI Header</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
We demonstrated 7 different ScanWorks actions to address the challenges of increased technology complexity, expansive software growth, and all accomplished via in-system programming with greater programming performance.

The UUT design will ultimately determine the speed at which the devices can be programmed, and which programming technology is best suited.

These solutions will save time in development and in production.

Lower costs can be achieved with ScanWorks onboard solutions than offboard solutions.
Resources

- **BST**

- **FFP**

- **PFP**
Questions and Contact Information

Contact Information:
Larry Osborn
7161 Bishop Rd. Ste. 250
Plano, TX 75024
losborn@asset-intertech.com
www.asset-intertech.com
Real Insight from Code to Silicon