ScanWorks FPGA-based Flash Programming A Two Instrument Example Guide for Opal Kelly XEM6002 Hardware

by Larry Osborn

Larry Osborn

Larry Osborn, Senior Product Manager, at ASSET InterTech, has over 30 years of experience in product management, hardware/software product design and development, product delivery to the marketplace and user support. Over the years, Larry has a proven track record for identifying user needs and opportunities in the marketplace, providing innovative solutions and exceeding the expectations of users. At ASSET, Larry is responsible for the profit and loss for a product group. Prior to ASSET, he has held positions with Lockheed Martin, OCD Systems, Wind River, Hewlett-Packard, Ford Aerospace, and Intel® Corporation. He holds a bachelor's degree in Computer Science from the University of Kansas and various technical and marketing training certifications.

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Purpose

The purpose of this document to instruct the user on the steps nessssary in using FPGA Module in the Design Resources tab found in ScanWorks 4.8 and higher. This is a new feature that provides the ability to create embedded instruments within an FPGA using ScanWorks FPGA-based Contolled Test (FCT) and ScanWorks FPGA-based Flash Programming (FFP) tools. To use this feature, either FCT or FFP tools must be licensed.

This document will cover only the ScanWorks FPGA-based Flash Programming (FFP) project setup and implementation.

The implemenation will cover the generation of the embedded instruments and the creation of the project actions necessary to exercise the embedded instruments.

The target for this manual is an Opal Kelly XEM6002 target with a PmodSF SPI Flash.

Notes:

Embedded Tester Generator (ETG) is the UI software component of the ScanWorks FPGA-based Fast Programming.

The ETG Release Notes can be found at C:\ScanWorks\ETG\ETG_ReleaseNotes.pdf please review the release notes to see the most current information on the release.

Microsemi Libero tool produces STAPL files not SVF and thus the ScanWorks action to program a Microsemi device should use a STAPL action and not an SVF action.

Customers must have access to in-house FPGA synthesis tools.

Note that once you define FPGA pins as output/bidir for an instrument, you cannot use the same pins for another instrument within the same embedded tester.

With ETG you could define two different Embedded Testers, however at this time ScanWorks cannot handle multiple embedded testers.

All FPGA pins being declared within ETG, should be researched in the FPGA datasheet, to see if they are declared as dedicated pins. If so, manual tool manipulation may be needed.

The SPI Flash IP, SPI Master and Frequency Measure instruments require that the FPGA have an active clock input. This clock will be used as a reference and while 100 MHz would be ideal, the acceptable range is 50-200 MHz

The Frequency_Measure IP instrument currently requires a free-running TCK, therefore the USB-100 controller will not work with this type of action.

ASSET support should always get the FPGA and target part numbers from the customer and run them by ASSET development to confirm that they are supported.

If the combined project name and embedded instrument names are too long, you might not be able to import the exported ETG project, Case-32462.

Normally you can use the Make button to compile just the .hgl file. There is currently a bug which requires that you use the Build button instead of the Make button. Case-27013.

Overview

This FPGA Module Example will instruct you on the following:

a. Install prerequisites
b. Build and download the ASSET Web Deployment Installer
c. Install ScanWorks and ETG
d. Request and install ScanWorks and FFP licenses
e. Configure the Embedded Tester Generator (ETG)
f. Use ETG to generate the FFP/ETG files
g. Create a ScanWorks project/design
h. Generate and run FFP actions

Prerequisites – Download and install

1. FPGA EDA Tools

To generate an FPGA instrument project, you must have access to the FPGA device manufacturer's synthesis tool for that specific FPGA. For this Example, which uses a Xilinx Spartan-6, XC6SLX9 FPGA, the ISE Design Tools are needed. The Xilinx_ISE_DS_14.7_1015_1.tar free installation can be downloaded from the Xilinx Download website. A username and password are needed on the Xilinx website.

a) Download Xilinx_ISE_DS_14.7_1015_1.tar file from Xilinx website.
b) Unzip the above downloaded .tar file to a temporary folder.
c) As administrator, run the xsetup.exe file from the temporary folder. Select all defaults except for selecting ISE WebPACK as the package to install and selecting 'Get Free ISE WebPACK License' for acquiring a License.

2. Opal Kelly Tools

This manual uses the Opal Kelly XEM6002 target with a PmodSF SPI Flash connected to POD 1 or POD 3 (depending on the action) on the Opal Kelly board. Shown in figure 1.

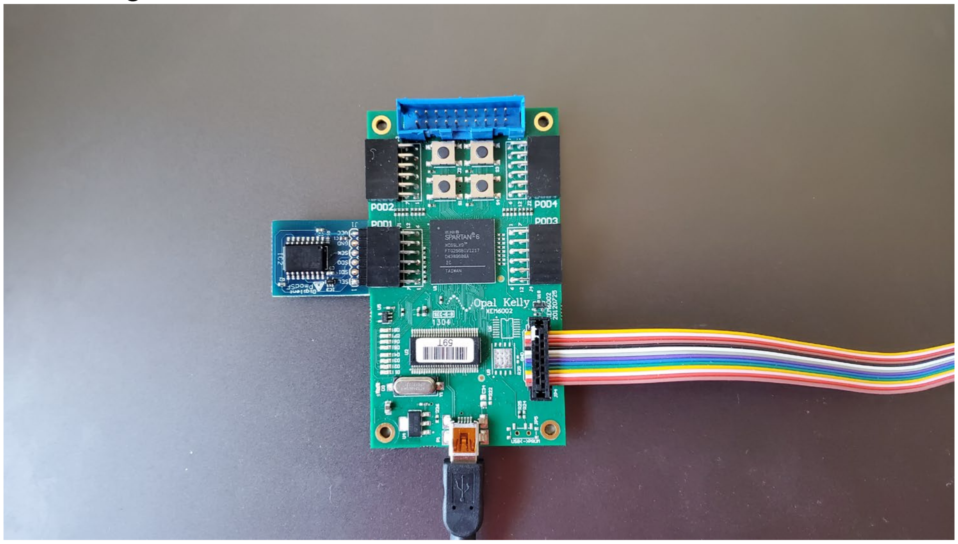
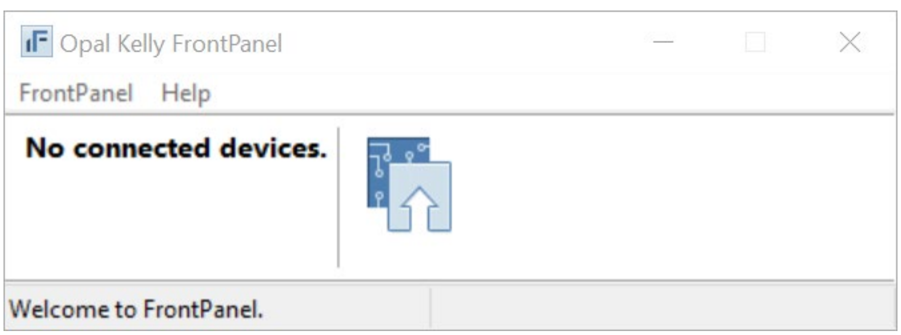


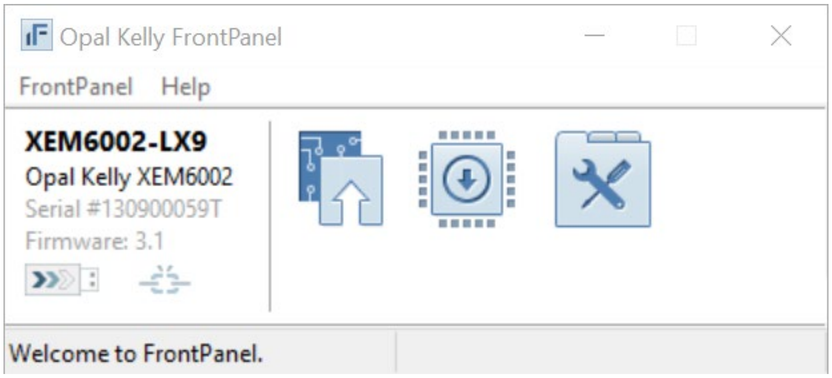
Figure 1 Opal Kelly XEM6002

The Opal Kelly XEM6002 has a FrontPanel software that needs to be installed. This interface is used to control the frequency of the FPGA and will be describe later in the manual. This software can be found at https://pins.opalkelly.com/ however, this will require the user to create a login to download the softare and proof of purchase of the hardware.

After installing the FrontPanel software and connecting the ScanWorks controller (this example will use the RIC-1000). Start the Opal Kelly interface as shown below.



Plugin the USB cable to the Opal Kelly Board and to the host where the FrontPanel and ScanWorks resides. The FrontPanel will look similar to the interface shown below.



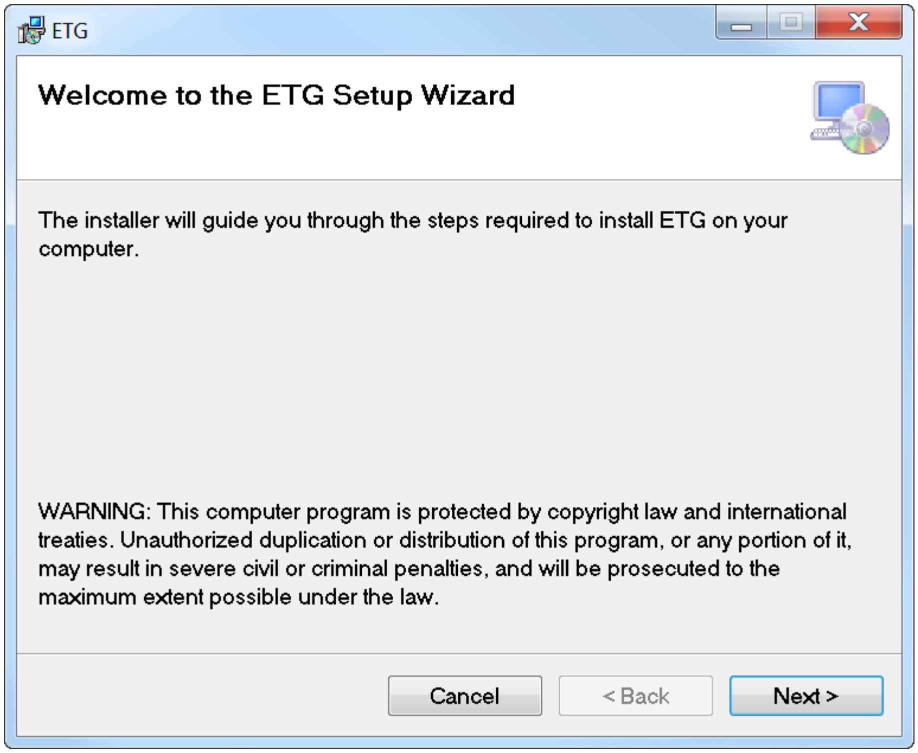
Later in the project we will configure the board with this FrontPanel application.

ScanWorks Software Installation

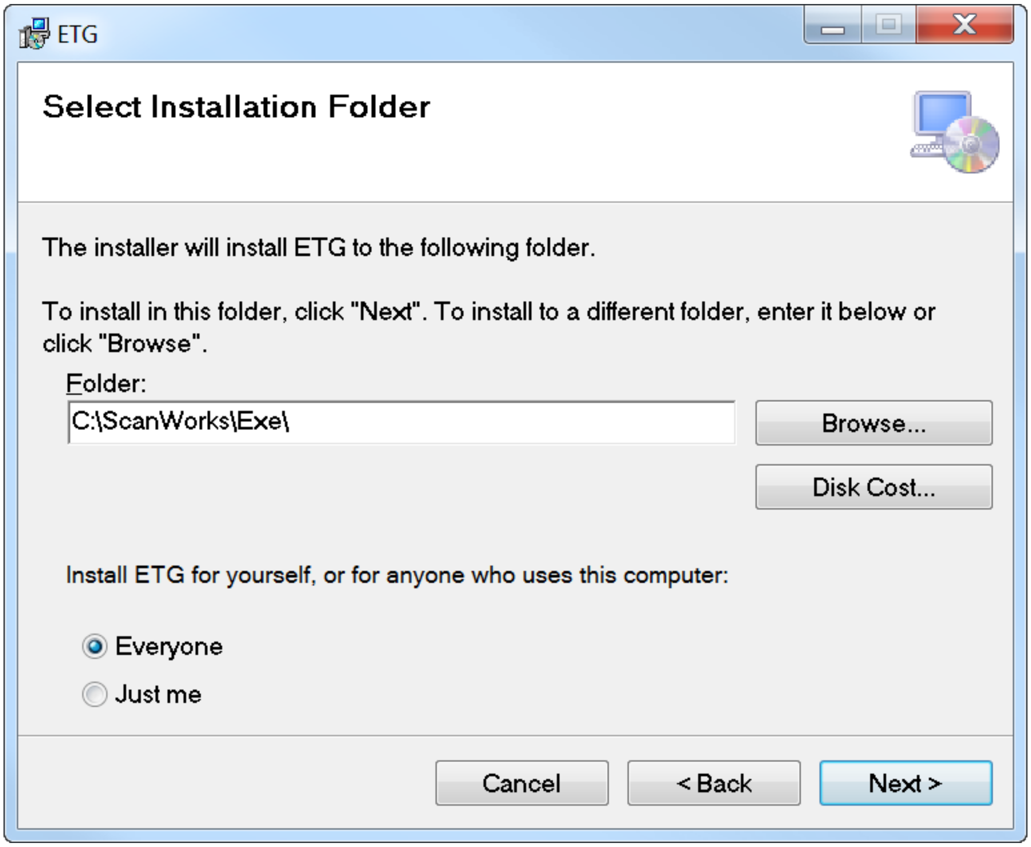
3. ETG Installer – Run

If you already have ScanWorks 4.8 installed, and are only installing ETG using the ETG Installer, continue below. If you are going to use the ASSET Web Deployment Installer to install ScanWorks and ETG, and perhaps other packages, proceed to ASSET Web Deployment Installer below.

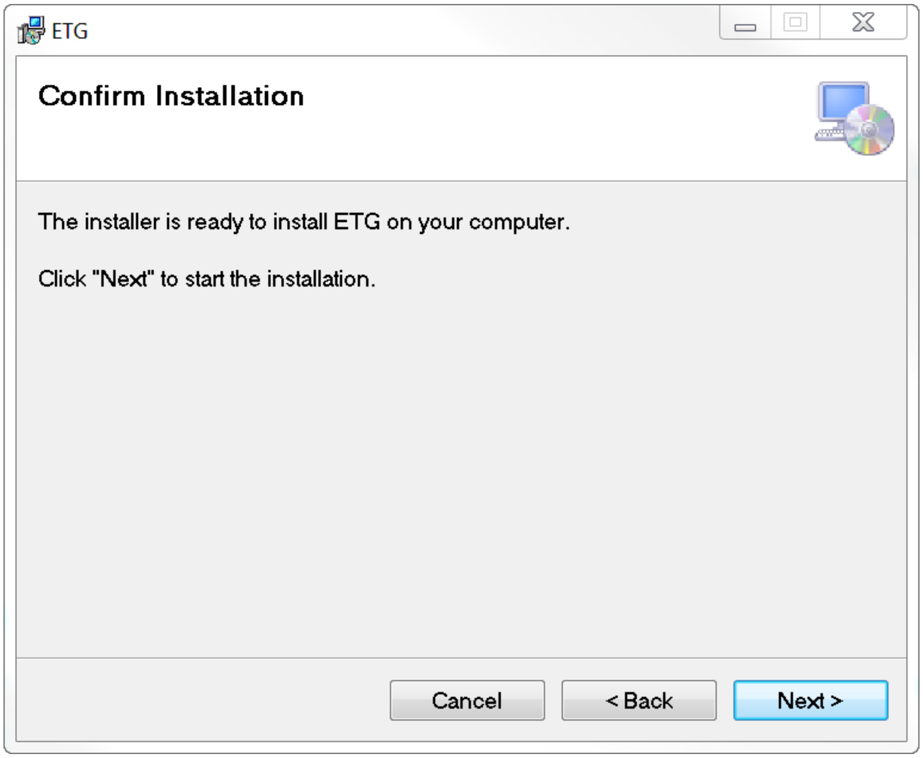
a. Double-click on the provided ScanWorks ETG_Setup.exe



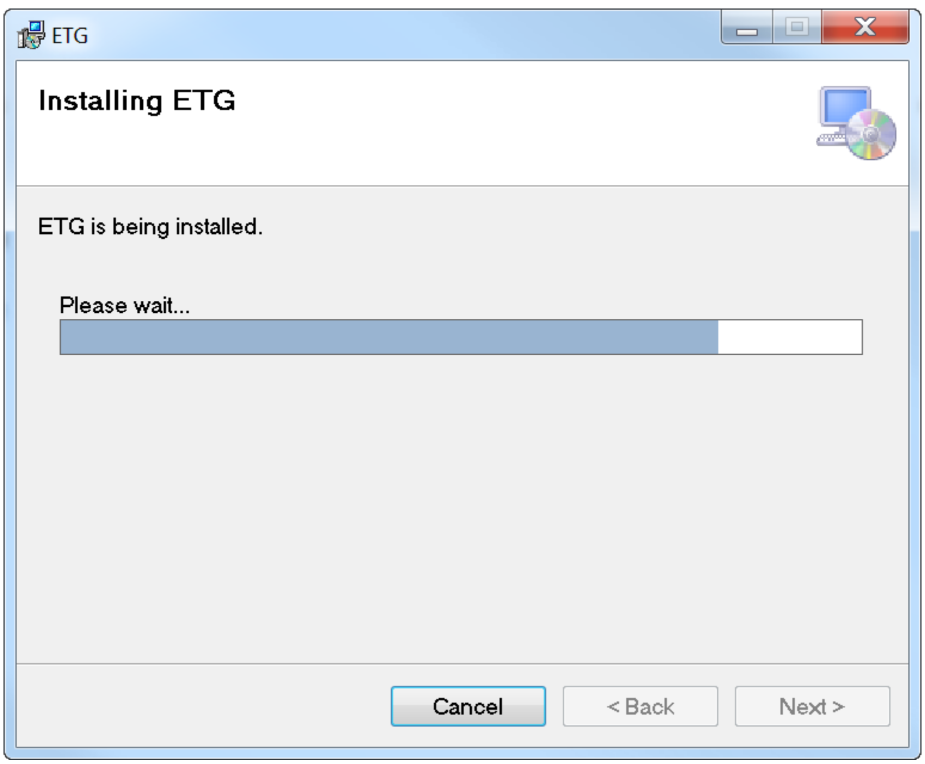
b. Select the Next button above.



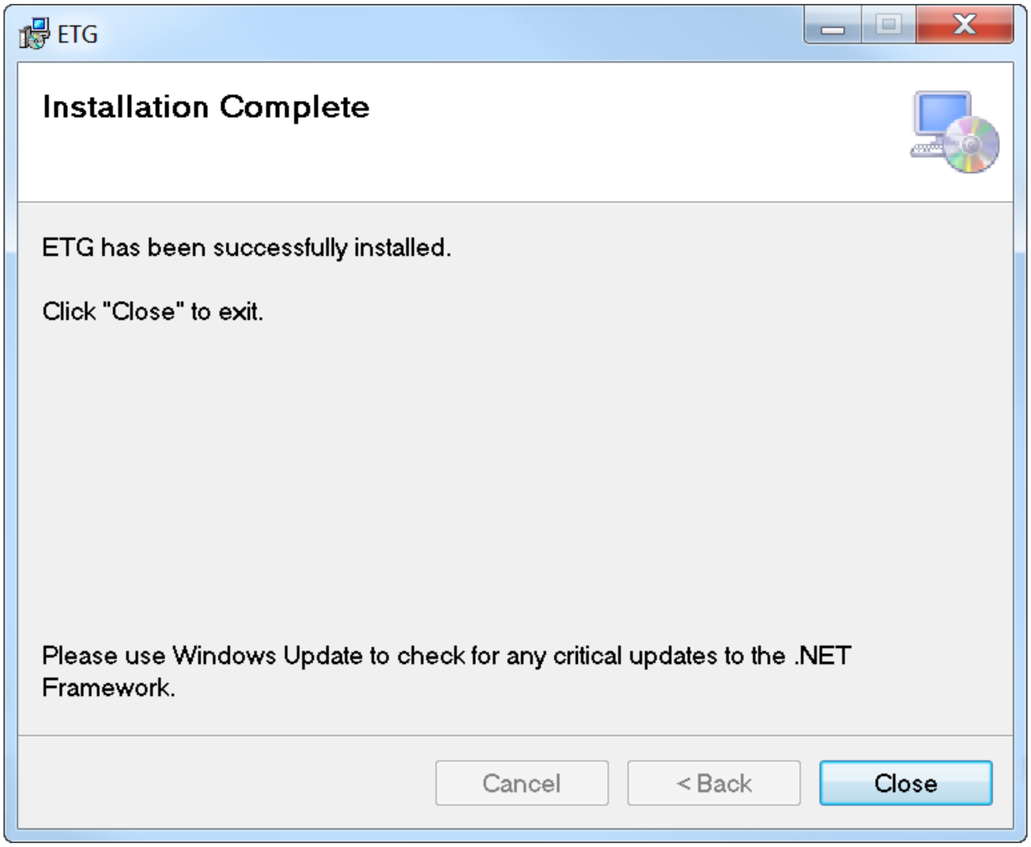
c. Next, browse to the ScanWorks\Exe folder and select Everyone or Just me. Or use the defaults if appropriate.
d. Select Next button as shown above.



e. Confirm the Installation by selecting Next button.



f. The installation will begin as shown above.



g. When the install completes as shown above, select the Close button.
h. Proceed to step 6 below.

4. ASSET Web Deployment Installer – Build and download

For this procedure use the link that was provided by ASSET order Fulfillment to build and download a custom installer program. Save this link as it is an active link and may be needed in the future for updating to never software revisions.

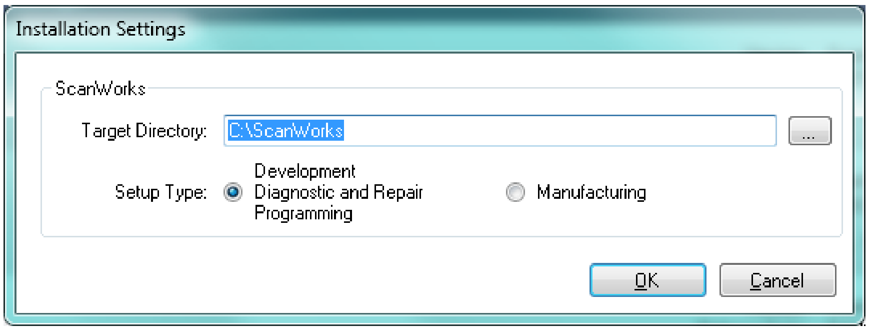
Click on the link provided by ASSET or paste it into your browser. The online instructions mention the methods for obtaining your ScanWorks license. Follow the online instructions to build and download the custom installer. The name of the custom installer reflects the versions of ScanWorks and ETG.

Example:
ASSET_WDI_ScanWorks.4.9.0.0-CreoView.10.2.20.23-CreoViewEA.10.2.20.23-ScanWorks_Platform.2.5.0.0-ETG.3.2.0.0.exe

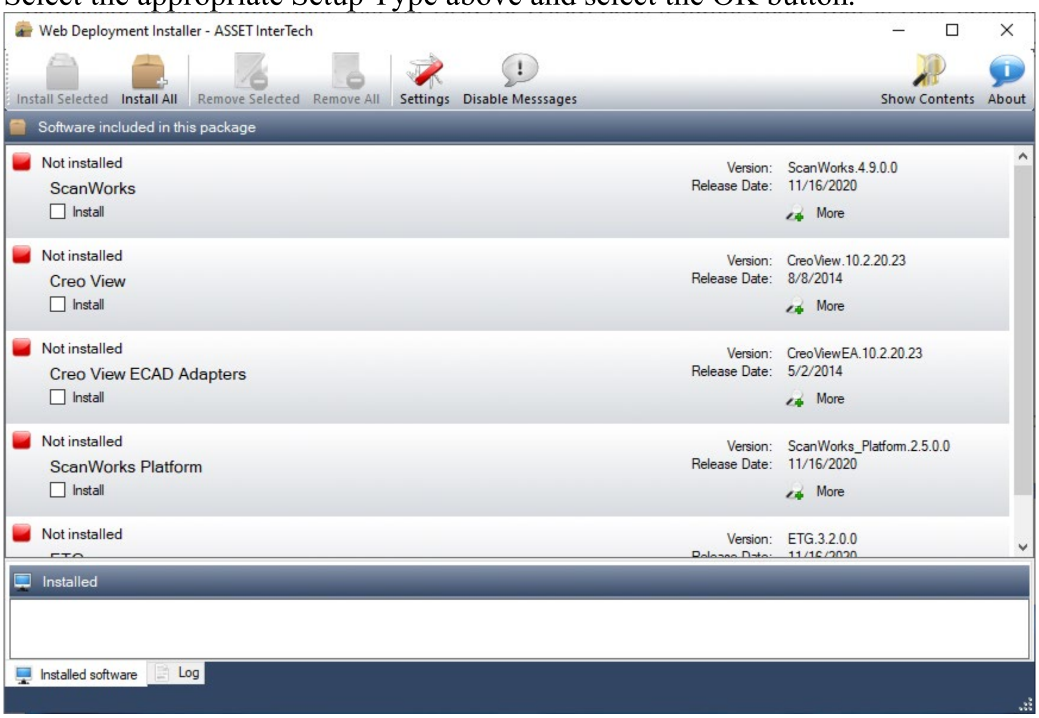
5. ASSET Web Deployment Installer – Run

Note: the following is an example of the steps necessary to use the WDI installer. Your exact experience will vary slightly from this example.

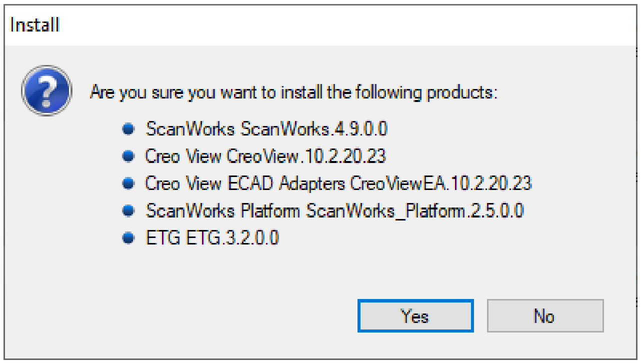
a. Run the installer as administrator.
b. Accept the license agreement.



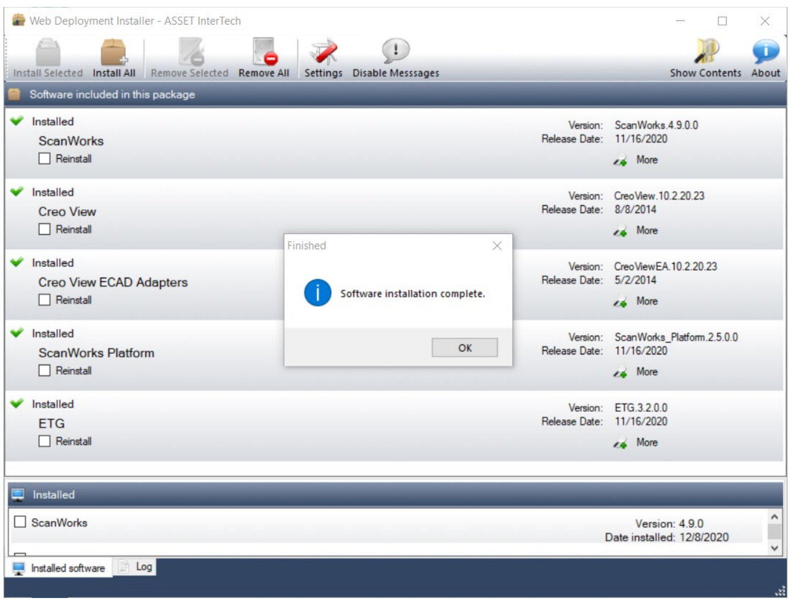
c. Select the appropriate Setup Type above and select the OK button.



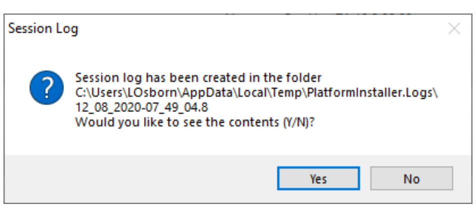
d. Select the Install All button above. (If you already have some packages installed, you can select only the ones needed and select 'Install Selected')



e. Select the Yes button above to accept the selections and start the install.



f. Select OK above when the installation completes.
g. Close the Web Deployment Installer window above.



h. Answer as desired above.

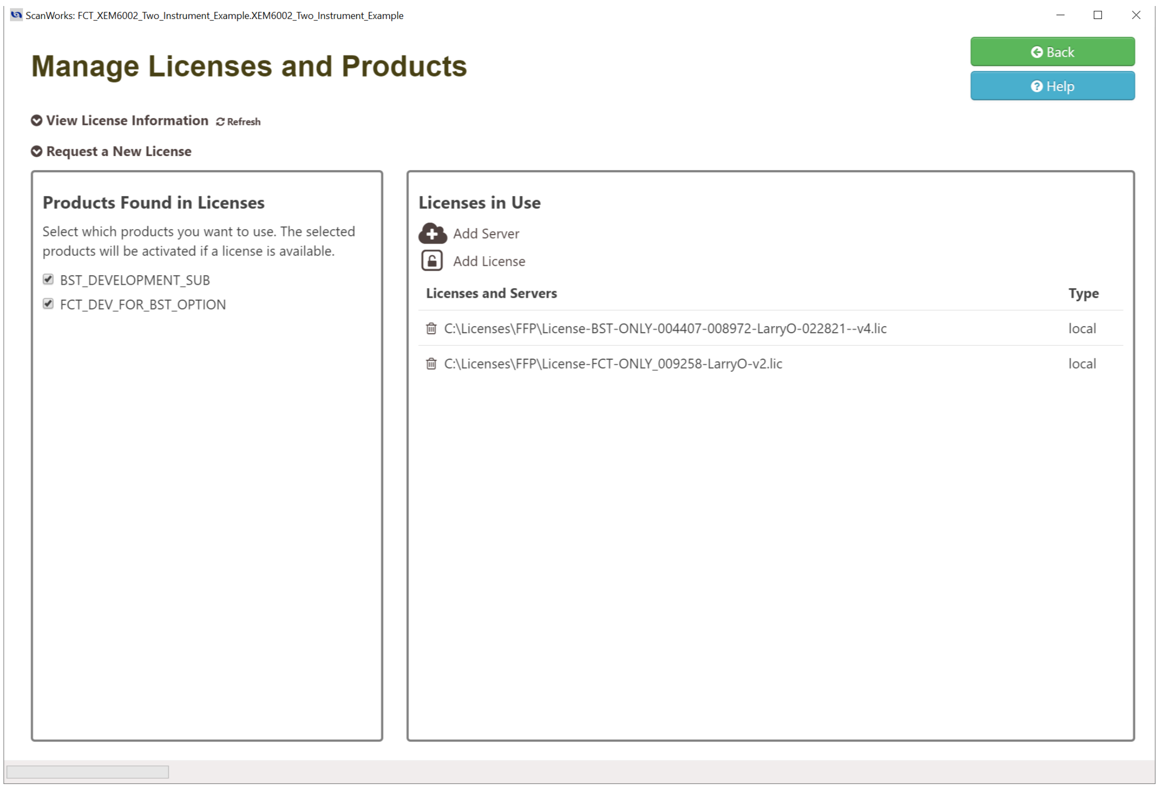
A ScanWorks ICON will be on the desktop when the installation is complete. Restart the computer.

Licensing

6. Request, Receive and Install Boundary Scan/ FFP/FFP Licenses

a. Refer to the email that you received for the order, or the document named C:\ScanWorks\doc\GettingStarted.pdf, to request, receive and install the Boundary Scan/FFP licenses.

b. After the licenses have been installed, open ScanWorks, using the License Manager window, select the boundary scan and FFP licenses that you intend to use. Note that all licenses checked will be immediately consumed when you open ScanWorks.



c. Close ScanWorks or select Back and ScanWorks will close.

Using FPGA Module

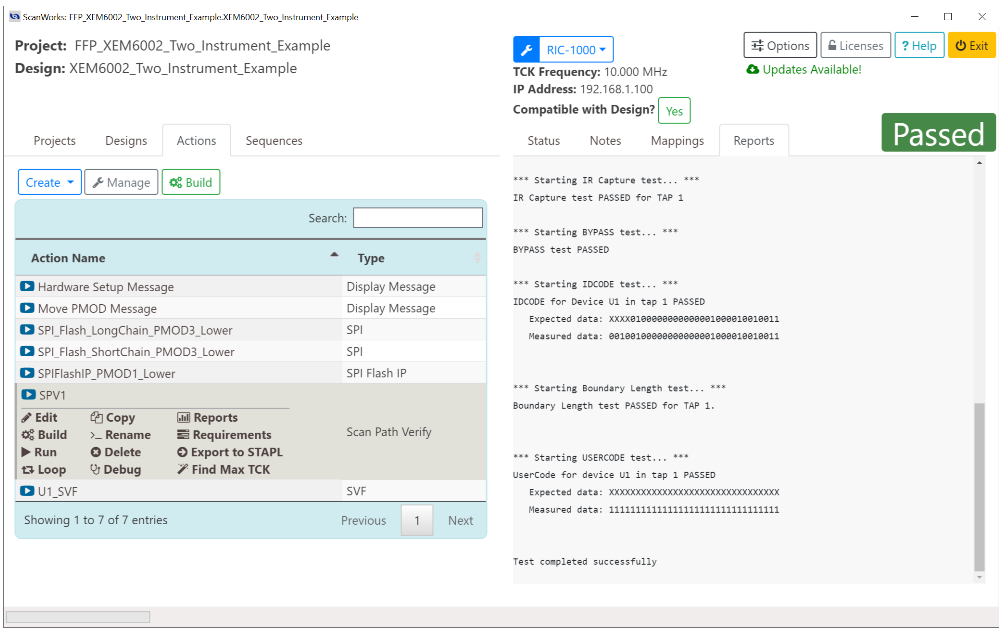
1. Getting Started with FPGA Module

a. Start by creating a new ScanWorks project and create the Design

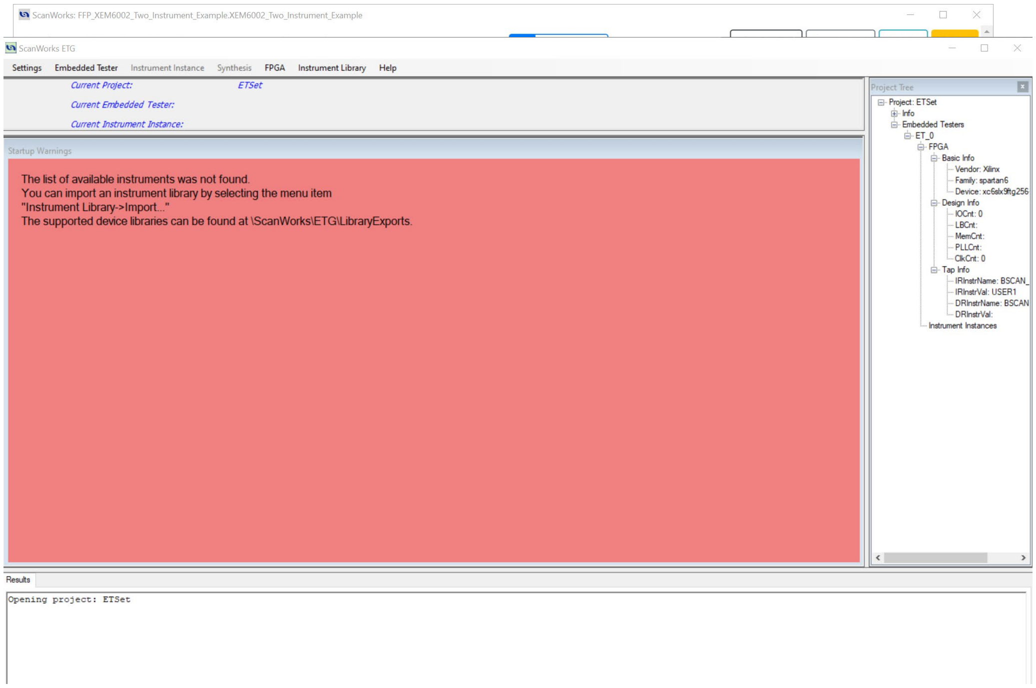
Note: This document will not provide the instructions for creating a project or design. We assume that the user is experience with ScanWorks. Also, we assume that a FPGA is within the Design

b. Select the Action tab and create an SPV action

c. Select the SPV action an verify the action passes. An example is shown below

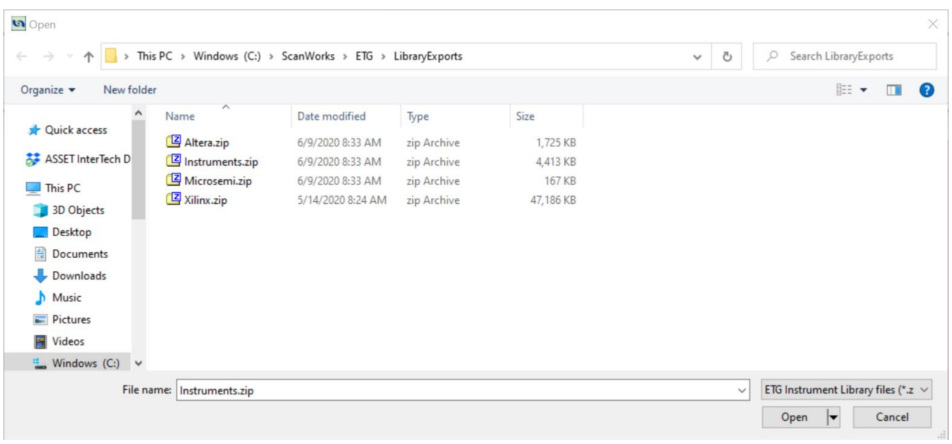


d. Select the Design tab and in the Design Resources and select FPGA Modules



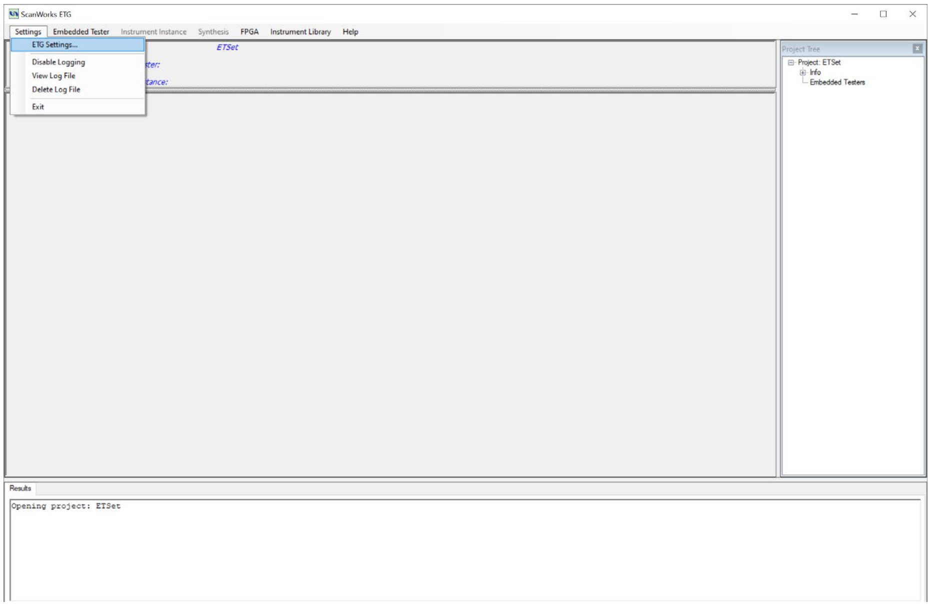
e. The ScanWorks ETG window will open

f. Follow the directions in the above screen. The browser will open as shown below.

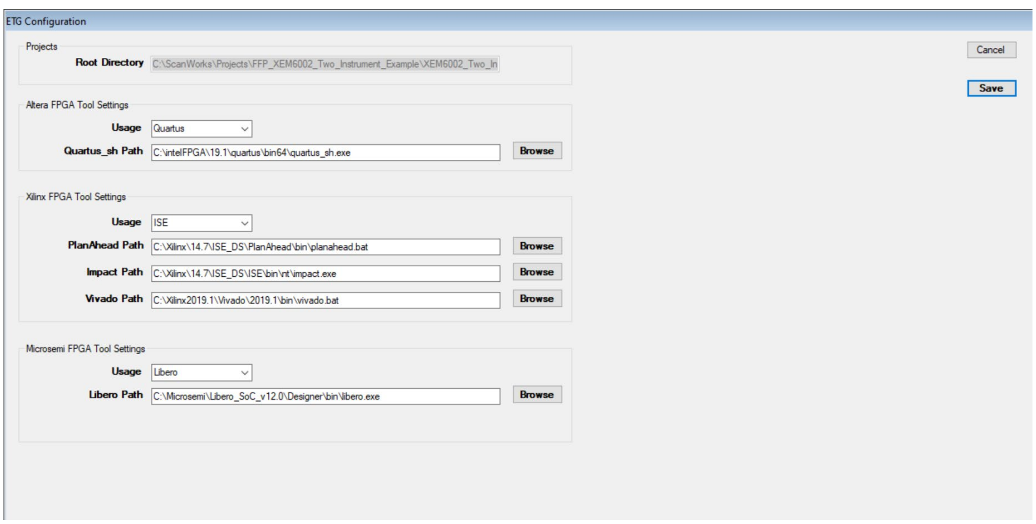


g. Select Instruments.zip Open

h. Select Settings -> ETG Settings



i. Now Configure the EDA tools locations as needed based upon the tool vendor. Shown below is an example with all three (Altera, Xilinx and Microsemi (a Microchip Company)) EDA tools are configured.

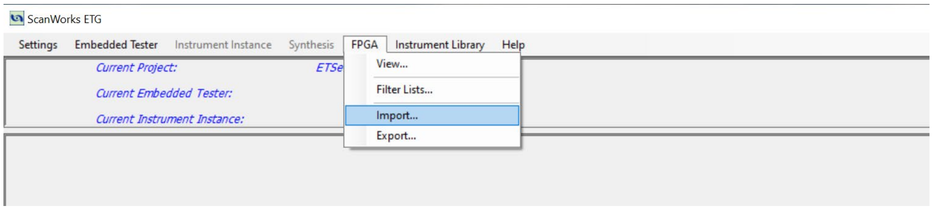


Select Save once you have configured the EDA tools you plan to use. For this example, we will be using Xilinx tools.

2. Importing the supported FPGA devices

a. The final step in preparing for the use of the FPGA Module is to import the FPGA devices support by the ScanWorks tool.

b. Select FPGA in the ScanWorks ETG window
c. Select Import



d. Browse to \ScanWorks\ETG\LibraryExports
e. Select the appropriate FPGA family zip file. For this project we are using Xilinx FPGA
f. Select yes if prompted to replacing local FPGA information for each FPGA imported.
g. The importing will complete. If you have other FPGA device families you wish to use, repeat the steps above to import the other devices.

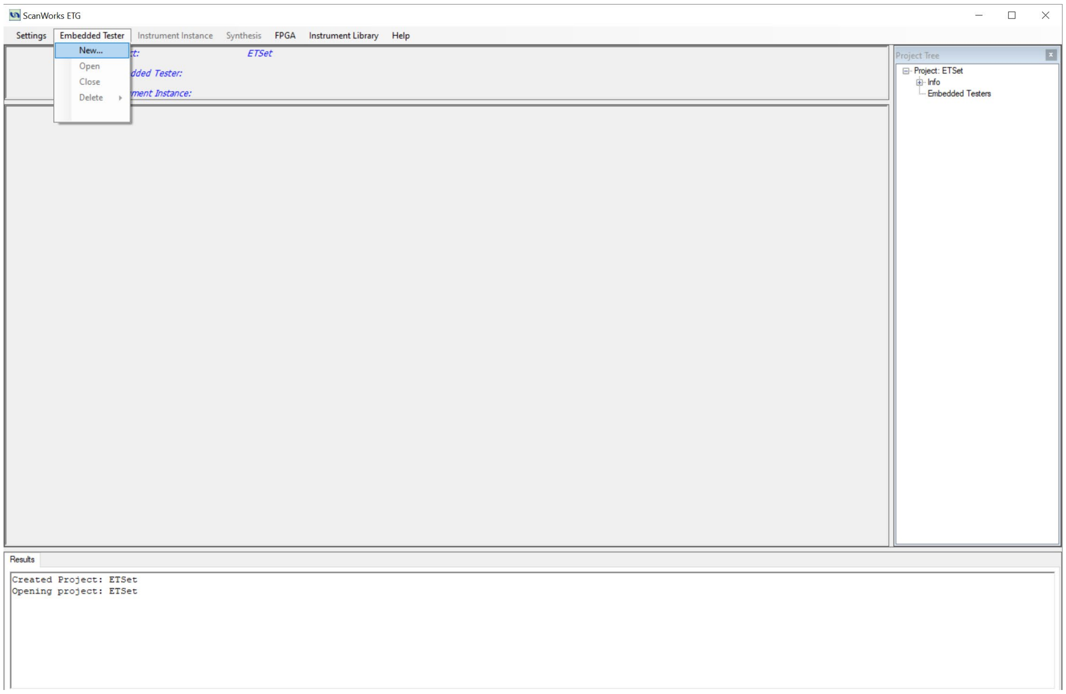
Embedded Tester Creation

3. Create an Embedded Tester

Embedded Testers are containers which hold instruments.
Embedded Testers can contain a single instrument or multiple instruments.
A ScanWorks design can currently only use a single embedded tester, so if you want to use multiple instruments you are better off putting them in a single embedded tester. That is assuming they will all fit into the FPGA being used.

The data input for these examples will be in a cyan color.

a) Select Embedded Test/New to create a new Tester.



b) Provide a name that is descriptive. Something with the instrument type and hardware could be used. FFP_Two_Instrument

c) Enter a user defined name for the project and select the OK button. **Naming Rules**: Must start with a letter and only use letters, numbers, dashes, and underscores.

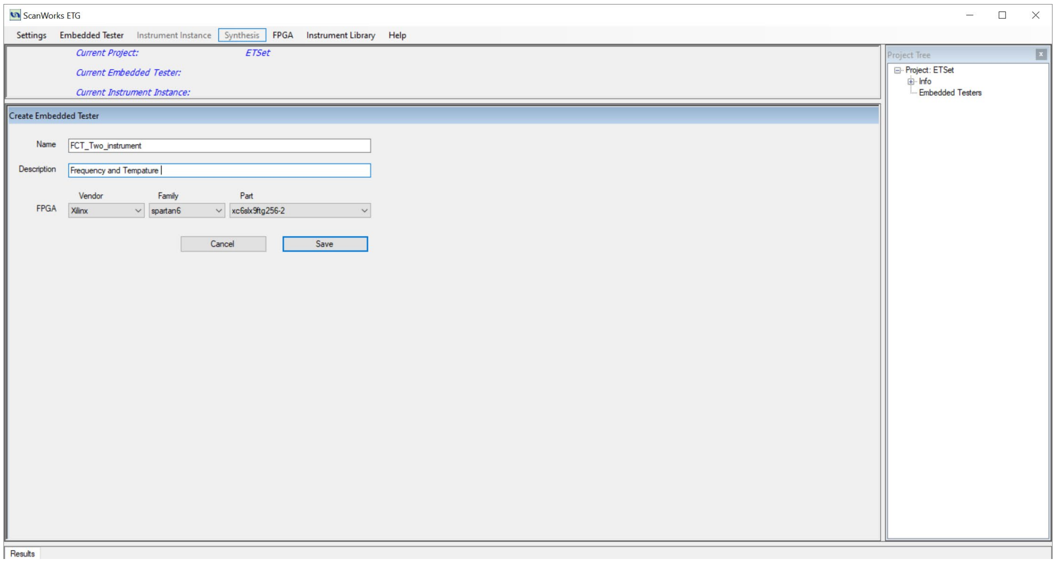
d) Enter a user defined description for the embedded tester.

e) Select the FPGA VENDOR Xilinx

f) Select the FPGA FAMILY Spartan6

g) Select the FPGA PART xc6slx9ftg256-2

h) Select the Save button.

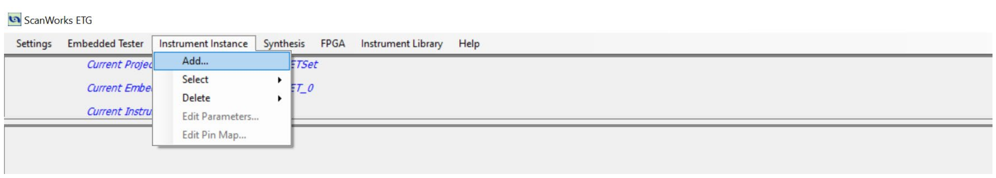


Note: the project tree that is being generated on the right side of the window.

4. Adding Instruments to the Embedded Tester

I. Add an instrument to create a Short Chain for programming the SPI Flash at PMOD3, lower position.

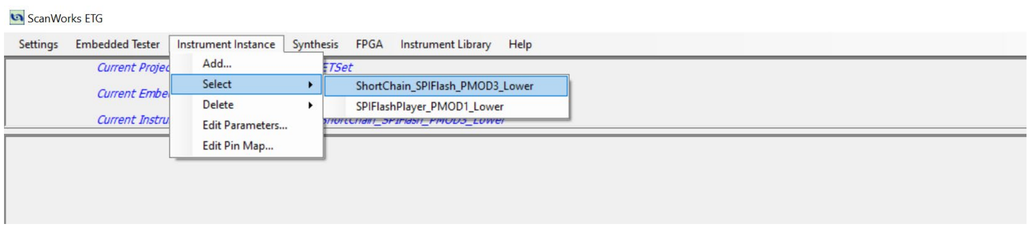
a. Select Instrument Instance ADD…



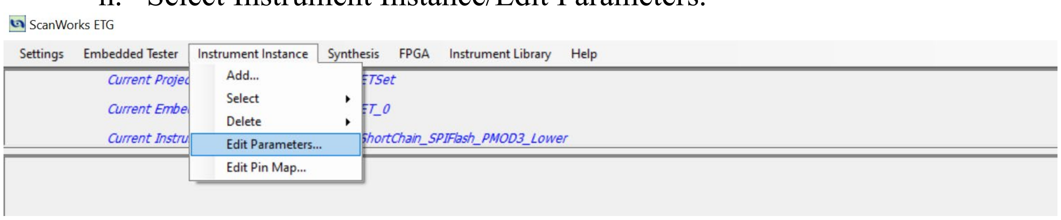
b. Enter a user defined name for the instrument.
ShortChain_SPIFlash_PMOD3_lower
c. Select the Instrument Type. GPIO
d. Select the Instrument Name. BST_IO
e. Select the Instrument Version. 1

f. Select the Save button below.

g. Select Instrument Instance/Select/ShortChain_SPIFlash_PMOD3_Lower.

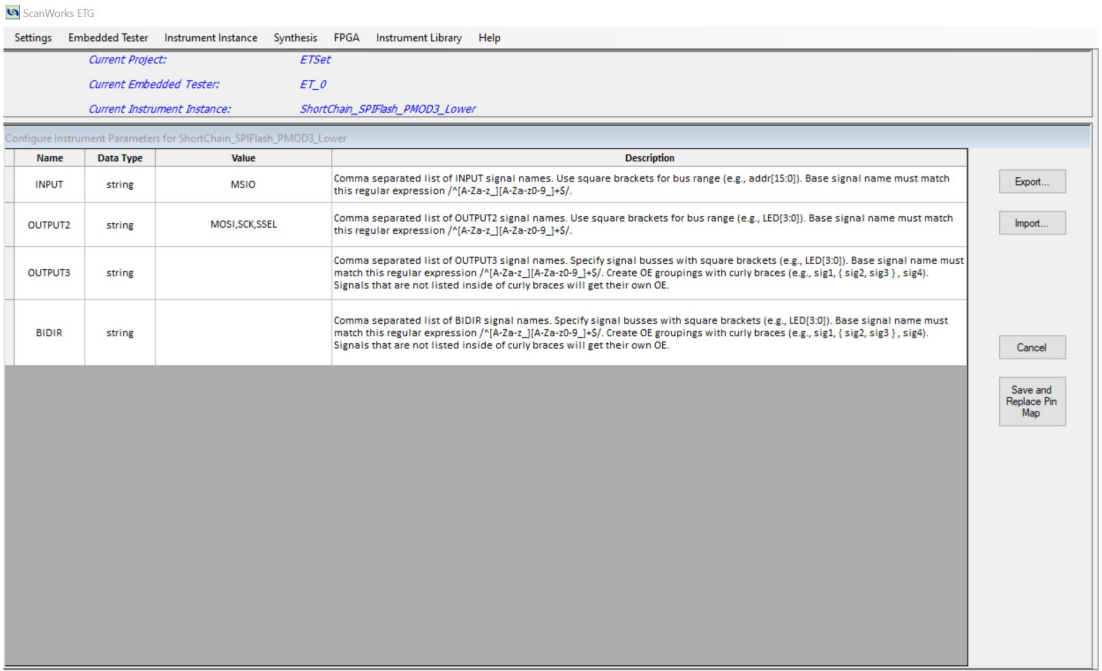


h. Select Instrument Instance/Edit Parameters.

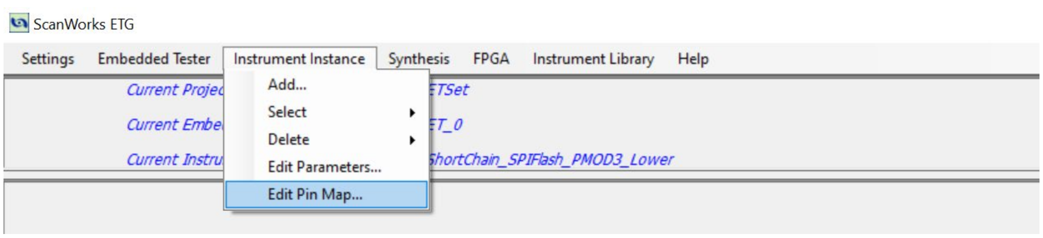


i. The parameters for this instrument are the ports/pins that you want in the short chain. Note that buses can also be declared in ScanWorks to control these pins. For this example, change them as shown below.

a. INPUT MSIO
b. OUTPUT MOSI, SCK, SSEL



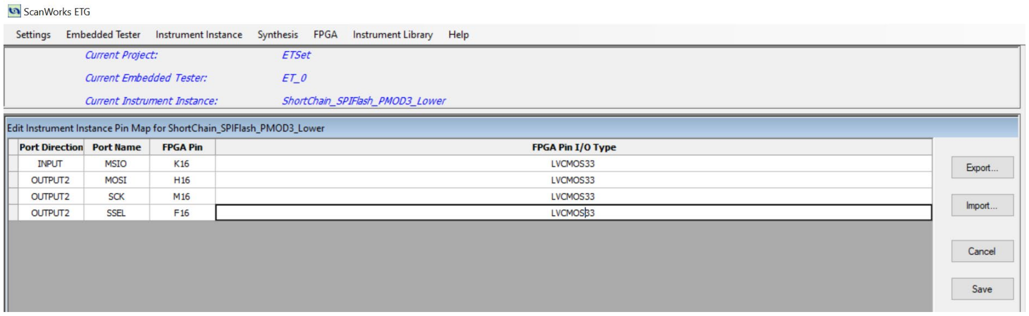
j. Select the 'Save and Replace Pin Map' button above.
k. Select Instrument Instance/Edit Pin Map.



l. Enter the 'FPGA Pins' as needed.
   a. MISO K16
   b. MOSI H16
   c. SCK M16
   d. SSEL F16

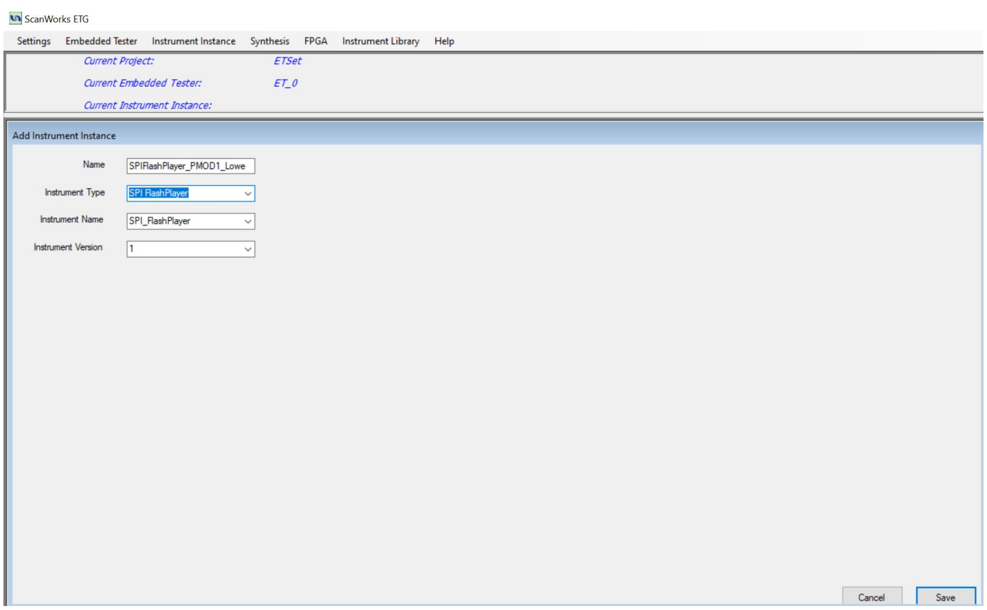
m. Enter the required I/O Type of the FPGA pins. LVCMO533

n. Select the Save button below.



II. Add **an SPI FlashPlayer instrument to program the SPI flash device at PMOD1, lower position.**

a. Select Instrument Instance/Add.
b. Enter a user defined name for the instrument.
SPIFlashPlayer_PMOD1_Lower
c. Select the Instrument Type. SPI FlashPlayer
d. Select the Instrument Name. SPI_FlashPlayer
e. Select the Instrument Version. 1
f. Select the Save button.

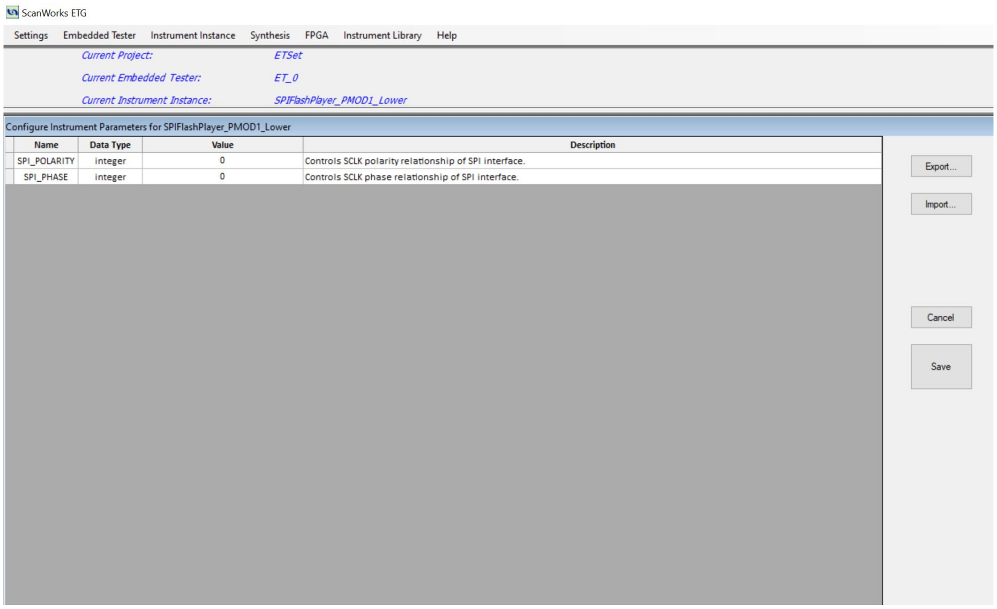


g. Select /Instrument Instance/Select/SPIFlashPlayer_PMOD1_Lower.
h. Select /Instrument Instance/Edit Parameters.

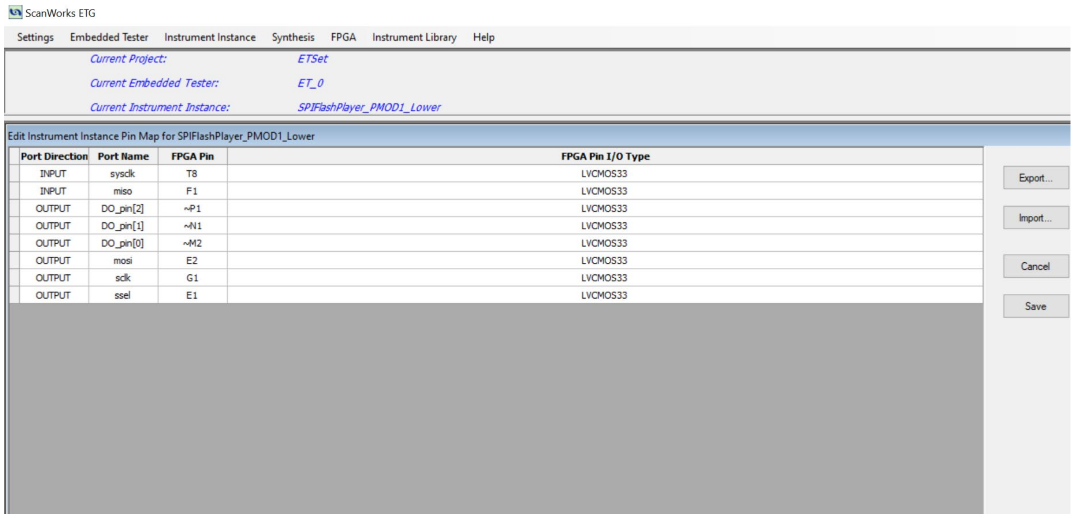
The parameters for this instrument are defined below and are adjustable.
SPI_POLARITY Controls SCLK polarity relationship of SPI interface (target device dependent)

SPI_PHASE Controls SCLK phase relationship of SPI interface (target device dependent)

i. Edit the parameters as needed, (leave as is for this example).
   a. SPI_POLARITY 0
   b. SPI_PHASE 0



j. Select the 'Save' button.
k. Select Instrument Instance/Edit Pin Map.
l. Enter the 'FPGA Pins' as needed.
   a. sysclk T8
   b. miso F1
   c. DO_pin[2] ~P1
   d. DO_pin[1] ~N1
   e. DO_pin[0] ~M2
   f. mosi E2
   g. sclk G1
   h. ssel E1
m. Enter the required I/O Type of the FPGA pins. LVCMOS33
n. Select the Save button.



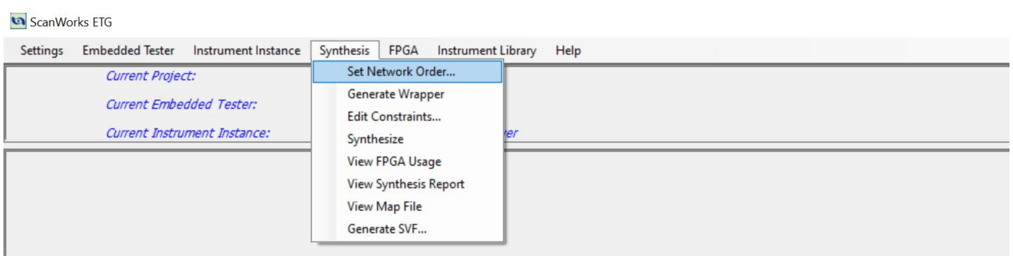
The three D0_pins declared above are static pins with a default state of 1 due to the ~. Since they are declared in this instrument, these pins can be set high or low within the ScanWorks SPI IP action, just as they could be in a standard SPI action. In the Opal Kelly design these pins are connected to D6, D7 and D8. Removing the ~ will illuminate these LEDs when the SVF is loaded into the FPGA.

In this case the two desired instruments have now been added to the new embedded tester.

5. Synthesis Steps for the Embedded Tester

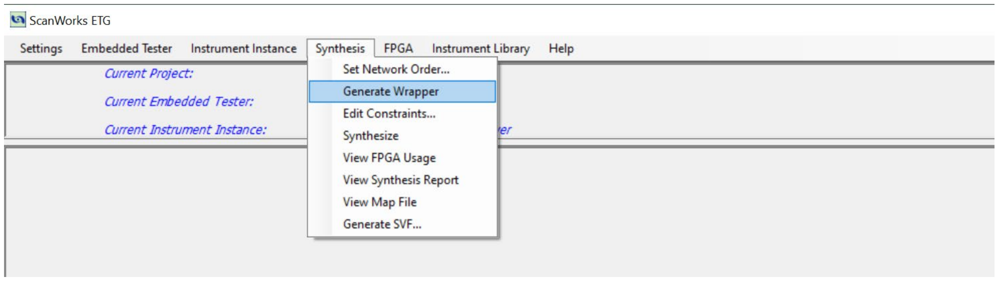
III. Establishing Network Order

a. Select /Synthesis/Set Network Order.



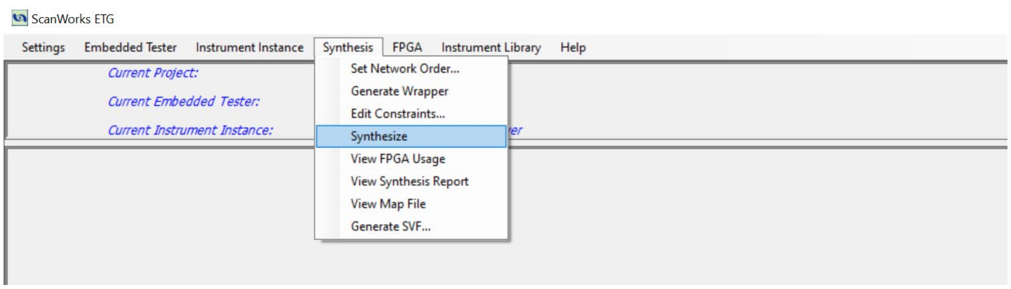
b. The order of the instruments can be changed, but leave as is for this example.
c. Select the Save button above.

d. Select /Synthesis/Generate Wrapper.

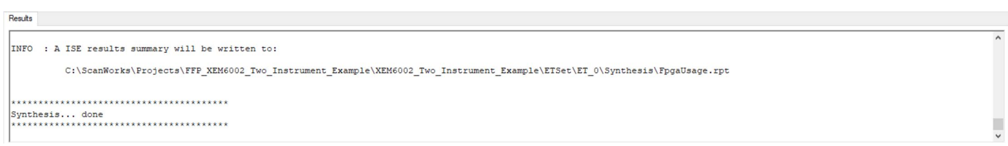


e. The Wrapper should generate as shown below.

f. Select /Synthesis/Synthesize.



g. The Synthesis should finish as shown below.

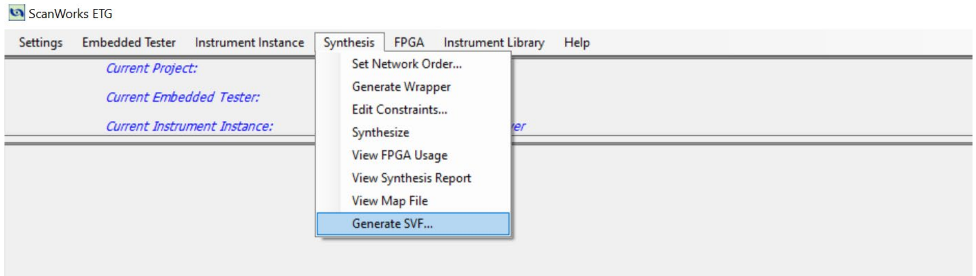


h. Select /Synthesis/View Synthesis Report.
i. Review the report for any warnings or errors.

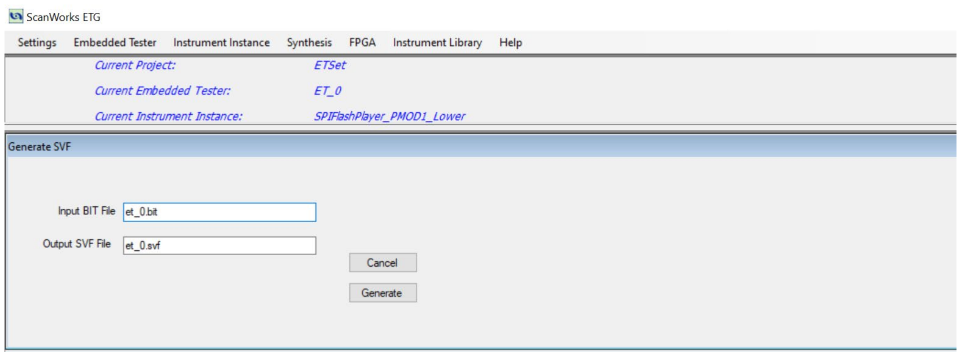
6. Create SVF File Step

I. Create an SVF file

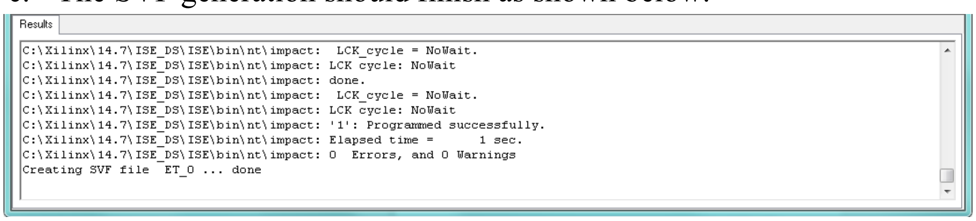
a. Select Synthesis/Generate SVF...



b. Select the Generate button below.



c. The SVF generation should finish as shown below.



d. Close the ScanWorks ETG window and return to the Design tab

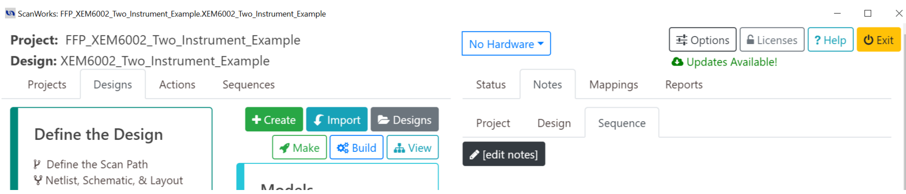
7. Recap of ETG Steps

Now that the FPGA synthesis is complete and the SVF file has been generated, you can find all of the files needed for building a ScanWorks actions with FFP actions in the ScanWorks directory, in the given ET directory for the ETG Project. For this example, they are found at:
C:\ScanWorks\Projects\FFP_XEM6002_Two_Instrument_Example\XEM6002_Two_Instrument_Example\ETSet\ET_0\ScanWorks

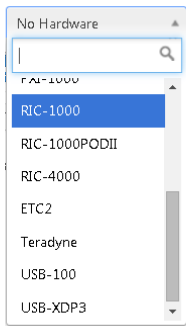
- Outputs of ETG
  - SVF – Serial Vector Format
  - BSDL – Boundary Scan Description Language
  - Pin Map

ScanWorks Setup

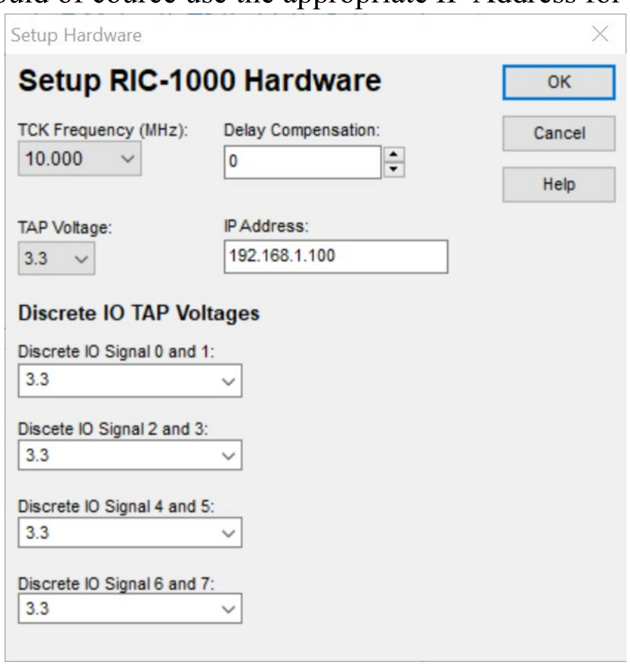
1. Select the ASSET Hardware



a. Select the ‘No Hardware’ link above.
b. Select the RIC-1000 from the drop-down menu.



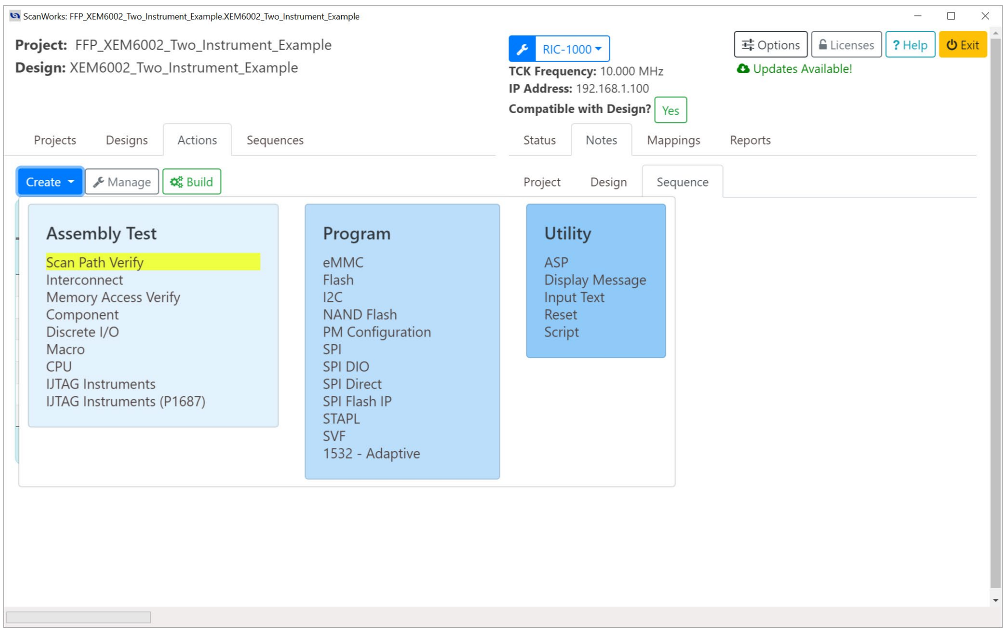
c. Configure the hardware. The RIC-1000 configuration is shown here, but other controllers can have different options. 10MHz is required for this example and you would of cource use the appropriate IP Address for your RIC-1000.



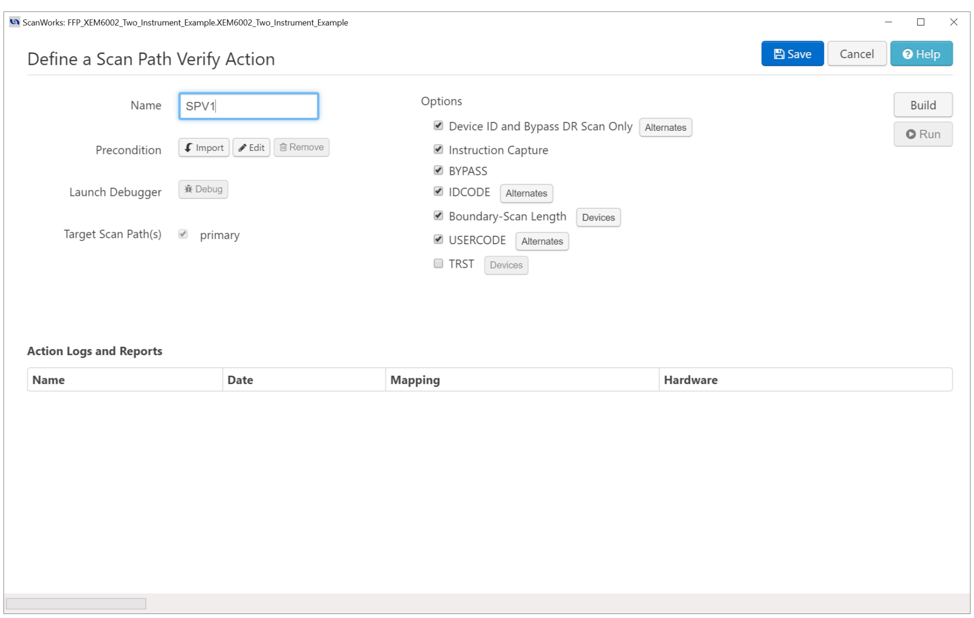
d. Select OK.

2. Create and run a Scan Path Verify (SPV) Action

a. Select the Actions tab.
b. Select the Create button.
c. Select the ‘Scan Path Verify’ link.



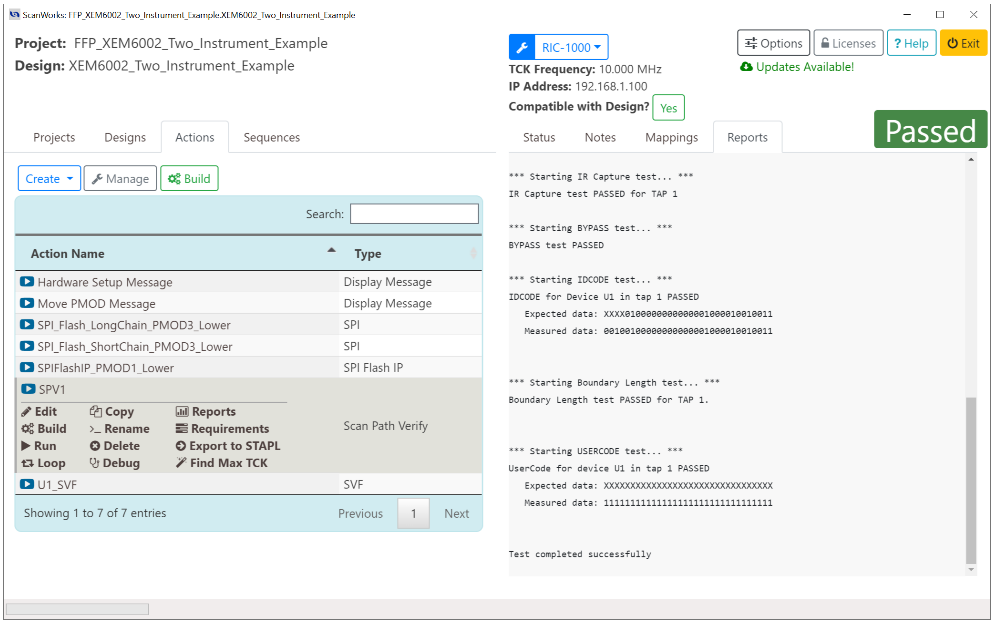
d. Below, accept the default or optionally you can rename the action.
e. Select the build button.



f. Select the Save button above.

3. Connect the ASSET hardware to the XEM6002 board.

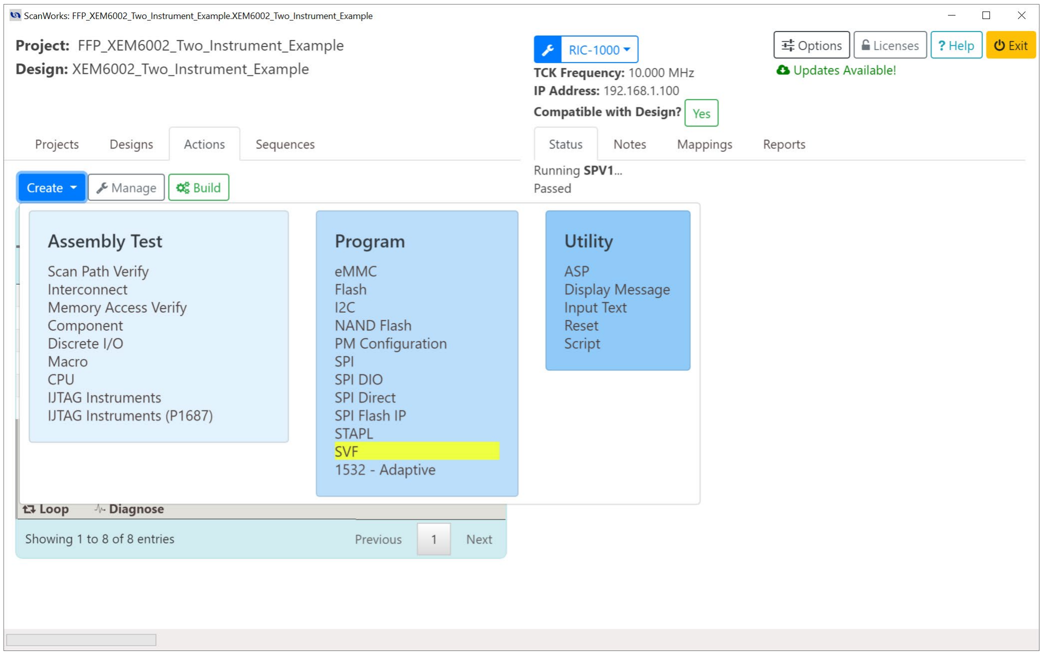
a. Power-up the XEM6002 by connecting the USB cable
b. Select the SPV1 Run button below.
c. Confirm the action passed as shown below.



4. Create and run an SVF Action - Configure the FPGA at U1 with the SPI Flash IP and GPIO instruments.

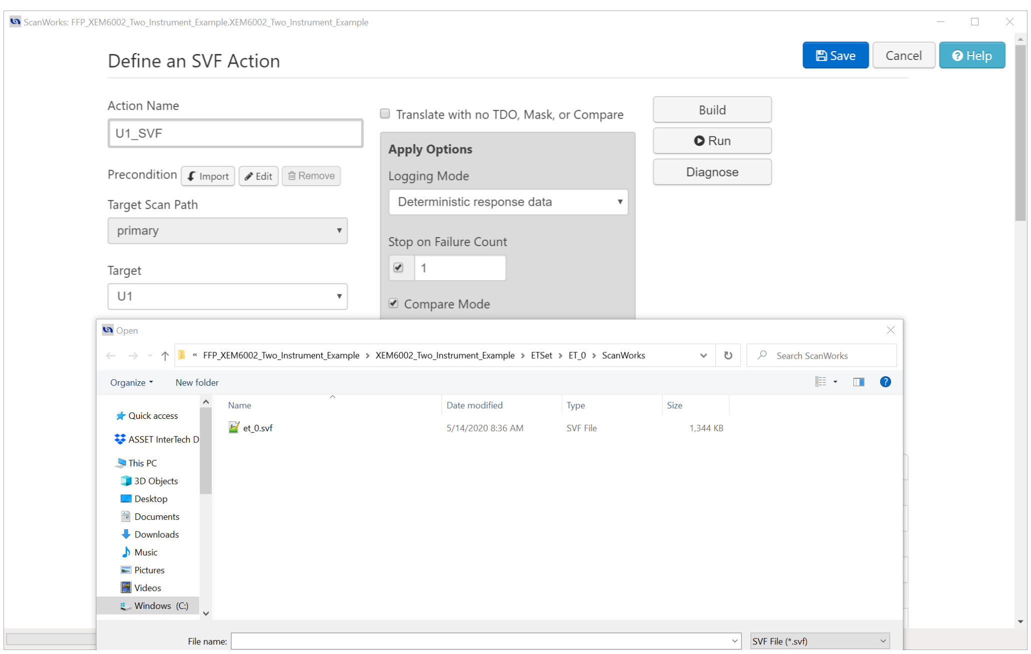
a. Select the Actions tab.
b. Select the Create button.

c. Select the SVF Link



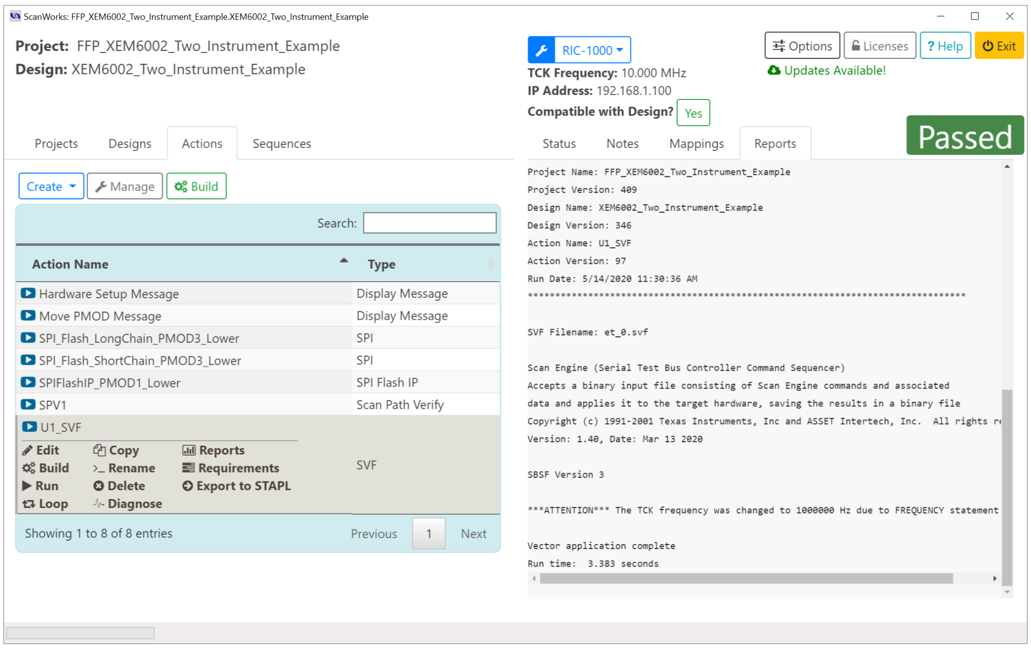
d. The Define an SVF Action will open.

e. Above you can optionally rename the action. U1_SVF
f. Set the Target drop-down to the device to be programmed. U1
g. Select the SVF import icon and browse to and select the .svf file in the appropriate ETG ScanWorks folder as shown below.



C:\ScanWorks\Projects\FFP_XEM6002_Two_Instrument_Example\XEM6002_Two_Instrument_Example\ETSet\ET_0\ScanWorks

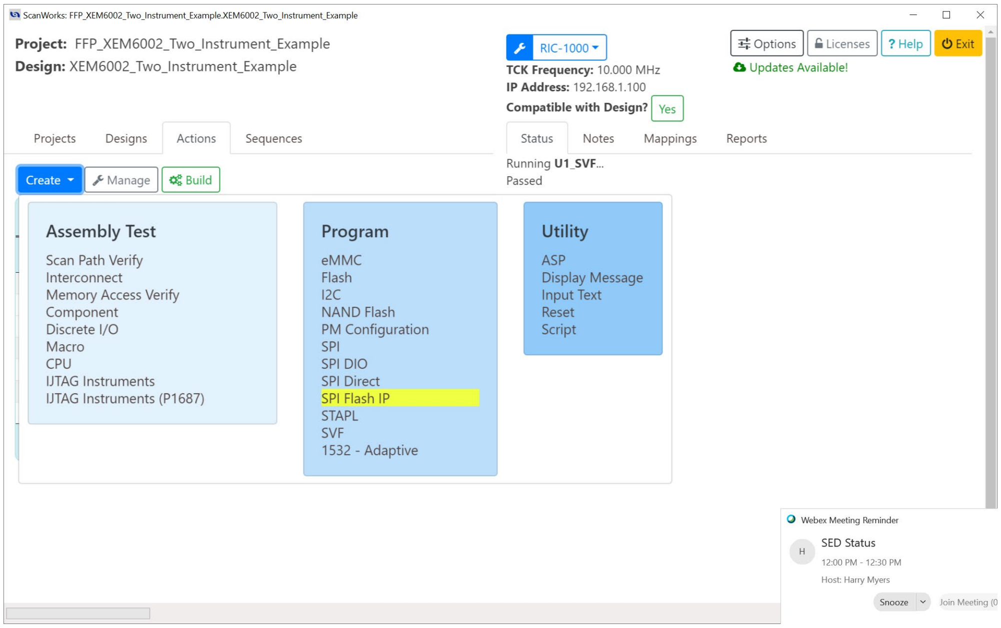
h. Select the Build button.
i. Select the Save button above.
j. Select the U1_SVF Run button below.
k. Confirm the action passed as shown below.



5. Create and run an SPI Flash IP Action - Program and Verify the SPI Flash device on PMOD1 lower position

a. Select the Actions tab.
b. Select the Create button.

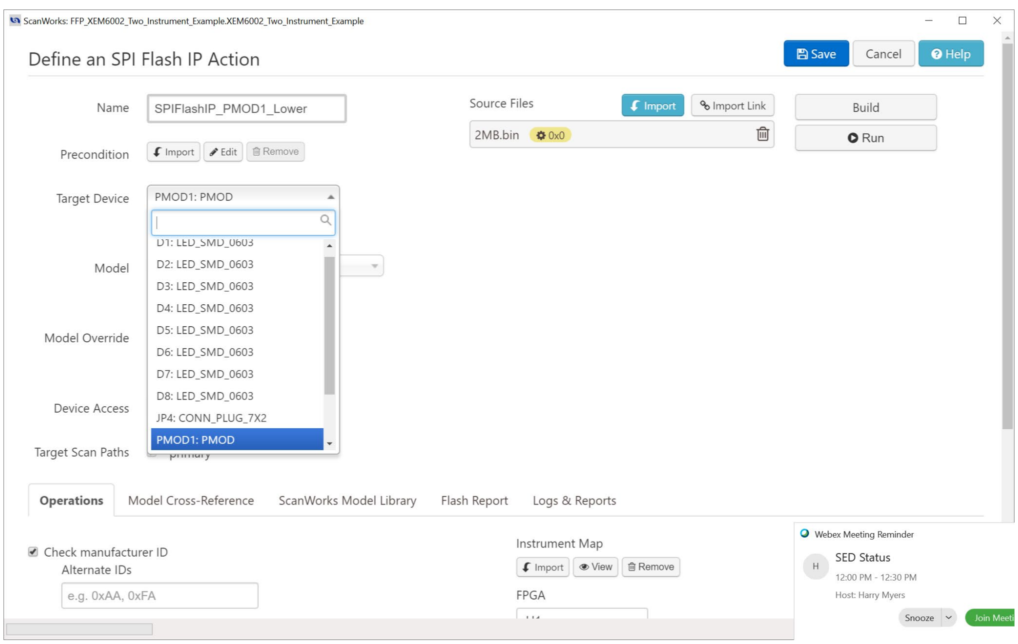
c. Select the ‘SPI Flash IP’ link.



d. Define an SPI Flash IP Action window opens

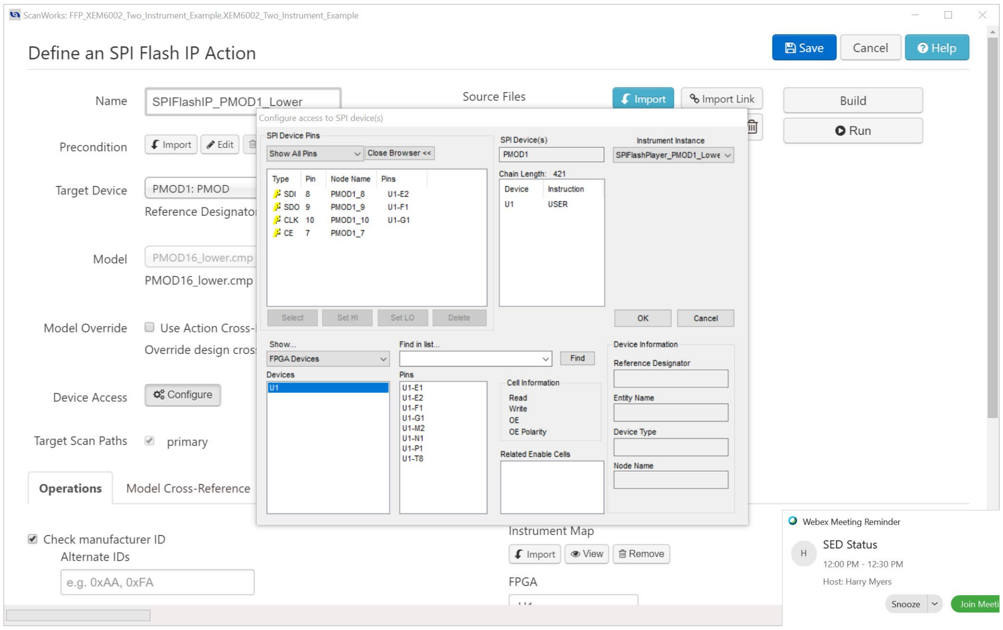
e. Provide a Name for the Action. SPIFlashIP_PMOD1_Lower

f. Select the target device to be programmed. (PMOD1)

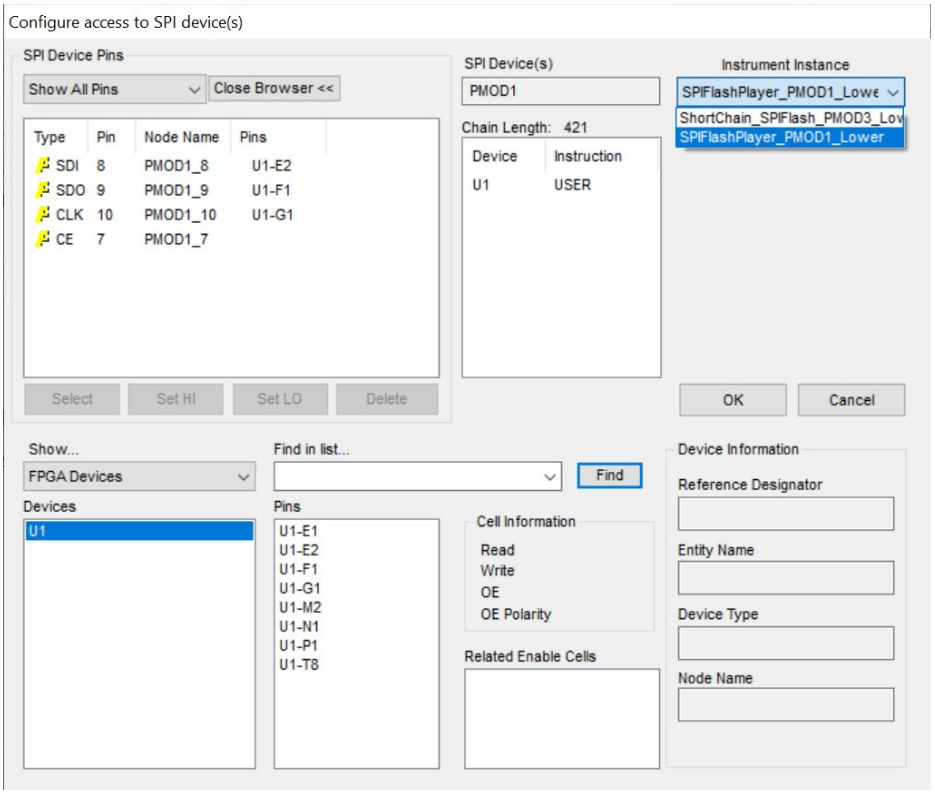


g. The Model should default to the PMOD16_lower.cmp.

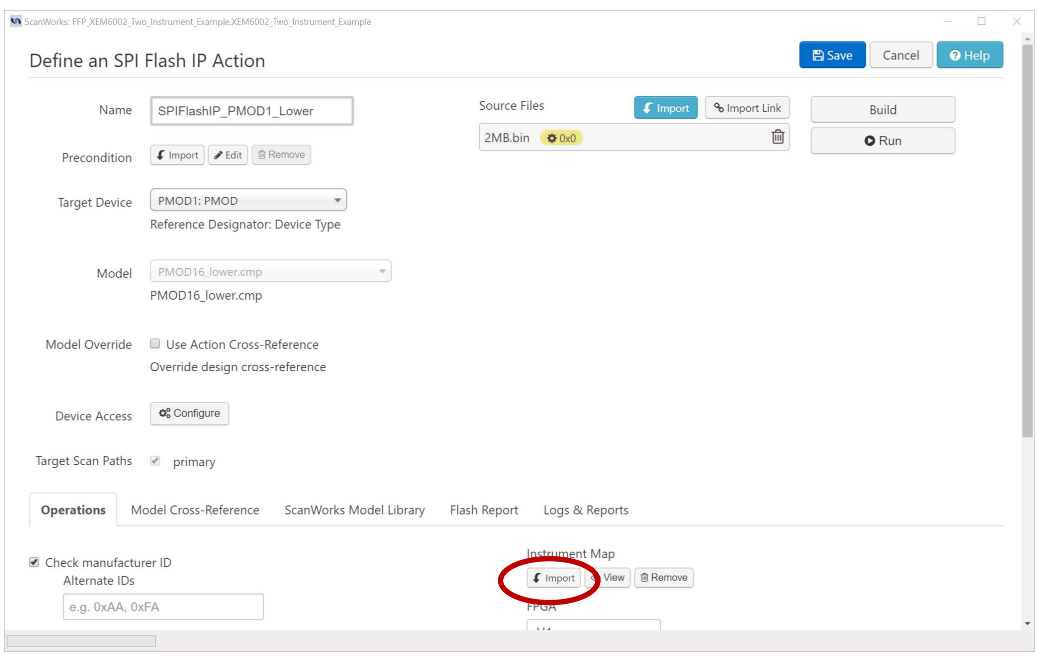
h. Select the Device Access Configure



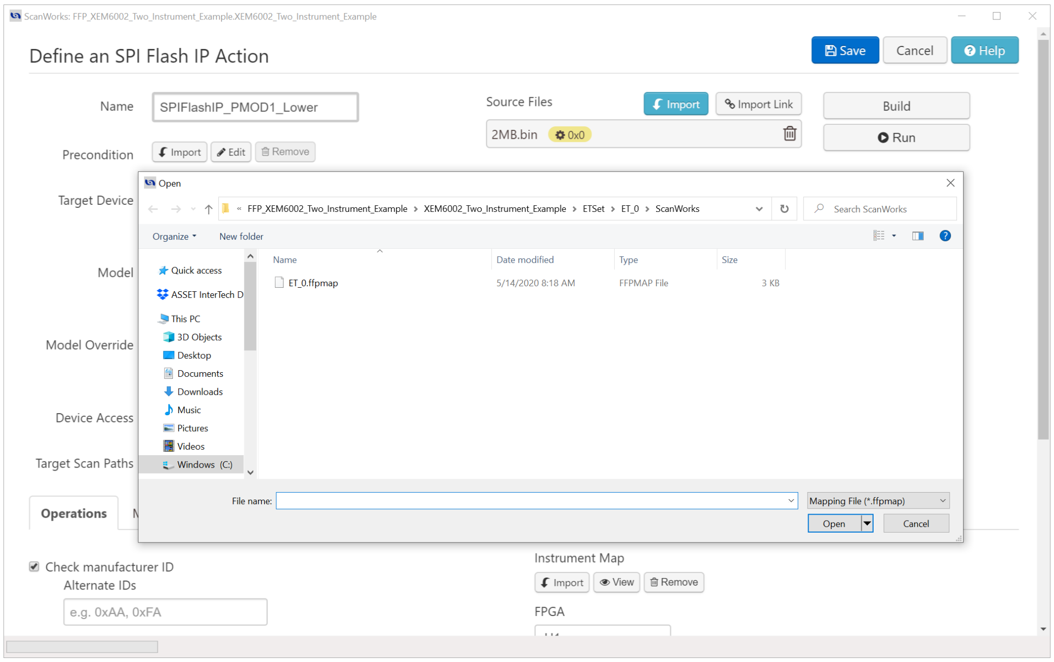
i. In the Configure access to SPI device(s) dialog select the Instrument Instance SPIFlashPlayer_PMOD1_Lower



j. Select the OK button. This will close the dialog.
k. In the Operations tab under Instrument Map select import



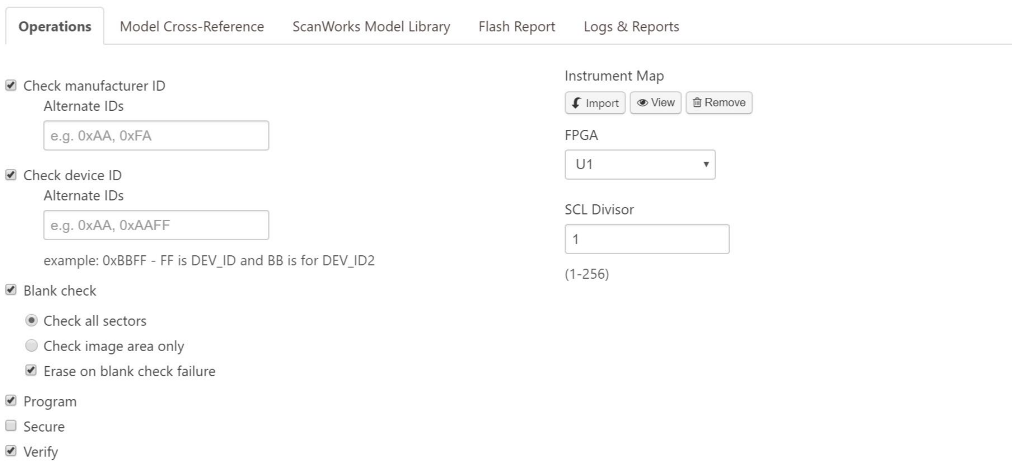
l. With the import browser open, browse to and double-click on the .ffpmap the instrument map. ET_0.ffpmap C:\ScanWorks\Projects\FFP_XEM6002_Two_Instrument_Example\XEM6002_Two_Instrument_Example\ETSet\ET_0\ScanWorks\ET_0.ffpmap in this case



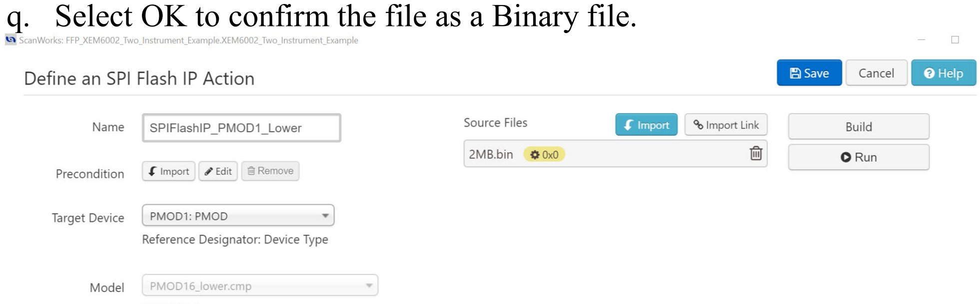
m. Select the Open button to acknowledge that the Import is complete.

n. Next in the Operations Tab
   a. Select the manufacture ID
   b. Select the deivce ID
   c. Select Blank check
      i. Check all sectors
      ii. Erase on blank check failure
   d. Select Program

e. Select Verify



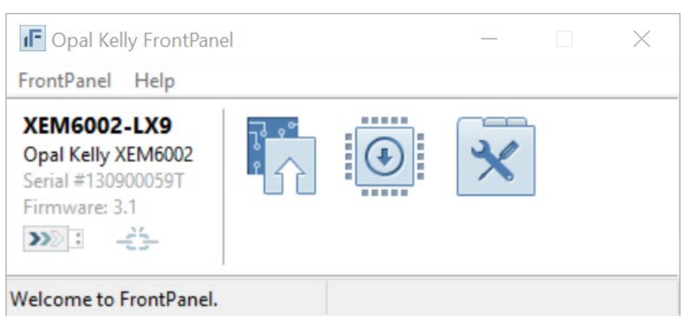
o. Select the blue Import icon next to "Source Files".
p. Browse to and double-click on the provided file named 2MB.bin.
q. Select OK to confirm the file as a Binary file.



r. Select the Build button.
s. Select Yes to confirm the action name change.
t. Select the Save button.

Opal Kelly FrontPanel Settings

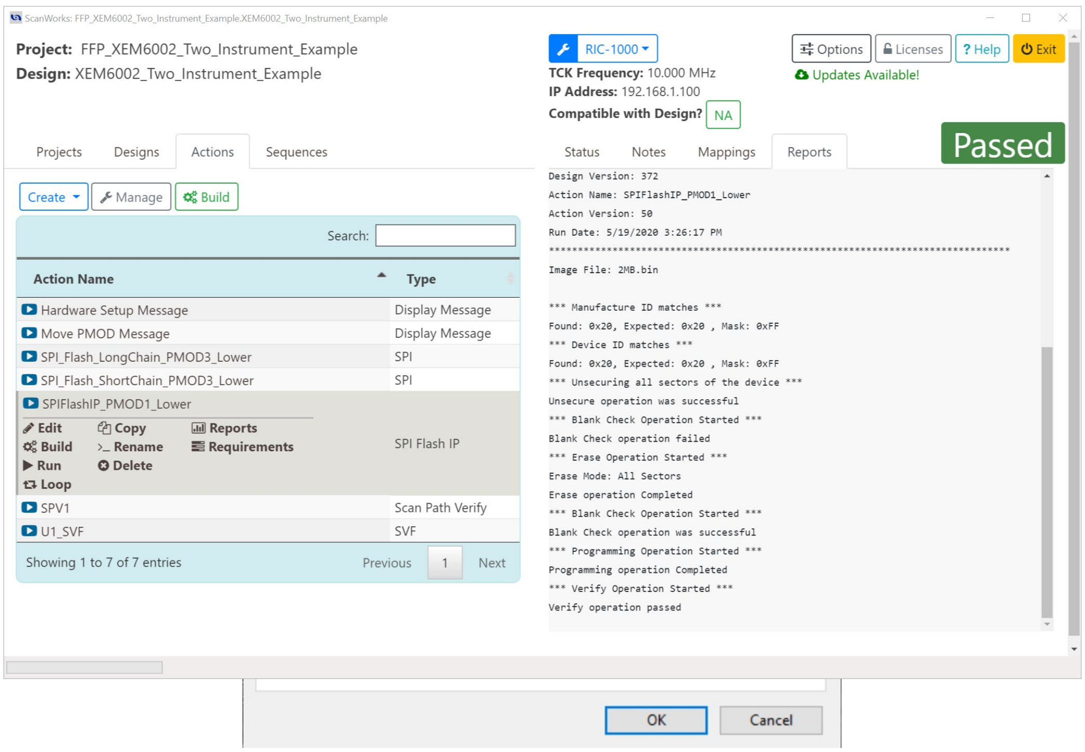
If you have closed the Opal Kelly FrontPanel, restart the application.



Select the tools icon and the following interface will open. Note that for this SPI Flash IP example, when using the Opal Kelly board, it needs to be set as follows, using the FrontPanel software, for the SPI Flash IP to Pass. Decrementing the Divider #1, DIV1N:, to less than 7, will increase the related frequency and cause a failure.

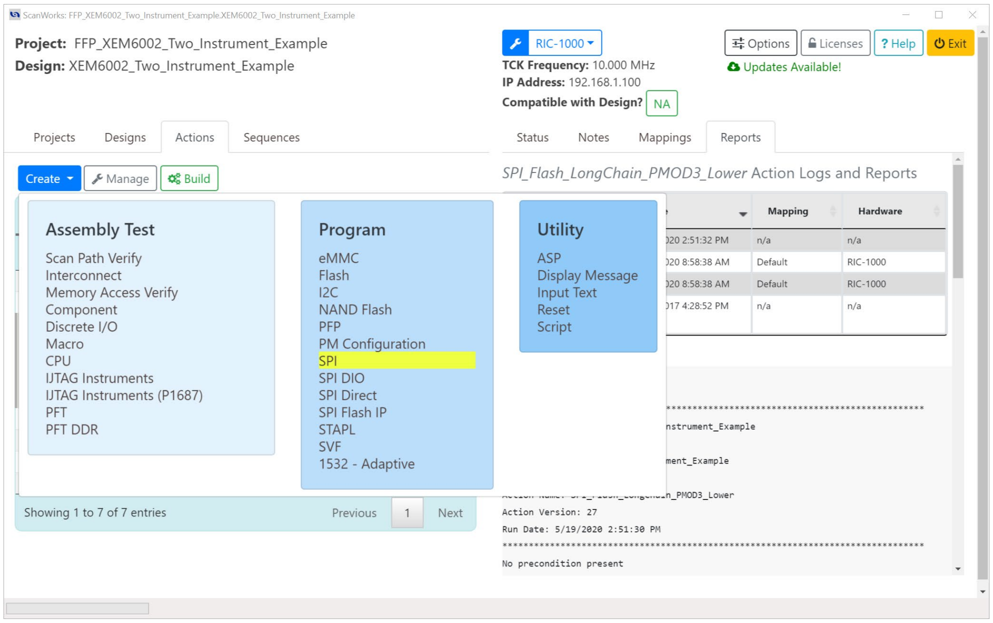
Return to ScanWorks

u. Select the SPIFlashIP_PMOD1_Lower Run button below.
v. Confirm the action passed as shown below.

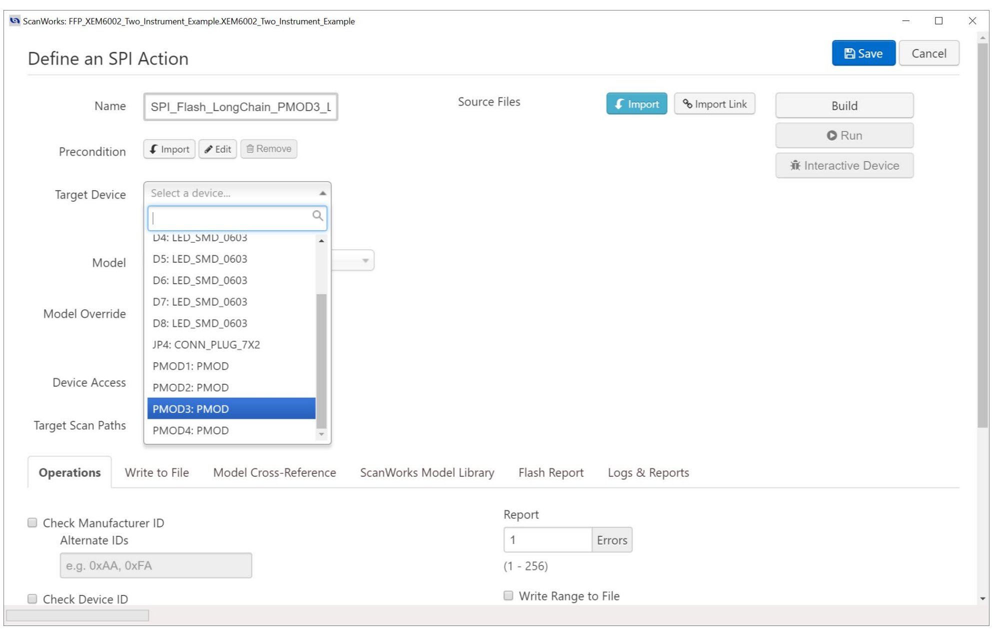


6. Create and run a standard Boundary Scan SPI Flash Action – Using the default boundary register and PMOD3 lower position

a. Power off the target
b. Physically move the SPI Flash PMOD from PMOD1 to PMOD3.
c. Select the Actions tab.
d. Select the Create button.
e. Select the 'SPI' link.

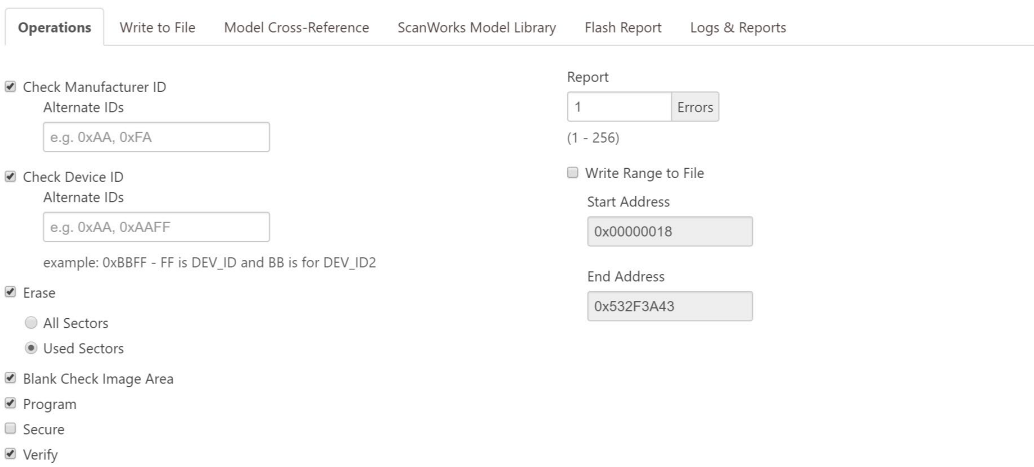


f. Enter Name SPI_Flash_LongChain_PMOD3_Lower
g. Select PMOD3 below as the device to program.
h. The Model should default to PMOD16_lower.cmp

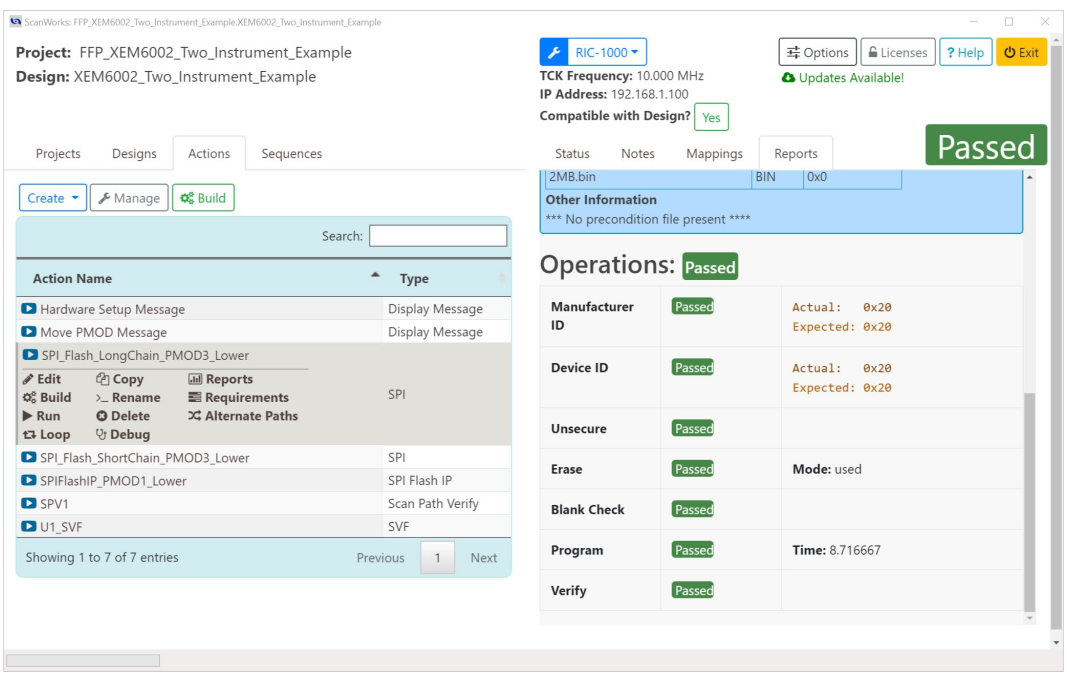


i. Device Access
   a. Select the Configure button.
   b. Ensure the Boundary Scan Master is U1
j. Select the OK button.

k. Select the two ID Checks, Erase, Blank check, Program, and Verify boxes.

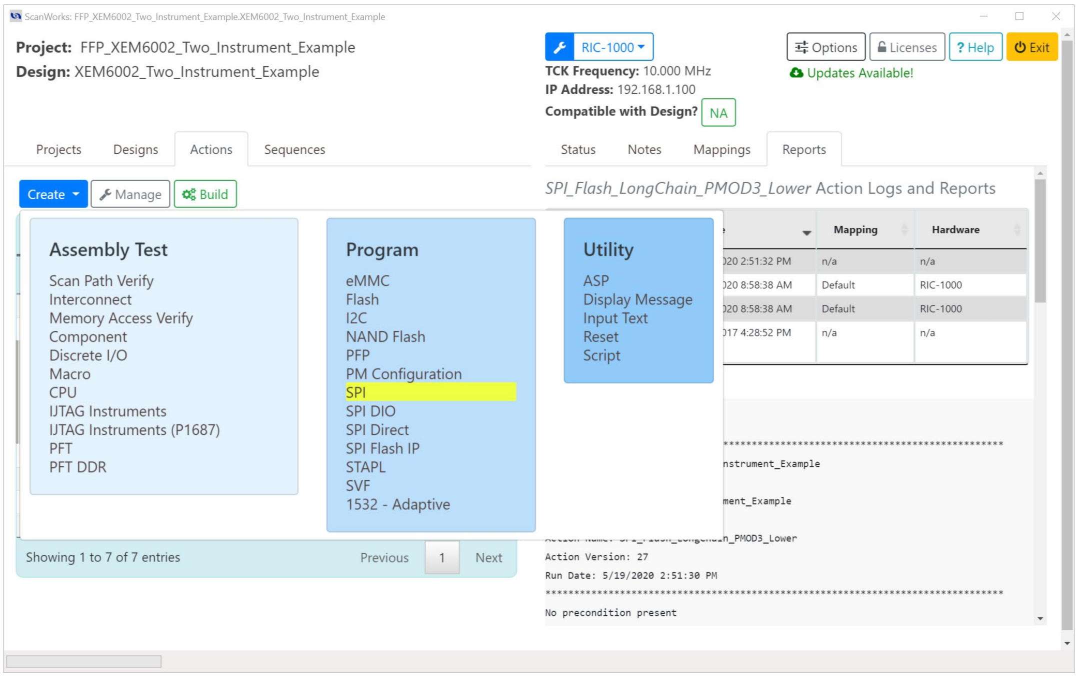


l. Select the blue Import icon next to "Source Files".
m. Browse to and double-click on the provided file named 2MB.bin.
n. Select Open to confirm the file as a Binary file.
o. Select the Build button.
p. Select the Save button.
q. Select the SPI_Flash_LongChain_PMOD3_Lower Run button below.
r. Confirm the action passed as shown below.



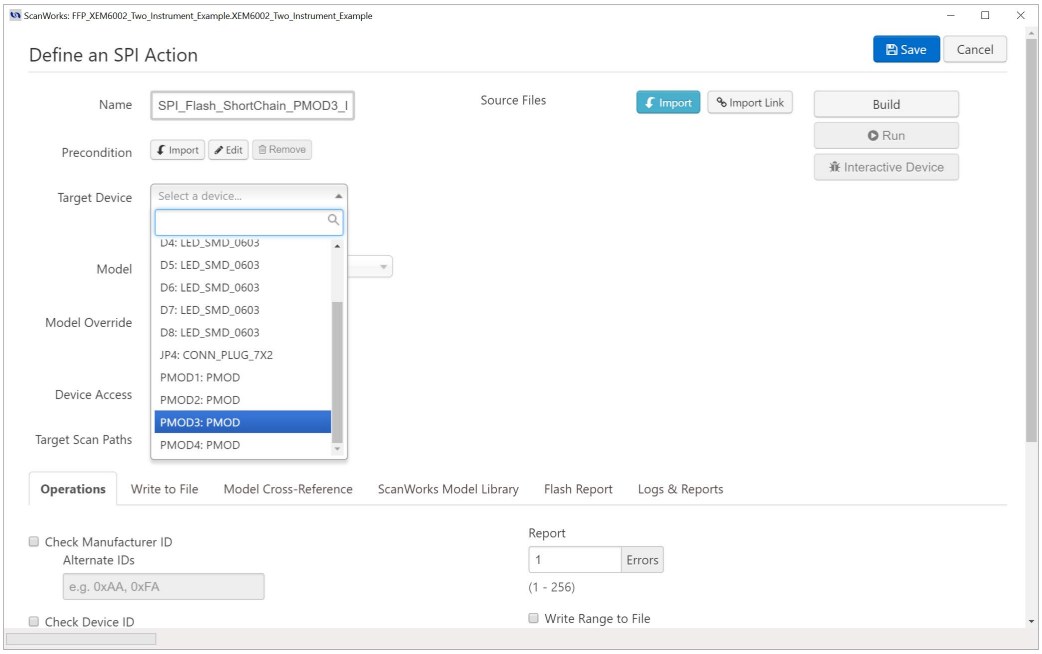
Create and run a standard Boundary Scan SPI Flash Action – Using the ETG short chain feature and PMOD3 lower position

a. Select the Actions tab.
b. Select the Create button.
c. Select the 'SPI' link.



d. Enter Name SPI_Flash_ShortChain_PMOD3_Lower

e. Select PMOD3 above as the device to program.



f. The Model should default to PMOD16_lower.cmp

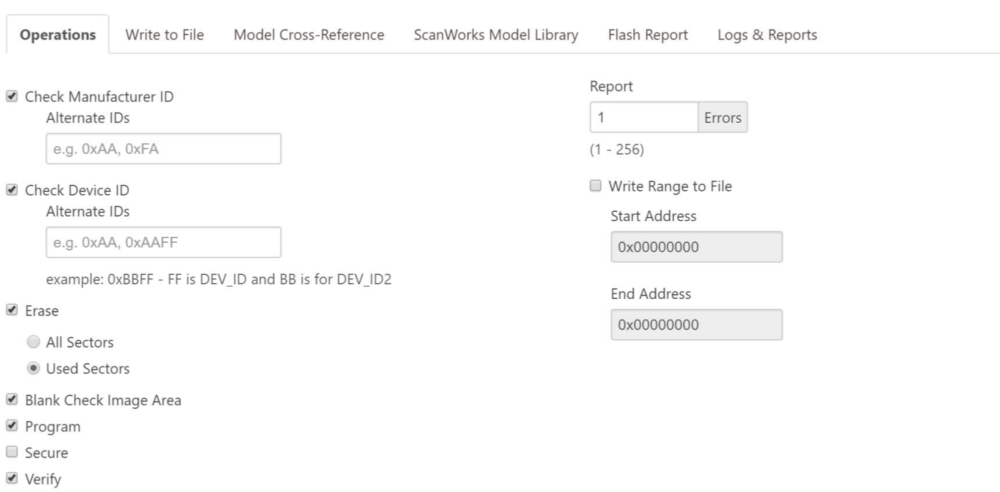
g. Device Access

    a. Select the Configure button.

    b. Ensure the Boundary Scan Master is U1

h. Select the OK button.

i. Select the two ID Checks, Erase, Blank check, Program, and Verify boxes.

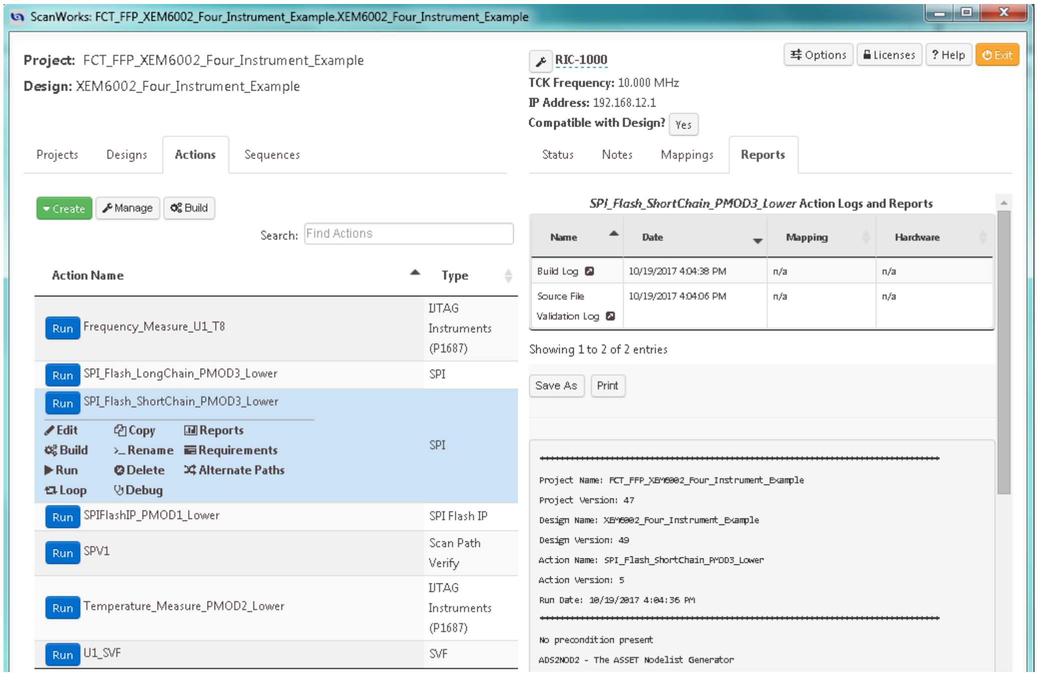


j. Select the blue Import icon next to “Source Files”.

k. Browse to and double-click on the provided file named 2MB.bin.

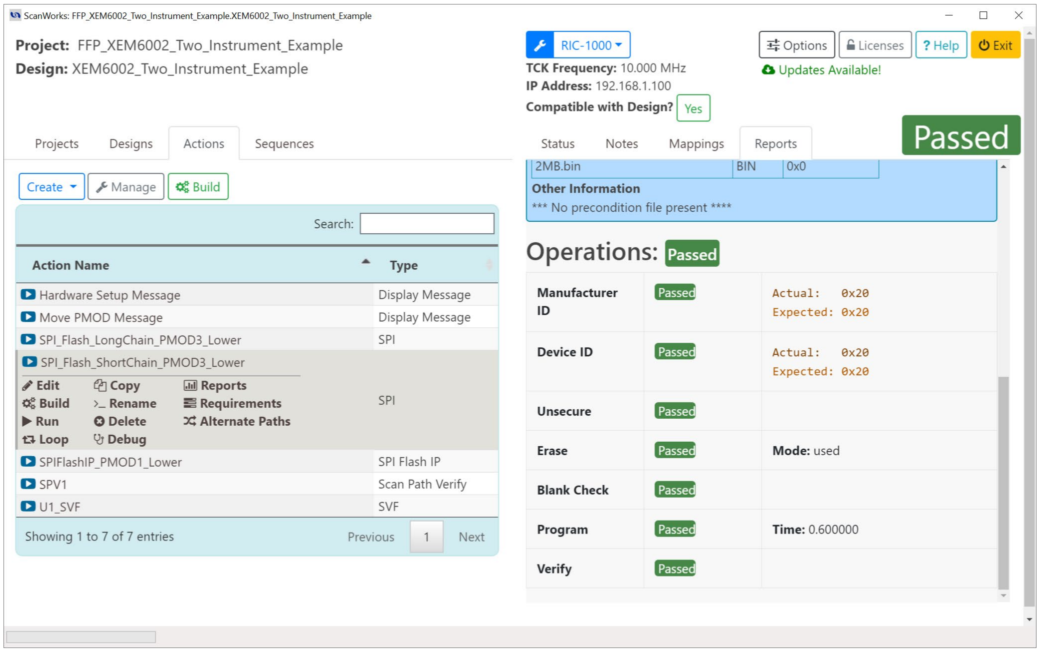
l. Select OK to confirm the file as a Binary file.

m. Select the OK button.
n. Select the Build button.
o. Select the Save button.
q. Single-click on the 'SPI_Flash_ShortChain_PMOD3_Lower' link below.



r. Select the 'SPI_Flash_ShortChain_PMOD3_Lower' Build button above.
s. Select the SPI_Flash_ShortChain_PMOD3_Lower Run button below.

t. Confirm the action passed as shown below.



7. Export the Project

The project should be exported for archiving purposes.

a. Select /Project/Export/
b. FFP_XEM6002_Two_Instrument_Example
c. Browse to desired folder to save the export.
d. Select Development/Archive (full)
e. Select the next
f. Select Export button

Note: that the example project also contains a sequence and other actions, but this documentation does not cover the generation of the other actions. For more information to export ScanWork and the Embedded Test capabilites refer to the Appendix.

APPENDIX

1. Other ETG Example Projects

Other ETG Example projects can be found at C:\ScanWorks\ETG\Examples folder. These example projects are provided as examples of what is possible with ScanWorks FPGA Contolled Test (FCT) and ScanWorks Fast Flash Programming (FFP) tools. Within the folder are example instrument projects that are based upon the type of license they use either FCT or FFP.

The structure of the project file name is as follows: <Tool License Type>_<Hardware Target Platform or device>_<Number of embedded instruments>.zip.

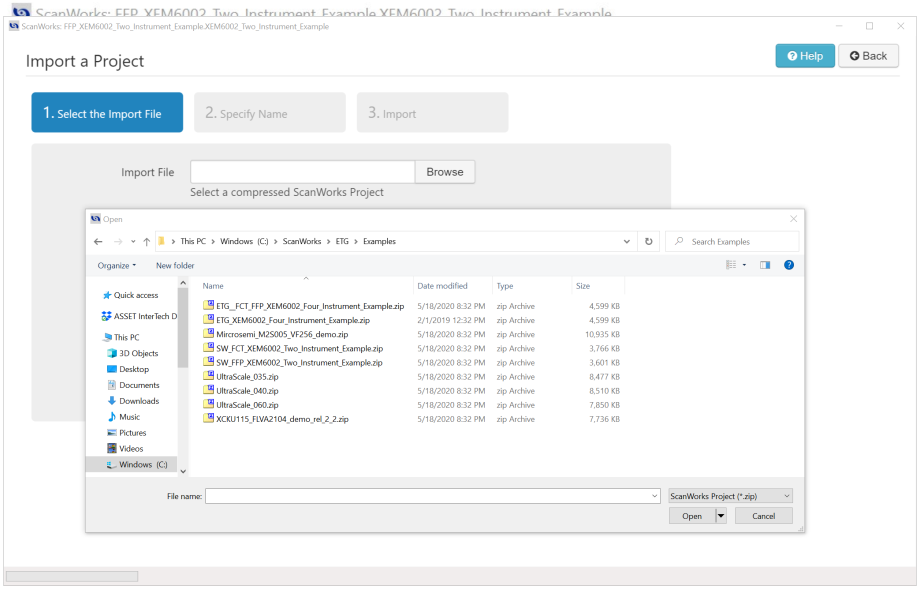
The ETG projects support the Opal Kelly XEM6002 board but, this board is not needed for the SVF generation by ETG. The ScanWorks projects are based on the Opal Kelly XEM6002 board and provide for the flashing of the device(s). Some target an SPI Flash PMOD and some target a temperature controller PMOD which are additional hardware connected to the PMOD interface of the board.

File	Comment
FFP_XEM6002_Two_Instrument_Example.zip	ScanWorks project with FFP instruments
FCT_XEM6002_Two_Instrument_Example.zip	ScanWorks project with FCT instruments

2. To Import ETG example project

a. With ScanWorks open

b. Select the Project tab and Select Import



c. Select Browse and browse to /ScanWorks/ETG/Examples

d. Select the project of interest and explore the project, design, and actions.