SCANWORKS FPGA-BASED FLASH PROGRAMMING Α **TWO INSTRUMENT EXAMPLE GUIDE** FOR **OPAL KELLY XEM6002** HARDWARE

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Purpose

The purpose of this document to instruct the user on the steps nessssary in using FPGA Module in the Design Resources tab found in ScanWorks 4.8 and higher. This is a new feature that provides the ability to create embedded instruments within an FPGA using ScanWorks FPGA-based Contolled Test (FCT) and ScanWorks FPGA-based Flash Programming (FFP) tools. To use this feature, either FCT or FFP tools must be licensed.

This document will cover only the ScanWorks FPGA-based Flash Programming (FFP) project setup and implementation.

The implementaion will cover the generation of the embedded instruments and the creation of the project actions necessary to exercise the embedded instruments.

The target for this manual is an Opal Kelly XEM6002 target with a PmodSF SPI Flash.







Notes:

Embedded Tester Generator (ETG) is the UI software component of the ScanWorks FPGA-based Fast Programming.

The ETG Release Notes can be found at C:\ScanWorks\ETG\ETG_ReleaseNotes.pdf please review the release notes to see the most current information on the release.

Microsemi Libero tool produces STAPL files not SVF and thus the ScanWorks action to program a Microsemi device should use a STAPL action and not an SVF action.

Customers must have access to in-house FPGA synthesis tools.

Note that once you define FPGA pins as output/bidir for an instrument, you cannot use the same pins for another instrument within the same embedded tester.

With ETG you could define two different Embedded Testers, however at this time ScanWorks cannot handle multiple embedded testers.

All FPGA pins being declared within ETG, should be researched in the FPGA datasheet, to see if they are declared as dedicated pins. If so, manual tool manipulation may be needed.

The SPI Flash IP, SPI Master and Frequency Measure instruments require that the FPGA have an active clock input. This clock will be used as a reference and while 100 MHz would be ideal, the acceptable range is 50-200 MHz

The Frequency_Measure IP instrument currently requires a free-running TCK, therefore the USB-100 controller will not work with this type of action.

ASSET support should always get the FPGA and target part numbers from the customer and run them by ASSET development to confirm that they are supported.

If the combined project name and embedded instrument names are too long, you might not be able to import the exported ETG project, Case-32462.

Normally you can use the Make button to compile just the .hgl file. There is currently a bug which requires that you use the Build button instead of the Make button. Case-27013.







Overview

This FPGA Module Example will instruct you on the following:

- a. Install prerequisites
- b. Build and download the ASSET Web Deployment Installer
- c. Install ScanWorks and ETG
- d. Request and install ScanWorks and FFP licenses
- e. Configure the Embedded Tester Generator (ETG)
- f. Use ETG to generate the FFP/ETG files
- g. Create a ScanWorks project/design
- h. Generate and run FFP actions

Prerequisites - Download and install

1. FPGA EDA Tools

To generate an FPGA instrument project, you must have access to the FPGA device manufacturer's synthesis tool for that specific FPGA. For this Example, which uses a Xilinx Spartan-6, XC6SLX9 FPGA, the ISE Design Tools are needed. The Xilinx_ISE_DS_14.7_1015_1.tar free installation can be downloaded from the Xilinx Download website. A username and password are needed on the Xilinx website.

- a) Download Xilinx_ISE_DS_14.7_1015_1.tar file from Xilinx website.
- b) Unzip the above downloaded .tar file to a temporary folder.
- c) As administrator, run the xsetup.exe file from the temporary folder. Select all defaults except for selecting ISE WebPACK as the package to install and selecting 'Get Free ISE WebPACK License' for acquiring a License.







2. Opal Kelly Tools

This manual uses the Opal Kelly XEM6002 target with a PmodSF SPI Flash connected to POD 1 or POD 3 (depending on the action) on the Opal Kelly board. Shown in figure 1.



Figure 1 Opal Kelly XEM6002

The Opal Kelly XEM6002 has a FrontPanel software that needs to be installed. This interface is used to control the frequency of the FPGA and will be describe later in the manual. This software can be found at <u>https://pins.opalkelly.com/</u> however, this will require the user to create a login to download the softare and proof of purchase of the hardware.

After installing the FrontPanel software and connecting the ScanWorks controller (this example will use the RIC-1000). Start the Opal Kelly interface as shown below.



Plugin the USB cable to the Opal Kelly Board and to the host where the FrontPanel and ScanWorks resides. The FrontPanel will look similar to the interface shown below.









Later in the project we will configure the board with this FrontPanel application.

ScanWorks Software Installation

3. ETG Installer – Run

If you already have ScanWorks 4.8 installed, and are only installing ETG using the ETG Installer, continue below. If you are going to use the ASSET Web Deployment Installer to install ScanWorks and ETG, and perhaps other packages, proceed to <u>ASSET Web Deployment Installer</u> below.







a. Double-click on the provided ScanWorks ETG_Setup.exe



b. Select the Next button above.







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🔂 ETG	
Select Installation Folder	
The installer will install ETG to the following folder.	
To install in this folder, click "Next". To install to a different folder, click "Browse".	enter it below or
<u>F</u> older:	
C:\ScanWorks\Exe\	Browse
	Disk Cost
Install ETG for yourself, or for anyone who uses this computer:	
Everyone Everyone	
🔘 Just me	
Cancel < Back	Next >

- c. Next, browse to the ScanWorks\Exe folder and select Everyone or Just me. Or use the defaults if appropriate.
- d. Select Next button as shown above.





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e. Confirm the Installation by selecting Next button.

1 ETG			
Installing ETG			
ETG is being installed.			
Please wait			
	Cancel	< Back	Next >









f. The installation will begin as shown above.

- g. When the install completes as shown above, select the Close button.
- h. Proceed to step 6 below.

4. ASSET Web Deployment Installer - Build and download

For this procedure use the link that was provided by ASSET order Fulfillment to build and download a custom installer program. Save this link as it is an active link and may be needed in the future for updating to never software revisions.

Click on the link provided by ASSET or paste it into your browser. The online instructions mention the methods for obtaining your ScanWorks license. Follow the online instructions to build and download the custom installer. The name of the custom installer reflects the versions of ScanWorks and ETG.

Example: ASSET_WDI_ScanWorks.4.9.0.0-CreoView.10.2.20.23-CreoViewEA.10.2.20.23-ScanWorks_Platform.2.5.0.0-ETG.3.2.0.0.exe







5. ASSET Web Deployment Installer - Run

Note: the following is an example of the steps necessary to use the WDI installer. Your exact experience will vary slightly from this example.

- a. Run the installer as administrator.
- b. Accept the license agreement.

Installation Settings			
ScanWorks			
Target Directory:	C:\ScanWorks		
Setup Type:	 Development Diagnostic and Repair Programming 	Manufacturing	
		<u> </u>]

c. Select the appropriate Setup Type above and select the OK button.

arrow Web Deployment Installer - ASSET InterTech	- 0	×
Install Selected Install All Remove Selected Remove All Settings Disable Messsages	Show Contents	About
Software included in this package		
Not installed Version: ScanWorks Release Date: Install Install	ScanWorks.4.9.0.0 11/16/2020 ₽₽ More	^
 Not installed Version: Creo View Release Date: Install 	Creo View. 10.2.20.23 8/8/2014 2 More	
 Not installed Version: Creo View ECAD Adapters Release Date: Install 	Creo ViewEA.10.2.20.23 5/2/2014	
Not installed Version: ScanWorks Platform Release Date: Install Install	ScanWorks_Platform.2.5.0.0 11/16/2020	
Not installed Version: Release Data	ETG.3.2.0.0	~
Installed		
Installed software Dog		

d. Select the Install All button above. (If you already have some packages installed, you can select only the ones needed and select 'Install Selected')









e. Select the Yes button above to accept the selections and start the install.

Heb Deployment Installer - ASSET InterTech		- 0	×
Install Selected Install All Remove Selected Remove All Settings Disable Messsages		Show Contents	About
Software included in this package		_	
✓ Installed ScanWorks ☐ Reinstal	Version: Release Date:	ScanWorks.4.9.0.0 11/16/2020	
✓ Installed Creo View ☐ Reinstal Finished ×	Version: Release Date:	Creo View.10.2.20.23 8/8/2014	
Installed Creo View ECAD Adapters Reinstal Software installation complete.	Version: Release Date:	Creo View EA.10.2.20.23 5/2/2014	
✓ Installed ScanWorks Platform OK OK	Version: Release Date:	ScanWorks_Platform.2.5.0.0 11/16/2020	
✓ Installed ETG Renstal	Version: Release Date:	ETG.3.2.0.0 11/16/2020	
Installed ScanWorks		Version: 4.9.0 Date installed: 12/8/2020	^
The Installed software Control Log			~

- f. Select OK above when the installation completes.
- g. Close the Web Deployment Installer window above.

Session Lo	yg ×
?	Session log has been created in the folder C:\Users\LOsborn\AppData\Local\Temp\PlatformInstaller.Logs\ 12_08_2020-07,49_04.8 Would you like to see the contents (Y/N)?
	Yes No

h. Answer as desired above.

A ScanWorks ICON will be on the desktop when the installation is complete. Restart the computer.







Licensing

- 6. Request, Receive and Install Boundary Scan/ FFP/FFP Licenses
 - a. Refer to the email that you received for the order, or the document named C:\ScanWorks\doc\GettingStarted.pdf, to request, receive and install the Boundary Scan/FFP licenses.
 - b. After the licenses have been installed, open ScanWorks, using the License Manager window, select the boundary scan and FFP licenses that you intend to use. Note that all licenses checked will be immediately consumed when you open ScanWorks.

Request a New License				
Products Found in Licenses	Licenses in Use			
elect which products you want to use. The selected	Add Server			
	Add License			
FCT DEV FOR BST OPTION	Licenses and Servers	Туре		
	C:\Licenses\FFP\License-BST-ONLY-004407-008972-LarryO-022821v4.lic	local		
	C:\Licenses\FFP\License-FCI-ONLY_009258-LarryO-v2.lic	local		

c. Close ScanWorks or select Back and ScanWorks will close.







Using FPGA Module

- 1. Getting Started with FPGA Module
 - a. Start by creating a new ScanWorks project and create the Design Note: This document will not provide the instructions for creating a project or design. We assume that the user is experience with ScanWorks. Also, we assume that a FPGA is within the Design
 - b. Select the Action tab and create an SPV action
 - c. Select the SPV action an verify the action passes. An example is shown below

ScanWorks: FFP_XEM6002_Two_Instrument_Example.XEM6002_Two_Instrument	it_Example	- 🗆 X			
Project: FFP_XEM6002_Two_Instrument_Examp	le	▶ RIC-1000 ▼ ▲ Licenses Placenses Placenses			
Design: XEM6002_Two_Instrument_Example		TCK Frequency: 10.000 MHz IP Address: 192.168.1.100 Compatible with Design? Yes			
Projects Designs Actions Sequences		Status Notes Mappings Reports Passed			
Create 🔹 💉 Manage 🗞 Build		*** Starting IR Capture test *** IR Capture test PASSED for TAP 1			
Se Action Name	Type	*** Starting BYPASS test *** BYPASS test PASSED			
Hardware Setup Message	Display Message	*** Starting IDCODE test ***			
Move PMOD Message	Display Message	IDCODE for Device U1 in tap 1 PASSED			
SPI_Flash_LongChain_PMOD3_Lower	SPI	Expected data: XXXX0100000000000000000000000000000000			
SPI Flash ShortChain PMOD3 Lower	SPI				
SPIFlashIP PMOD1 Lower	SPI Flash IP				
		*** Starting Boundary Length test ***			
<i>P</i> Edit ⁽²⁾ Copy ⁽²⁾ Copy ⁽²⁾ Reports ⁽²⁾ Requirements ⁽²⁾ Requirements ⁽²⁾ Requirements ⁽²⁾ Copy ⁽²⁾ Copy ⁽²⁾ Find Max TCK ⁽²⁾ Copy	Scan Path Verify	Boundary Length test PASSED for TAP 1.			
▶ U1_SVF	SVF	Expected data: XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX			
Showing 1 to 7 of 7 entries	Previous 1 Next	Measured data: 111111111111111111111111111111111			
		Test completed successfully			

d. Select the Design tab and in the Design Resources and select FPGA Modules







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canWorks: FFP_XEM6002_Two_Instrument_Example.XEM6002_Two_Instrument_Example		
NORS EIG		
s Embedded Tester Instrument Instance Synthesis FPGA Instrument Library Help		
Current Project: ETSet	Project Tree	
Current Embedded Tester:	⊖-Project: E	TSet
Current Instrument Instance:	- Embe	dded Testers
Washing		.T_0 ≜⊢FPGA
List of available instruments was not found. I can import an instrument library by selecting the menu item trument Library-Import •supported device libraries can be found at \ScanWorks\ETG\LibraryExports.		 Levelor Viol Franky service reference Desoy hot <lidesoy hot<="" li=""> Desoy hot Desoy hot</lidesoy>
ng project: ETSet		

- e. The ScanWorks ETG window will open
- f. Follow the directions in the above screen. The browser will open as shown below.

anize 🔻 New folde	er				
^	Name	Date modified	Туре	Size	
Quick access	🗳 Altera.zip	6/9/2020 8:33 AM	zip Archive	1,725 KB	
ASSET InterTech D	Instruments.zip	6/9/2020 8:33 AM	zip Archive	4,413 KB	
This PC	🖾 Microsemi.zip	6/9/2020 8:33 AM	zip Archive	167 KB	
3D Objects	🖾 Xilinx.zip	5/14/2020 8:24 AM	zip Archive	47,186 KB	
Desktop					
Documents					
- Downloads					
Music					
Pictures					
Videos					
Windows (C:)					

g. Select Instruments.zip Open







ScanWorks ETG		- 🗆 ×
Settings Embedded Tester Instr	ument Instance Synthesis FPGA Instrument Library Help	
Disable Logging View Log File	ETSet en: Gran	Project Tree
Delete Log File		
<u>Evit</u>		
Results		
Opening project: ETSet		

h. Select Settings -> ETG Settings

i. Now Configure the EDA tools locations as needed based upon the tool vendor. Shown below is an example with all three (Altera, Xilinx and Microsemi (a Microchip Company)) EDA tools are configured.

-		
Projects Root Directory	C:\ScanWorks\Projects\FFP_XEM6002_Two_Instrument_Example\XEM6002_Two_In	
Altera FPGA Tool Settings		
Usage	Quartus ~	
Quartus_sh Path	C:\intelFPGA\19.1\quartus\bin64\quartus_sh.exe	Browse
Xilinx FPGA Tool Settings		
Usage	ISE v	
PlanAhead Path	C:\Xilinx\14.7\ISE_DS\PlanAhead\bin\planahead.bat	Browse
Impact Path	C:\Xilinx\14.7\ISE_DS\ISE\bin\nt\impact.exe	Browse
Vivado Path	C:\Xiinx2019.1\\Ivado\2019.1\bin\vivado.bat	Browse
Microsemi FPGA Tool Settings		
Usage	Libern V	
Libero Path	C:\Microsemi\Libero SoC v12.0\Designer\bin\libero exe	Browse

Select Save once you have configured the EDA tools you plan to use. For this example, we will be using Xilinx tools.

2. Importing the supported FPGA devices

a. The final step in preparing for the use of the FPGA Module is to import the FPGA devices support by the ScanWorks tool.







- b. Select FPGA in the ScanWorks ETG window
- c. Select Import

Settings	Embedded Tester	Instrument Instance	Synthesis	FPGA	Instrument Library	Hel
	Current Project: ETSe Current Embedded Tester: Current Instrument Instance:			V	/iew	
				F	ilter Lists	
				Import		
				E	xport	

- d. Browse to \ScanWorks\ETG\LibraryExports
- e. Select the appropriate FPGA family zip file. For this project we are using Xilinx FPGA
- f. Select yes if prompted to replacing local FPGA information for each FPGA imported.
- g. The importing will complete. If you have other FPGA device families you wish to use, repeat the steps above to import the other devices.

Embedded Tester Creation

3. Create an Embedded Tester

Embedded Testers are containers which hold instruments. Embedded Testers can contain a single instrument or multiple instruments. A ScanWorks design can currently only use a single embedded tester, so if you want to use multiple instruments you are better off putting them in a single embedded tester. That is assuming they will all fit into the FPGA being used.

The data input for these examples will be in a cyan color.







🐚 ScanWorks ETG		- 0
Settings Embedded T	ter Instrument Instance Synthesis FPGA Instrument Library Help	
Open Close Delete	t: ETSet ded Tester: , ment listance:	Project:Tree Project:ETSet Ho Embedded Testers
Results		
Created Project: Opening project:	Tšee Tšee	

a) Select Embedded Test/New to create a new Tester.

- b) Provide a name that is descriptive. Something with the instrument type and hardware could be used. FFP Two Instrument
- c) Enter a user defined name for the project and select the OK button. **Naming Rules**: Must start with a letter and only use letters, numbers, dashes, and underscores.
- d) Enter a user defined description for the embedded tester.
- e) Select the FPGA VENDOR Xilinx
- f) Select the FPGA FAMILY Spartan6
- g) Select the FPGA PART xc6slx9ftg256-2







h) Select the Save button.

ScanWork	s EIG	- 🗆 X
Settings I	Embedded Tester Instrument Instance Synthesis FPGA Instrument Library Help	
	Current Project: ETSet	Project Tree
	Current Embedded Tester:	
L	Current Instrument Instance:	Embedded Testers
Create Embed	Jded Tester	
Name	RCT_Two_instrument	
Description	Frequency and Tempature	
FPGA	Vendor Family Part XBinx Ispatian6 ixo6id/902562 Cancel Save	
Dente		<u>,</u>

Note: the project tree that is being generated on the right side of the window.

4. Adding Instruments to the Embedded Tester

- I. Add an instrument to create a Short Chain for programming the SPI Flash at PMOD3, lower position.
 - a. Select Instrument Instance ADD...

🐚 ScanWo	rks ETG							
Settings	Embedded Tester	Instrument Instance Sys	nthesis	FPGA	Instrument Library	Help		
	Current Projec	Add	TSe					
	Ourrent Embe	Select	·					
	contine Empe	Delete	• 1'-'					
	Current Instru	Edit Parameters						
		Edit Pin Map						
			_					

- b. Enter a user defined name for the instrument. ShortChain SPIFlash PMOD3 lower
- c. Select the Instrument Type.
- d. Select the Instrument Name.



e. Select the Instrument Version.







f. Select the Save button below.

Add Instrument Instance			
Name	atChain_SPIFlash_POD3_Lower		
Instrument Type	GPIO V		
Instrument Name	BST_IO v		
Instrument Version			
		Cancel Sav	e

g. Select Instrument Instance/Select/ShortChain_SPIFlash_PMOD3_Lower.

ScanWorks ETG		
Settings Embedded Tester	Instrument Instance Synthe	isis FPGA Instrument Library Help
Current Projec	Add	TSet
Ourrent Embe	Select +	ShortChain_SPIFlash_PMOD3_Lower
	Delete +	SPIFlashPlayer_PMOD1_Lower
Current Instru	Edit Parameters	INDICCIDAIN_BHINABIL_FMOUD_LOWEI
	Edit Pin Map	

h. Select Instrument Instance/Edit Parameters.

🔄 ScanWorks ETG

Settings Embedded Tester	Instrument Instance Synthe	esis FPGA Instrument Library Help
Current Proje	Add	TSet
Ourset Embr	Select +	
Current Embe	Delete +	
Current Instru	Edit Parameters	ShortChain_SPIFlash_PMOD3_Lower
	Edit Pin Map	

i. The parameters for this instrument are the ports/pins that you want in the short chain. Note that buses can also be declared in ScanWorks to control these pins. For this example, change them as shown below.

a.	INPUT	MSIO
b.	OUTPUT	MOSI, SCK, SSEL





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	Current Project:	E	TSet	
	Current Embedd	ed Tester: E	<u>_</u> 0	
	Current Instrume	ent Instance: Si	ortChain_SPIFlash_PMOD3_Lower	
uura laetau	ment Darameters fo	ar Short Chain SDIElach DMOD	Louise	
Name	Data Type	Value	Description	
INPUT	string	MSIO	Comma separated list of INPUT signal names. Use square brackets for bus range (e.g., addr(15:0)). Base signal name must match this regular expression /*[A-Za-:1][A-Za-:0-9_]+5/.	Export
UTPUT2	string	MOSI,SCK,SSEL	Comma separated list of OUTFUT2 signal names. Use square brackets for bus range (e.g., LED[3:0]). Base signal name must match this regular expression /^[A-2a-1_][A-2a-10-9_]+5/.	Import
UTPUT3	string		Comma separated list of OUTPUT3 signal names. Specify signal busses with square brackets (e.g., LED[3:0]). Base signal name must match this regular expression //[A-2a-1][A-2a-10-9]=45/. Create OE groupings with curly braces (e.g., sig1, (sig2, sig3), sig4). Signals that are not listed inside of curly braces will get their own OE.	
BIDIR	string		Comma separated list of BIDIR signal names. Specify signal busses with square brackets (e.g., LED[3:0]). Base signal name must match this regular expression //[h-2a-1][h-2a-t0-9]+5/. Create OE groupings with curly braces (e.g., sig1, (sig2, sig3), sig4). Signals that are not listed inside of curly braces will get their own OE.	Cancel
				Save and Replace Pin Map

- j. Select the 'Save and Replace Pin Map' button above.
- k. Select Instrument Instance/Edit Pin Map.

ScanWorks ETG

Settings Embedd	led Tester Instrument Instance	Synthesis FPGA Instrument Library Help
Curi	rent Projec Add	TSet
Curi	Select	• FT_0
	Delete	•
Cun	Edit Parameter	s snortchain_SPIFiash_PMOD3_Lower
	Edit Pin Map	

1. Enter the 'FPGA Pins' as needed.

a.	MISO	K16
b.	MOSI	H16
c.	SCK	M16
d.	SSEL	F16

m. Enter the required I/O Type of the FPGA pins. LVCMO533





n. Select the Save button below.

Current Project: ETSet Current Embedded Tester: ET_0 Current Instrument Instance: Shortt							
Current Embedded Tester: ET_0 Current Instrument Instance: Shortt							
Current Instrument Instance: Shortd							
Current Instrument Instance: ShortChain_SPIFlash_PMOD3_Lower							
It Instrument Instance Pin Map for ShortChain, SPIFlash, PMOD3 Lower							
Port Direction Port Name FPGA Pin	FPGA Pin I/O Type						
INPUT MSIO K16	LVCMOS33 Exce						
OUTPUT2 MOSI H16	LVCMOS33						
OUTPUT2 SCK M16	LVCMOS33						
OUTPUT2 SSEL F16	LVCMOS\$3						

II. Add an SPI FlashPlayer instrument to program the SPI flash device at PMOD1, lower position.

SPI FlashPlayer

SPI FlashPlayer

1

- a. Select Instrument Instance/Add.
- b. Enter a user defined name for the instrument. SPIFlashPlayer_PMOD1_Lower
- c. Select the Instrument Type.
- d. Select the Instrument Name.
- e. Select the Instrument Version.

- $g. \ Select / Instrument \ Instance / Select / SPIF lash Player _ PMOD1 _ Lower.$
- h. Select /Instrument Instance/Edit Parameters.







The parameters for this instrument are defined below and are adjustable. SPI_POLARITY Controls SCLK polarity relationship of SPI interface (target device dependent)

SPI_PHASE Controls SCLK phase relationship of SPI interface (target device dependent)

i. Edit the parameters as needed, (leave as is for this example).

	a.	SPI_P	OLA	RITY 0	
	b.	SPI P	HAS	E 0	
ScanWor	ks ETG	_			
Settings	Embedded Tester	Instrument Instance	Synthesis	PGA Instrument Library Help	
	Current Proje	ct:	ETSet		
	Current Embe	edded Tester:	ET_0		
	Current Instru	ument Instance:	SPIFlas	Pbyer_PMOD1_Lower	
Configure In:	strument Paramete	rs for SPIFlashPlayer_PM	OD1_Lower		
SPI_POLAF	Data Type RITY integer	Value 0		Controls SCLK polarity relationship of SPI interface.	Great
SPI_PHA	SE integer	0		ontrols SCLK phase relationship of SPI interface.	Export
					Import
					Cancel
					Save
i.	Select	the 'Say	ve' b	utton.	
J. 1_	0.1	T		Γ 1' Γ 1' Γ 1' Γ	
К.	Select	Instrum	ient I	nstance/Edit Pin Map.	
1.	Enter	the 'FPO	GA P	ins' as needed.	
	a.	sysclk		Τ8	
	b.	miso		F1	
	c.	DO pi	n[2]	~P1	
	d.	DO ni	n[1]	~N1	
	e	DO_{ni}	n[0]	~M2	

- e. DO_pin[0]
 ~M2

 f. mosi
 E2

 g. sclk
 G1

 h. ssel
 E1
- m. Enter the required I/O Type of the FPGA pins. LVCMOS33
- n. Select the Save button.







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Settings	Embedded Tester	Instrument Instance	Synthesis	FPGA	Instrument Library	Help		
	Current Projec	ct:	ETSe	et -				
	Current Embe	dded Tester:	ET_0	,				
	Current Instru	iment Instance:	SPIE	ashPlave	r PMOD1 Lower			
				,				
it Instrum	ent Instance Pin Map	p for SPIFlashPlayer_PM	10D1_Lower					_
Port Dire	tion Port Name	FPGA Pin					FPGA Pin I/O Type	
INPUT	sysclk	T8					LVCMOS33	Export
INPUT	miso	F1					LVCMOS33	
OUTPU	F DO_pin[2]	~P1					LVCMOS33	Import
OUTPU	F DO_pin[1]	~N1					LVCMOS33	mpon
OUTPU	F DO_pin[0]	~M2					LVCMOS33	
OUTPU	r mosi	E2					LVCMOS33	Cance
OUTPU	r sdk	G1					LVCMOS33	_
OUTPU	r ssel	E1					LVCMOS33	Sauce
OUTPU	r ssel	E1					LVCMOS33	

The three D0_pins declared above are static pins with a default state of 1 due to the \sim . Since they are declared in this instrument, these pins can be set high or low within the ScanWorks SPI IP action, just as they could be in a standard SPI action. In the Opal Kelly design these pins are connected to D6, D7 and D8. Removing the \sim will illuminate these LEDs when the SVF is loaded into the FPGA.

In this case the two desired instruments have now been added to the new embedded tester.

5. Synthesis Steps for the Embedded Tester

- III. Establishing Network Order
 - a. Select /Synthesis/Set Network Order.



- b. The order of the instruments can be changed, but leave as is for this example.
- c. Select the Save button above.







d. Select /Synthesis/Generate Wrapper.

ScanWorks E	IG			
Settings Em	bedded Tester Instru	ment Instance	Synthesis FPGA Instrume	ent Library Help
Current Project:		Set Network Order		
		Generate Wrapper		
Current Embedded Tester.			Edit Constraints	
Current Instrument Instance:		Synthesize	ler	
			View FPGA Usage	
			View Synthesis Report	
			View Map File	
			Generate SVF	

e. The Wrapper should generate as shown below.

Renda	
	^
Creating Network File	
curToken: IP Files	- 10
curToken: IP Ports	
Network File Created successfully	
Generating P1687 wrapper for ET_0	
gin.exe: INFO: The Configuration File provided is "C:\ScanWorks\Projects\FFP XEM6002 Two_Instrument_Example\XEM6002_Two_Instrument_Example\ETSet\ET_0\Synthesis\ET_0.Conf."	
gin.exe: 0 Errors, and 0 Warnings	
Generating P1687 wrapper for ET_0 done	
	24

f. Select /Synthesis/Synthesize.

Settings Embedded Tester Instrument Instance Synthesis FPGA Instrument Library Help Current Project: Current Embedded Tester: Generate Wrapper Edit Constraints.... Generate View FPGA Usage View FPGA Usage View Synthesis Report View Map File Generate SVF... Generate SVF...

g. The Synthesis should finish as shown below.

F	16/8	
-	NFO : À ISE results summary will be written to:	^
	C:\ScanWorks\Projects\FFF_XEM6002_Two_Instrument_Example\XEM6002_Two_Instrument_Example\ETSet\ET_0\Synthesis\FpgaUsage.rpt	
ŀ		
	ymthesis done	10
н		~

- h. Select /Synthesis/View Synthesis Report.
- i. Review the report for any warnings or errors.

6. Create SVF File Step

- I. Create an SVF file
 - a. Select Synthesis/Generate SVF...







SCANWORKS FPGA-BASED FLASH PROGRAMMING A TWO INSTRUMENT EXAMPLE GUIDE

Settings Embedded Tester Instrument Instance	Synthesis FPGA Instrument Library Help	
Current Project:	Set Network Order	
Ourrent Embedded Tester:	Generate Wrapper	
current Embeudeu Tester.	Edit Constraints	
Current Instrument Instance:	Synthesize ///	
	View FPGA Usage	
	View Synthesis Report	
	View Map File	
	Generate SVF	

b. Select the Generate button below.

🔄 ScanWo	orks ETG							
Settings	Embedded Tester	Instrument Instance	Synthesis	FPGA	Instrument Library	Help		
	Current Proje	ct:	ETSe	t				
	Current Embe	dded Tester:	ET_0					
	Current Instru	iment Instance:	SPIF	ashPlaye	_PMOD1_Lower			
Generate SV	(F							
lr Outp	nput BIT File et_0.bt			Car	rate			

c. The SVF generation should finish as shown below.

Results		
C:\Xilinx\14.7\	ISE DS\ISE\bin\nt\impact:	LCK cycle = NoWait.
C:\Xilinx\14.7\	ISE_DS\ISE\bin\nt\impact: 1	LCK cycle: NoWait
C:\Xilinx\14.7\	ISE_DS\ISE\bin\nt\impact: (done.
C:\Xilinx\14.7\	ISE_DS\ISE\bin\nt\impact:	LCK_cycle = NoWait.
C:\Xilinx\14.7\	ISE_DS\ISE\bin\nt\impact:	LCK cycle: NoWait
C:\Xilinx\14.7\	ISE_DS\ISE\bin\nt\impact:	'1': Programmed successfully.
C:\Xilinx\14.7\	ISE_DS\ISE\bin\nt\impact: 1	Elapsed time = 1 sec.
C:\Xilinx\14.7\	ISE_DS\ISE\bin\nt\impact:	0 Errors, and 0 Warnings
Creating SVF fi	Le ET_O done	
I		

d. Close the ScanWorks ETG window and return to the Design tab

7. Recap of ETG Steps

Now that the FPGA synthesis is complete and the SVF file has been generated, you can find all of the files needed for building a ScanWorks actions with FFP actions in the ScanWorks directory, in the given ET directory for the ETG Project. For this example, they are found at:

C:\ScanWorks\Projects\FFP_XEM6002_Two_Instrument_Example\XEM6002_Two Instrument_Example\ETSet\ET_0\ScanWorks

- Outputs of ETG
 - SVF Serial Vector Format
 - BSDL Boundary Scan Description Language
 - Pin Map







ScanWorks Setup

1. Select the ASSET Hardware

ScanWorks: FFI	_XEM6002_Two_Ins	trument_Example.X	EM6002_Two_Instrument_Example					-		\times
Project: FFP_XEM6002_Two_Instrument_Example Design: XEM6002_Two_Instrument_Example					are 🔻		Image: Contract of the second sec	ses ? Help	<mark>ර</mark> Ex	it
Projects	Designs	Actions	Sequences	Status	Notes	Mappings	Reports			
Defir	e the Des	ign	+ Create Import Designs	Project	Design	Sequence				
₽ Defir ೪ Netli	e the Scan Pat st, Schematic, 8	th & Layout	Madala	🖋 [edit no	otes]					

- a. Select the 'No Hardware' link above.
- b. Select the RIC-1000 from the drop-down menu.

No Hardware	
1	Q
LVI-TOOD	
RIC-1000	
RIC-1000PODII	
RIC-4000	
ETC2	
Teradyne	
USB-100	
USB-XDP3	-

c. Configure the hardware. The RIC-1000 configuration is shown here, but other controllers can have different options. 10MHz is required for this example and you would of cource use the appropriate IP Address for your RIC-1000.

Coture DIC 40	00 Hardwara	
Setup Ric-10	uu Hardware	OK
TCK Frequency (MHz):	Delay Compensation:	Cancel
10.000 ~	0	
		Help
TAP Voltage:	IP Address:	
3.3 ~	192.168.1.100	
Discrete IO TAP Vol	tados	
Discrete IO TAP Vol	tages	
Discrete IO TAP Vol Discrete IO Signal 0 and 1	ltages	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3	Itages I:	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3	tages t: ∽	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3 Discete IO Signal 2 and 3:	tages	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3 Discete IO Signal 2 and 3 3.3	Itages I: ·	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3 Discete IO Signal 2 and 3 3.3	Itages I: ∽ :	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3 Discete IO Signal 2 and 3 3.3 Discrete IO Signal 4 and 5	Itages 1: ~ :	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3 Discete IO Signal 2 and 3 3.3 Discrete IO Signal 4 and 5 3.3	Itages 1: ↓ : ↓ 5: ↓	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3 Discete IO Signal 2 and 3 3.3 Discrete IO Signal 4 and 5 3.3	Itages 1: ✓ : ✓ 5: ✓	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3 Discete IO Signal 2 and 3 3.3 Discrete IO Signal 4 and 5 3.3	Itages 1: ↓ : ↓ 5: ↓	
Discrete IO TAP Vol Discrete IO Signal 0 and 1 3.3 Discete IO Signal 2 and 3 3.3 Discrete IO Signal 4 and 5 3.3 Discrete IO Signal 6 and 7	Itages t: ✓ : ✓ 5: ✓ 7: ✓	







d. Select OK.







2. Create and run a Scan Path Verify (SPV) Action

- a. Select the Actions tab.
- b. Select the Create button.
- c. Select the 'Scan Path Verify' link.

ScanWorks: FFP_XEM6002_Two_Instrument_Example.XEM6002_Two_Instru	ment_Example		- 🗆 X
Project: FFP_XEM6002_Two_Instrument_Exar Design: XEM6002_Two_Instrument_Example	nple	RIC-1000 ~ TCK Frequency: 10.000 MHz IP Address: 192.168.1.100 Compatible with Design?	Image: Constraint of the second se
Projects Designs Actions Sequences		Status Notes Mappings	Reports
Create 🝷 🖋 Manage 📽 Build		Project Design Sequence	
Assembly Test Scan Path Verify Interconnect Memory Access Verify Component Discrete I/O Macro CPU UTAG Instruments UTAG Instruments (P1687)	Program eMMC Flash 12C NAND Flash PM Configuration SPI DIO SPI DIO SPI DIO SPI DIO SPI DIO SPI Flash IP STAPL SVF 1532 - Adaptive	Utility ASP Display Message Input Text Reset Script	
			*

- d. Below, accept the default or optionally you can rename the action.
- e. Select the build button.

Precondition Import Precondition Import Edit Remove Istruction Capture Precondition Precondit	Name	SPV1	Options	Buil
Precondition Instruction Capture ByPASS Instruction Capture Boundary-Scan Length Devices Target Scan Path(s) primary USERCODE Attenates TRST Devices		Classest & Citia @ Pomous	Device ID and Bypass DR Scan Only Alternates	O R
Launch Debugger Debug Primary	Precondition	Functional Sector	 Instruction Capture Pypage 	
Target Scan Path(s) 🗷 primary 🖉 Boundary-Scan Length Devices T Target Scan Path(s) 🖉 primary 📽 USERCODE Attenates T TRST Devices tition Logs and Reports lame Date Mapping Hardware	Launch Debugger	賽 Debug	✓ IDCODE Alternates	
Target Scan Path(s) <table-cell> primary 🛛 USERCODE Atternates TRST Devices tion Logs and Reports lame Date Mapping Hardware</table-cell>			Boundary-Scan Length Devices	
Ition Logs and Reports Iame Date Mapping Hardware				
tion Logs and Reports Jame Date Mapping Hardware	Target Scan Path(s)	primary	USERCODE Alternates	
	Target Scan Path(s)		USERCODE Atternates TRST Devices	
	Target Scan Path(s)	primary	USERCODE Atternates TRST Devices	
	Target Scan Path(s) ttion Logs and Reports lame	primary	USERCODE Atternates TRST Devices Mapping Hardware	
	Target Scan Path(s) ttion Logs and Reports lame	primary	USERCODE Atternates TRST Devices Mapping Hardware	
	Target Scan Path(s) ction Logs and Reports lame	primary	USERCODE Atternates TRST Devices Mapping Hardware	
	Target Scan Path(s) ction Logs and Reports lame	primary	USERCODE Atternates TRST Devices Hardware	







f. Select the Save button above.







- 3. Connect the ASSET hardware to the XEM6002 board.
- a. Power-up the XEM6002 by connecting the USB cable
- b. Select the SPV1 Run button below.
- c. Confirm the action passed as shown below.

ScanWorks: FFP_XEM6002_Two_Instrument_Example.XEM6002_Two_Instrument	t_Example	- 🗆 X
Project: FFP_XEM6002_Two_Instrument_Examp	le	F RIC-1000 ▼
Design: XEM6002_Two_Instrument_Example		TCK Frequency: 10.000 MHz IP Address: 192.168.1.100 Compatible with Design? Yes
Projects Designs Actions Sequences		Status Notes Mappings Reports Passed
Create 🔻 Manage		*** Starting IR Capture test *** IR Capture test PASSED for TAP 1
Se Action Name	Type	*** Starting BYPASS test *** BYPASS test PASSED
Hardware Setup Message	Display Message	*** Starting IDCODE test ***
Move PMOD Message	Display Message	IDCODE for Device U1 in tap 1 PASSED
SPI_Flash_LongChain_PMOD3_Lower	SPI	Expected data: XXXX0100000000000000000000000000000000
SPI Flash ShortChain PMOD3 Lower	SPI	Measured data, doiobidddddddddddddddddddddddi
SPIFlashIP PMOD1 Lower	SPI Flash IP	
SPV1		*** Starting Boundary Length test ***
	Scan Path Verify	Boundary Length test PASSED for TAP 1.
U1_SVF	SVF	Expected data: XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
Showing 1 to 7 of 7 entries	Previous 1 Next	Measured data: 11111111111111111111111111111111
		Test completed successfully

- 4. Create and run an SVF Action Configure the FPGA at U1 with the SPI Flash IP and GPIO instruments.
 - a. Select the Actions tab.
 - b. Select the Create button.







c. Select the SVF Link

ScanWorks: FFP_XEM6002_Two_Instrument_Example.XEM6002_Two_In	nstrument_Example		- 🗆 ×
Project: FFP_XEM6002_Two_Instrument_E: Design: XEM6002_Two_Instrument_Examp Projects Designs Actions Sequent Create ~ ✓ Manage ✓ Selid ✓	xample le ces	RIC-1000 V TCK Frequency: 10.000 MHz IP Address: 192.168.1.100 Compatible with Design? Yes Status Notes Mappings Running SPV1 Passed	Image: Options Image: Licenses Image: Help Image: Options Image: Options Image: Options Image: Options Image: Options <td< th=""></td<>
Assembly Test Scan Path Verify Interconnect Memory Access Verify Component Discrete I/O Macro CPU IJTAG Instruments IJTAG Instruments (P1687)	Program eMMC Flash I2C NAND Flash PM Configuration SPI DIO SPI DIO SPI Direct SPI Flash IP STAPL SVF 1532 - Adaptive	Utility ASP Display Message Input Text Reset Script	
Showing 1 to 8 of 8 entries	Previous 1 Next		

- d. The Define an SVF Action will open.
- e. Above you can optionally rename the action. U1_SVF
- f. Set the Target drop-down to the device to be programmed. U1
- g. Select the SVF import icon and browse to and select the .svf file in the appropriate ETG ScanWorks folder as shown below.

Define an SVF Action	🖹 Save Cancel
Action Name	Translate with no TDO, Mask, or Compare Build
U1_SVF	Apply Options O Run
Precondition 🕼 Import 🖋 Edit 🗎 Remove	Logging Mode Diagnose
Target Scan Path	Deterministic response data
primary •	Stop on Failure Count
Target	· · · · · · · · · · · · · · · · · · ·
U1 •	Compare Mode
← → · ↑ ■ « FFP_XEM6002_Two_Instrument_Example Organize • New folder	e → XEM6002_Two_Instrument_Example → ETSet → ET_0 → ScanWorks v D P Search ScanWorks
Image: Arrow of the second	Date modified Type Size 5/14/2020 8:36 AM SVF File 1,344 KB
Cibeos	







 $\label{eq:c:ScanWorksProjectsFFP_XEM6002_Two_Instrument_Example\XEM6002_Two_Instrument_Example\ETSet\ET_0\ScanWorks$

- h. Select the Build button.
- i. Select the Save button above.
- $j. \quad Select \ the \ U1_SVF \ Run \ button \ below.$
- k. Confirm the action passed as shown below.

ScanWorks: FFP_XEM6002_Two_Instrument_Example.XEM6002_Two_Instrumen	t_Example		- 🗆 X
Project: FFP_XEM6002_Two_Instrument_Examp	le		로 Options 🔒 Licenses ? Help Ů Exit
Design: XEM6002_Two_Instrument_Example		TCK Frequency: 10.000 MHz IP Address: 192.168.1.100	Updates Available!
		Compatible with Design? Yes	
Projects Designs Actions Sequences		Status Notes Mappings	Reports Passed
Create 👻 🖌 Manage		Project Name: FFP_XEM6002_Two_Instrument_ Project Version: 409	Example
Se	earch:	Design Name: XEM0002_ING_INStrument_Examp Design Version: 346 Action Name: U1_SVF	116
Action Name	🕈 Туре 🔶	Action Version: 97	
Hardware Setup Message	Display Message	Ruil Date: 3/14/2020 11.30.30 An	****
Move PMOD Message	Display Message		
SPI_Flash_LongChain_PMOD3_Lower	SPI	SVF Filename: et_0.svf	
SPI_Flash_ShortChain_PMOD3_Lower	SPI	Seen Engine (Semial Test Bus Controller C	Command Convension)
SPIFlashIP_PMOD1_Lower	SPI Flash IP	Accepts a binary input file consisting of	f Scan Engine commands and associated
SPV1	Scan Path Verify	data and applies it to the target hardwar	re, saving the results in a binary file
U1_SVF		Copyright (c) 1991-2001 Texas Instruments	s, Inc and ASSET Intertech, Inc. All rights re
	SVF	Version: 1.40, Date: Mar 13 2020 SBSF Version 3	
Showing 1 to 8 of 8 entries	Previous 1 Next	***ATTENTION*** The TCK frequency was cha Vector application complete	nged to 1000000 Hz due to FREQUENCY statement
		Run time: 3.383 seconds	

- 5. Create and run an SPI Flash IP Action Program and Verify the SPI Flash device on PMOD1 lower position
 - a. Select the Actions tab.
 - b. Select the Create button.







c. Select the 'SPI Flash IP' link.

Projects Designs Ac Create Manage C I Assembly Test Scan Path Verify Interconnect Memory Access Verify Component Discrete I/O Macro CPU UTAG Instruments UTAG Instruments (P164) Define an SPI Provide a Nar Select the targe Name SPIFlash IP Name SPIFlash	etions Sequences Build Program eMMC Flash ICC NAND Fla PM Confit SPI SPI Direct SPI Flash STAPL SVF 1532 - Ad ISS2 - Ad IS32 - Ad ISS2 - Ad IS32 -	m ash iguration t P daptive on window on. e programm	Status Notes Running U1_SVF Passed Utility ASP Display Messa Input Text Reset Script V opens SPIF1as med. (PM	shIP_P OD1)	Reports MOD	Weber Meeting Reminder H SED Status Host: Hany Myess Snooze v Jo LOWER
Create	Build Program eMMC Flash I2C NAND Fla PM Confi SPI Direct SPI DIRECT	m ash iguration daptive on window on. e programm	v opens SPIF1as med. (PM	^{age} shIP_P OD1)	MOD	Webex Meeting Reminder B SED Status 1200 PM - 1220 PM Host: Harry Myers Income v ke
Assembly Test Scan Path Verify Interconnect Memory Access Verify Component Discrete I/O Macro CPU UTAG Instruments UTAG Instruments UTAG Instruments (P164 Define an SPI Provide a Nar Select the targ	87) Program eMMC Flash I2C NAND Flash SPI Direct SPI DI	m ash iguration daptive on window on. e programm	Utility ASP Display Messa Input Text Reset Script	shIP_P OD1)	MOD	Weber Meeting Reminder H SED Status 12:00 PM - 12:20 PM Hott: Harry Myers Sneoze v # 1_LOWER
Define an SPI Provide a Nan Select the targ Works FFP_XEMG002_Two_Instrument_Ear Define an SPI Flash IP Name SPIFlashI	I Flash IP Action ne for the Action get device to be	on window on. e programr	v opens SPIFlas med. (PM	shIP_P OD1)	MOD	Weber Mesting Reminder SED Status 12:00 PM - 12:30 PM Host: Harry Myers Income v in
Works: FFP_XEM6002_Two_Instrument_Ear Define an SPI Flash IP Name SPIFlashI	mple XEM6002_Two_Instrument_Example			OD1)		
Name SPIFlashi	Action					- C Save Cancel @ Hel
	IP_PMOD1_Lower	Source File	les f	Import % Imp	oort Link	Build
Precondition Import	🖋 Edit) 🖀 Remove	2MB.bin	© 0x0			O Run
Target Device						
Model D2: LED_SI D3: LED_SI D4: LED_SI	SMD_0603					
Model Override D5: LED_SI D6: LED_SI D6: LED_SI D7: LED_SI	SMD_0603 SMD_0603 SMD_0603					
Device Access JP4: CONN	SMD_0603					
Farget Scan Paths	PMOD +					
Operations Model Cross-R			Logs & Dt-			
	Reference ScanWorks Model Libr	erary Flash Report	Logs & Reports			
Check manufacturer ID	Reference ScanWorks Model Libr	rary Flash Report	nstrument Map		0	Webex Meeting Reminder

g. The Model should default to the PMOD16_lower.cmp.







Name	SPIElaship PMOD	1 Lower	Source Files	Import & Import Link	Build
Ivanie		Configure access to SPI device(s)			build
Precondition	🖡 Import	SPI Device Pins Show All Pins v Close Browser <<	SPI Device(s) PMOD1	Instrument Instance	O Run
Target Device	PMOD1: PMOD	Type Pin Node Name Pins	Chain Length: 421 Device Instruction		
	Reference Designato	J ² SDO 9 PMOD1_9 U1-F1 J ² CLK 10 PMOD1_10 U1-G1 J ² CE 7 PMOD1_7	U1 USER		
Model	PMOD16_lower.cmp				
	PMOD16_lower.cmp				
Model Override	Use Action Cross-	Select Set HI Set LO D	elete	OK Cancel	
	Override design cros	Show Find in list FPGA Devices	→ Find	Device Information Reference Designator	
Device Access	¢° Configure	Devices Pins U1-E1 U1-E2 U1-F1	Cell Information Read Write	Entty Name	
arget Scan Paths	✓ primary	U1-G1 U1-M2 U1-N1 U1-N1 U1-P1 U1-T8	OE OE Polarity Related Enable Cells	Device Type	
	Nodel Cross-Reference				
Operations N					

h. Select the Device Access Configure

i. In the Configure access to SPI device(s) dialog select the Instrument Instance SPIFlashPlayer_PMOD1_Lower







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	SPI Device(s)	Instrument Instance
Close Browser <<	PMOD1	SPIFlashPlayer_PMOD1_Lowe ~
e Pins U1-E2 U1-F1 U1-G1	Chain Length: 421 Device Instruction U1 USER	ShortChain_SPIFlash_PMOD3_Lov SPIFlashPlayer_PMOD1_Lower
Set LO Delete	· Find	OK Cancel Device Information Reference Designator
Pins U1-E1 U1-E2 U1-F1 U1-G1 U1-M1 U1-M2 U1-M1 U1-P1 U1-T8	Cell Information Read Write OE OE Polarity Related Enable Cells	Entity Name Device Type
	Close Browser << e Pins U1-E2 U1-F1 0 U1-G1 Find in list Pins U1-E1 U1-E2 U1-F1 U1-E2 U1-F1 U1-G1 U1-F1 U1-G1 U1-P1	Close Browser < SPI Device(s) PINS PM0D1 U1-E2 Device U1-F1 Device 0 U1-G1 Set LO Delete Find in list Find Pins Cell Information U1-E1 U1-E1 U1-F1 Cell Information U1-E1 Read U1-F1 OE U1-F1 OE U1-F1 U1-P1 U1-P1 Related Enable Cells

- j. Select the OK button. This will close the dialog.k. In the Operations tab under Instrument Map select import

Name	SPIFlashIP_PMOD1_Lower	Source Files	€ Import Solution	Build	
Precondition	↓ Import ▲ Edit □ Remove □	2MB.bin 🕸 0x0	圃	O Run	
Target Device	PMOD1: PMOD				
Model	PMOD16_lower.cmp PMOD16_lower.cmp				
Model Override	Use Action Cross-Reference Override design cross-reference				
Device Access	₽ ^o Configure				
Target Scan Paths	✓ primary				
Operations M	lodel Cross-Reference ScanWorks Model Library	y Flash Report Logs & Rep	ports		
Check manufactu Alternate IDs	irer ID	Instrument Ma	ap View 🗟 Remove		
e.g. 0xAA, 0	xFA	HPGA			

1. With the import browser open, browse to and double-click on the .ffpmap the instrument map. ET 0.ffpmap

C:\ScanWorks\Projects\FFP_XEM6002_Two_Instrument_Example\XEM6002_Two_Instrument_Example\ETSet\ET_0\ScanWorks\ET_0.ffpmap in this case

ScanWorks: FFP_XEM6002_T	wo_Instrument_Example.XEM600	12_Two_Instrument_Example				Save Cancel	🕑 Help
Name	SPIFlashIP_PMOD	1_Lower	Source Files	f Import	% Import Link	Build	
Precondition	🖌 Import 🕜 Edit 🥤	i Remove	2MB.bin \$\$ 0x0		Ē	O Run	
Frecondition							Л
Target Device	← → · ↑ I « FFP_;	XEM6002_Two_Instrument_Example >	XEM6002_Two_Instrument_Example > ETS	et > ET_0 > ScanWorks	v ق	✓ Search ScanWorks	
	Organize * New folder					i · 🔳 🔞	
Model	★ Quick access ♦ ASSET InterTech D	Name	Date modified 5/14/2020 8:18 AM	Type FFPMAP File	Size 3 KB		
Model Override	 This PC 3D Objects Desktop Documents 						
Device Access	 Downloads Music Pictures Videos 						
Target Scan Paths	🐛 Windows (C:)						
Operations N	File nam	e:			~	Mapping File (*.ffpmap) ~ Open V Cancel	
Check manufactu	urer ID		Instrument	Map ⊛ View			
e.g. 0xAA, 0	IxFA		FPGA				

- m. Select the Open button to acknowledge that the Import is complete.
- n. Next in the Operations Tab
 - a. Select the manufacture ID
 - b. Select the deivce ID
 - c. Select Blank check
 - i. Check all sectors
 - ii. Erase on blank check failure
 - d. Select Program





Model Cross-Reference	ScanWorks Model Library	ash Report Logs & Reports	
neck manufacturer ID Alternate IDs		Instrument Map	
e.g. 0xAA, 0xFA		FPGA	
neck device ID Alternate IDs		U1	¥
e.g. 0xAA, 0xAAFF		SCL Divisor	
example: 0xBBFF - FF is DEV_ID and	BB is for DEV_ID2	1	
ank check		(1-256)	
Check all sectors			
Check image area only			
Erase on blank check failure			
ogram			
ecure			
erify			

- o. Select the blue Import icon next to "Source Files".
- p. Browse to and double-click on the provided file named 2MB.bin.
- q. Select OK to confirm the file as a Binary file.

efine an SPI	Flash IP Action			Save Cancel @ He
Name	SPIFlashIP_PMOD1_Lower	Source Files	f Import Share Sha	Build
Precondition	📕 Import 🖉 Edit 📄 Remove	2MB.bin 🔅 0x0	Đ	O Run
Target Device	PMOD1: PMOD			
Model	PMOD16_lower.cmp			

- r. Select the Build button.
- s. Select Yes to confirm the action name change.
- t. Select the Save button.

Opal Kelly FrontPanel Settings

If you have closed the Opal Kelly FrontPanel, restart the application.









Select the tools icon and the following interface will open. Note that for this SPI Flash IP example, when using the Opal Kelly board, it needs to be set as follows, using the FrontPanel software, for the SPI Flash IP to Pass. Decrementing the Divider #1, DIV1N:, to less than 7, will increase the related frequency and cause a failure.

Return to ScanWorks

- u. Select the SPIFlashIP_PMOD1_Lower Run button below.
- v. Confirm the action passed as shown below.

SamWorks: FFP_XEM6002_Two_Instrument_Example.XEM6002_Two_Instrument Project: FFP_XEM6002_Two_Instrument_Example Design: XEM6002_Two_Instrument_Example Project: Decigns Actions Sequences	t,Example le	KIC-1000 ▼ TCK Frequency: 10.000 MHz IP Address: 192.168.1.100 Compatible with Design? NA Status Notas Mappings Reports Passed Passed Pass
Create - Manage Of Build	ırch:	Action Name: SPIFlashIP_PMOD1_Lower Action Version: 50 Run Date: 5/19/2020 3:26:17 PM
Action Name	🕈 Type 🕴	Image File: 2MB.bin
Hardware Setup Message	Display Message	*** Manufacture ID matches ***
Move PMOD Message	Display Message	Found: 0x20, Expected: 0x20 , Mask: 0xFF
SPI_Flash_LongChain_PMOD3_Lower	SPI	Found: 0x20, Expected: 0x20 , Mask: 0xFF
SPI_Flash_ShortChain_PMOD3_Lower	SPI	*** Unsecuring all sectors of the device ***
SPIFlashIP_PMOD1_Lower		Unsecure operation was successful
<i>d</i> ² Edit ^C Edit	SPI Flash IP	*** Blank Check Operation Started *** Blank Check operation failed *** Erase Operation Started *** Erase Mode: All Sectors
SPV1	Scan Path Verify	Erase operation Completed *** Blank Check Operation Started ***
U1_SVF	SVF	Blank Check operation was successful
Showing 1 to 7 of 7 entries	Previous 1 Next	*** Programming Operation Started *** Programming operation Completed *** Verify Operation Started *** Verify operation passed
		OK Cancel

- 6. Create and run a standard Boundary Scan SPI Flash Action Using the default boundary register and PMOD3 lower position
 - a. Power off the target
 - b. Physically move the SPI Flash PMOD from PMOD1 to PMOD3.
 - c. Select the Actions tab.
 - d. Select the Create button.
 - e. Select the 'SPI' link.







SCANWORKS FPGA-BASED FLASH PROGRAMMING A TWO INSTRUMENT EXAMPLE GUIDE

sign: XEM6002_Two_Instrument_Exar	mple	TCK Frequency: 10.000 MH: IP Address: 192.168.1.100 Compatible with Design?	NA D	Updates Availab	ole!
Projects Designs Actions Sequ	uences	Status Notes Ma	appings Repo	orts	•
eate 👻 🖋 Manage 🕼 Build		SPI_Flash_LongChain_I	PMOD3_Lower	Action Log	s and Reports
				, Mapping	Hardware
Assembly lest	Program	Utility	020 2:51:32 PM	n/a	n/a
Scan Path Verify	eMMC	ASP	020 8:58:38 AM	Default	RIC-1000
Interconnect Memory Access Verify	Flash I2C	Display Message	020 8:58:38 AM	Default	RIC-1000
Component	NAND Flash	Reset	017 4:28:52 PM	n/a	n/a
Discrete I/O	PFP DNA Conferenction	Script			
CPU	SPI				
IJTAG Instruments	SPI DIO				
IJTAG Instruments (P1687)	SPI Direct		* * * * * * * * * * * * * * * *	***********	*****
PFT DDR	STAPL		nstrument_Examp	le	
	1532 - Adaptive		ment_Example		
owing 1 to 7 of 7 entries	Previous 1 Next	Action Version: 27	n_PMOD3_Lower		
3		Run Date: 5/19/2020 2:51:30	PM		
		*****	**************	***********	*****

- f. Enter Name SPI_Flash_LongChain_PMOD3_Lower
- g. Select PMOD3 below as the device to program.
- h. The Model should default to PMOD16_lower.cmp

Name	SPI_Flash_LongChain_PMOD3_L	Source Files Source Files	Build
Precondition	F Import S Edit	· 復日	Run
Target Device	Select a device		
Model	D4: LED_SMD_0603	×	
Model Override	D7: LED_SMD_0603 D8: LED_SMD_0603 JP4: CONN_PLUG_7X2		
Device Access	PMOD1: PMOD PMOD2: PMOD		
arget Scan Paths	PMOD3: PMOD PMOD4: PMOD		
Operations W	rite to File Model Cross-Reference	ScanWorks Model Library Flash Report Logs & Reports	

- i. Device Access
 - a. Select the Configure button.
 - b. Ensure the Boundary Scan Master is U1
- j. Select the OK button.







k. Select the two ID Checks, Erase, Blank check, Program, and Verify boxes.

Operations	Write to File	Model Cross-Reference	ScanWorks Model Library	Flash Report	Logs & Report
Check Manufa Alternate II e.g. 0xAA	cturer ID Ds , 0xFA ID Ds			Report 1 (1 - 256) Write Range to Start Address	Errors o File
e.g. 0xAA example: 0x	, 0xAAFF xBBFF - FF is DE	V_ID and BB is for DEV_ID2		0x00000018 End Address	
 Erase All Sectors Used Secto 	ors			0x532F3A43	
Blank Check In	nage Area				
Program Secure					
Verify					

- 1. Select the blue Import icon next to "Source Files".
- m. Browse to and double-click on the provided file named 2MB.bin.
- n. Select Open to confirm the file as a Binary file.
- o. Select the Build button.
- p. Select the Save button.
- q. Select the SPI Flash LongChain PMOD3 Lower Run button below.
- r. Confirm the action passed as shown below.

Project: FFP_XEM6002_Two_Instrument_Example	onks:HP_XEMb002_two_instrument_Example.XEMb002_two_instrument_Example	
Design: XEM6002_Two_Instrument_Example Projects Designs Actions Sequences Projects Designs Actions Sequences Status Notes Mappings Reports Status Notes Mappings Reports Search: Action Name Type Hardware Setup Message Display Message <th>ret: FFP_XEM6002_Two_Instrument_Example FIC-1000 - 로 Opt</th> <th>ions 🔓 Licenses 🛛 ? Help 🖞 Exi</th>	ret: FFP_XEM6002_Two_Instrument_Example FIC-1000 - 로 Opt	ions 🔓 Licenses 🛛 ? Help 🖞 Exi
Projects Designs Actions Sequences Projects Designs Actions Sequences Create C Manage C Build Create C Manage C Build Action Name Type Display Message Display Message Disp	gn: XEM6002_Two_Instrument_Example TCK Frequency: 10.000 MHz 🗅 Upda	ates Available!
Action Name Type Action Name Type Action Name Type Action Name Type Bland KongChain_PMOD3_Lower Display Message Display Message Display Message Status Note: Unit Optical Expected: 0x20 Device ID Passed SPIF Flash, ShortChain_PMOD3_Lower SPI SPI Flash IP Sinth Che	IP Address: 192.168.1.100	
Projects Designs Actions Sequences Status Notes Mappings Reports Park Create * * Manage @ Build Search: Action Name * Type Display Message Display	Compatible with Design? Yes	
Create Manage Q\$ Build BIN 0xd Search: Other Information *** No precondition file present **** Action Name Type D Hardware Setup Message Display Message D SPL Flash LongChain_PMOD3_Lower Display Message P Blid Cropy Reports Store Phash SPI S Build >	pjects Designs Actions Sequences Status Notes Mappings Reports	Passed
Create Manage Operations: Passed Action Name Type D Hardware Setup Message Display Message Operations: Passed D Move PMOD Message Display Message Display Message Display Message D SPL_Flash_LongChain_PMOD3_Lower SPI Passed Actual: 0x20 E dit Copy Imanufacturer Passed Actual: 0x20 SPL_Flash_LongChain_PMOD3_Lower SPI SPI Passed Actual: 0x20 S SPL_Flash_ShortChain_PMOD3_Lower SPI SPI SPI Passed Mode: used D SPV1 Scan Path Verify Scan Path Verify Scan Path Verify Passed Mode: used D In SVF SVF SVF Passed Fassed Passed) ^
Action Name Type D Hardware Setup Message Display Message D Move PMOD Message Display Message SPL_Flash_LongChain_PMOD3_Lower Passed Edit COpy Build Rename SPL_Flash_ShortChain_PMOD3_Lower SPI SPL_Flash_ShortChain_PMOD3_Lower SPI SPLFlash_ShortChain_PMOD3_Lower SPI SPLFlash_ShortChain_PMOD3_Lower SPI SPIFIash_ShortChain_PMOD3_Lower SPI SPIFIash_ShortChain_PMOD3_Lower SPI SPIFIash_ShortChain_PMOD3_Lower SPI SPIFIash_ShortChain_PMOD3_Lower SPI SPIFIash/PMOD1_Lower SPI SPIV1 Scan Path Verify Un_SVF SVF	Other Information	
Action Name Type D Hardware Setup Message Display Message D Move PMOD Message Display Message D Move PMOD Message Display Message D SPL Flash_LongChain_PMOD3_Lower Passed E dit C) Copy E Reports SPI S Build >. Rename D Delete X Alternate Paths S Di Flash.IshortChain_PMOD3_Lower SPI S SPI Flash.IshortChain_PMOD3_Lower SPI S SPIFlash.IshortChain_PMOD3_Lower SPI S SPIFlash.IshortChain_PMOD3_Lower SPI S SPIFlash.IP SPI S SPI T Scan Path Verify S If VI_SVF SVF	Search:	
Action Name Type D Hardware Setup Message Display Message D Move PMOD Message Display Message D SPL_Flash_LongChain_PMOD3_Lower SPI E dit C Copy Reports SPL SPI S Build > Rename Requirements S PL_Flash_Long Chain_PMOD3_Lower SPI > SPL SPI S Build > Rename SPI S SPL Flash_ShortChain_PMOD3_Lower SPI S SPIFlash.IP_PMOD3_Lower SPI S SPIFlash.IP_PMOD3_Lower SPI S SPIFlash.IP_PMOD3_Lower SPI S SPIFlash.IP_PMOD3_Lower SPI S SPI To Scan Path Verify Scan Path Verify S U 1_SVF SVF	Operations: pour	
Display Message Display Message Move PMOD Message Display Message Move PMOD Message Display Message SPL_Flash_LongChain_PMOD3_Lower Display Message & Edit C) Copy Image: Reports & Bditl C) Delete X Actual: & Delete X Alternate Paths > SPL_Flash_ShortChain_PMOD3_Lower SPI > SPI-Flash.ShortChain_PMOD3_Lower SPI > SPI-Flash.ShortChain_PMOD3_Lower SPI > SPI-Top Scan Path Verify > SPV1 Scan Path Verify > Un_SVF SVF	tion Name Type	
Display Message Display Message Display Message Display Message SPI_Flash_LongChain_PMOD3_Lower Device ID Passed Actual: 0x20 SPI Device ID Passed Actual: 0x20 Device ID Device ID Passed Mctual: 0x20 SPI Device ID Passed Mctual: 0x20 SPI Device ID Passed Mctual: 0x20 SPIFlash.ShortChain_PMOD3_Lower SPI Passed Mode: used SPIFlashIP_PMOD1_Lower SPI Flash IP Blank Check Passed Un_SVF SVF Blank Check Passed	ardware Setup Message Display Message Manufacturer Passed Actua	al: 0x20
SPI_Flash_LongChain_PMOD3_Lower Perice ID Passed Actual: 0x20 Edit Cp Copy Reports SPI Spi Plash_ShortChain_PMOD3_Lower SPI SPI_Flash.ShortChain_PMOD3_Lower SPI SPIFlash.PMOD1_Lower SPI SPIFlash.PMOD1_Lower SPI SPI SPIFlash.PPMOD1_Lower SPI SVI Scan Path Verify SVI SvF	ove PMOD Message Display Message ID Expect	ted: 0x20
Edit Copy Parente Edit Copy Reports SPI SPI Locy	Pl_Flash_LongChain_PMOD3_Lower	1. 0.20
^{CS} Build S. Rename Requirements ^{SPI} ^{SPI} ^{CS} Build S. Rename Requirements ^{SPI}	it Copy III Reports	ted: 0x20
VInsecure Passed D SPU_Flash_ShortChain_PMOD3_Lower SPI S SPI Flash IP_PMOD1_Lower SPI Flash IP D SPV1 Scan Path Verify D LIJ_SVF SVF	uild >_ Rename Requirements SPI	
D SPL Flash_ShortChain_PMOD3_Lower SPL D SPL Flash IP PMOD1_Lower SPL Flash IP D SPV1 Scan Path Verify D U1_SVF SVF	op Vi Debug Unsecure Passed	
D SPIFlashIP_PMOD1_Lower SPI Flash IP Erase Passed Mode: used D SPV1 Scan Path Verify Blank Check Passed Mode: used	PI_Flash_ShortChain_PMOD3_Lower SPI	
D SPV1 Scan Path Verify D U1_SVF SVF	PIFlashIP_PMOD1_Lower SPI Flash IP Passed Mode	e: used
DU1_SVF SVF Time: 9.716667	PV1 Scan Path Verify Blank Check Passed	
Brogram Barrad Time: 9.746667	1_SVF SVF	
Showing 1 to 7 of 7 entries Previous 1 Next Program Provide Automatic Action Previous 1 Next Program Provide Action Previous Prev	ving 1 to 7 of 7 entries Previous 1 Next Program Passed Time:	8.716667
Verify Passed	Verify Passed	







Create and run a standard Boundary Scan SPI Flash Action – Using the ETG short chain feature and PMOD3 lower position

- a. Select the Actions tab.
- b. Select the Create button.
- c. Select the 'SPI' link.

ScanWorks: FFP_XEM6002_Two_Instrument_Example.XEM6002_Two_Instru	ument_Example				>
Project: FFP_XEM6002_Two_Instrument_Exa Design: XEM6002_Two_Instrument_Example Projects Designs Actions Sequence	s	RIC-1000 TCK Frequency: 10.000 MHz IP Address: 192.168.1.100 Compatible with Design? Status Notes Mathematical Set Legachains Status Notes	NA ppings Repo	Options L L Updates Availab	censes) ? Help 😃 Exit
Create Manage Assembly Test	Program			Mapping	Hardware
Assembly rest	riogram	Othity	020 2:51:32 PM	n/a	n/a
Scan Path Verify	eMMC Flack	ASP Display Massage	020 8:58:38 AM	Default	RIC-1000
Memory Access Verify	I2C	Input Text	020 8:58:38 AM	Default	RIC-1000
Component	NAND Flash	Reset	017 4:28:52 PM	n/a	n/a
Discrete I/O Macro CPU UTAG Instruments UTAG Instruments (P1687) PFT PFT DDR	PFP PM Configuration SPI SPI DIO SPI Direct SPI Flash IP STAPL SVF 1532 - Adaptive Previous 1 Next	Script	nstrument_Examp ment_Example n_PMOD3_Lower	le	
		Run Date: 5/19/2020 2:51:30 P	M	****	

d. Enter Name SPI_Flash_ShortChain_PMOD3_Lower







e. Select PMOD3 above as the device to program.

ScanWorks: FFP_XEM6002_Two	o_Instrument_Example.XEM6002_Two_Instrument_Example.	le	- 🗆 X
Define an SPI	Action		🖺 Save Cancel
Name	SPI_Flash_ShortChain_PMOD3_I	Source Files	Build
Precondition	Fimport Edit Remove		● Run
Target Device	Select a device		
Model	D4: LED_SMD_0603	v	
Model Override	D7: LED_SMD_0603 D8: LED_SMD_0603 JP4: CONN_PLUG_7X2		
Device Access	PMOD1: PMOD PMOD2: PMOD		
Target Scan Paths	PMOD3: PMOD PMOD4: PMOD		
Operations W	rite to File Model Cross-Reference	ScanWorks Model Library Flash Report Logs & Reports	
Check Manufactur Alternate IDs e.g. 0xAA, 0x	rer ID FA	Report Errors 1 Errors (1 - 256) Errors	
Check Device ID		Write Range to File	-

- f. The Model should default to PMOD16 lower.cmp
- g. Device Access
 - a. Select the Configure button.
 - b. Ensure the Boundary Scan Master is U1
- h. Select the OK button.
- i. Select the two ID Checks, Erase, Blank check, Program, and Verify boxes.

Operations	Write to File	Model Cross-Reference	ScanWorks Model Library	Flash Repo	ort Logs & Rep	orts	
Check Manur Alternate	facturer ID IDs A, 0xFA			Report 1 (1 - 256)	Errors		
Check Device	e ID			Write Range	ge to File		
Alternate	IDs			Start Add	ress		
e.g. 0xA	A, 0xAAFF			0x00000	000		
example:	0xBBFF - FF is DE	V_ID and BB is for DEV_ID2		End Addre	255		
Elase				0x00000	000		
 All Sector Used Sector 	s tors						
Blank Check	Image Area						
🗹 Program							
Secure							
Verify							

- j. Select the blue Import icon next to "Source Files".
- k. Browse to and double-click on the provided file named 2MB.bin.
- 1. Select OK to confirm the file as a Binary file.







- m. Select the OK button.
- n. Select the Build button.
- o. Select the Save button.
- q. Single-click on the 'SPI_Flash_ShortChain_PMOD3_Lower' link below.

ScanWorks: FCT_FFP_XEM6002_Four_Instrument_Example.XEM6002_Four_Instrument_Example							
Project: FCT_FFP_XEM6002_Four_Instrument_Example Design: XEM6002_Four_Instrument_Example Projects Designs Actions Sequences	ct: FCT_FFP_XEM6002_Four_Instrument_Example m: XEM6002_Four_Instrument_Example TCK Frequency: 10.000 MHz IP Address: 192.168.12.1 Compatible with Design? Yes cts Designs Actions Sequences Status Notes Mappings Reports SPI_Flash ShortChain_PM003_Lower Action Logs and Reports						
- Constan & Manager M ² Build							
Search: Find Actions		Name 🔺	Date 🔻	Mapping 🝦	Hardware 🔶		
Action Name	🔺 Type 🍦	Build Log 🛛	10/19/2017 4:04:38 PM	n/a	n/a		
Run Frequency_Measure_U1_T8	IJTAG Instruments	Source File Validation Log	10/19/2017 4:04:06 PM	n/a	n/a		
	(P1687)	1687) Showing 1 to 2 of 2 entries					
Run SPI_Flash_LongChain_PMOD3_Lower	SPI	Save As Print					
Rom SPL_Hasp_shortChain_PMOUs_Lower /Edit (2) Copy IBIR exports % Boild >_Rename IR Requirements > Run Ø Delete X Alternate Paths (3) Loop (9) Debug	SPI	Project Name: FCT_FFP_XBr6882_Four_Instrument_Brample					
Run SPIFlashIP_PMOD1_Lower	SPI Flash IP	sh IP Design Name: XEY0802_Four_Instrument_Example					
Run SPV1	Scan Path Verify	h Design Version: 49 Action Name: SPI_Flash_ShortChain_PYD03_Lower					
Run Temperature_Measure_PMOD2_Lower	UTAG Instruments (P1687)	Action Version: 5 Run Dæte: 18/23/2017 4:04:36 PM					
Run U1_SVF	SVF	No precondition present ADS2NDD2 - The ASSET Nodelist Generator					

- r. Select the 'SPI_Flash_ShortChain_PMOD3_Lower' Build button above.
- s. Select the SPI_Flash_ShortChain_PMOD3_Lower Run button below.







t. Confirm the action passed as shown below.

Projects Designs Actions Sequences		TCK Frequency: 10.0 IP Address: 192.168.	000 MHz	Updates Available!	es ? Help O Ex
Projects Designs Actions Sequences		Compatible with De	sign? Yes		
		Status Notes	Mappings	Reports	Passed
Create 👻 🗲 Manage 🕰 Build		2MB.bin Other Information	Bl	N 0x0	^
Search	·	Operation	S: Passed		
Action Name	Display Message	Manufacturer	Passed	Actual: 0x20	
Move PMOD Message	Display Message	ID		Expected: 0x20	
SPI Flash LongChain PMOD3 Lower	SPI				
SPI_Flash_ShortChain_PMOD3_Lower		Device ID	Passed	Actual: 0x20 Expected: 0x20	
P Edit (2) Copy im Reports % Build >_ Rename ➡ Requirements ▶ Run ③ Delete X ² Alternate Paths	SPI	Unsecure	Passed		
SPIFlashIP PMOD1 Lower	SPI Flash IP	Erase	Passed	Mode: used	
SPV1	Scan Path Verify	Blank Check	Passed		
U1_SVF	SVF	Diank Check	105500		
Showing 1 to 7 of 7 entries	Previous 1 Next	Program	Passed	Time: 0.600000	
		Verify	Passed		

7. Export the Project

The project should be exported for archiving purposes.

- a. Select /Project/Export/
- b. FFP_XEM6002_Two_Instrument_Example
- c. Browse to desired folder to save the export.
- d. Select Development/Archive (full)
- e. Select the next
- f. Select Export button

Note: that the example project also contains a sequence and other actions, but this documentation does not cover the generation of the other actions. For more information to export ScanWork and the Embedded Test capabilites refer to the Appendix.







APPENDIX

1. Other ETG Example Projects

Other ETG Example projects can be found at C:\ScanWorks\ETG\Examples folder. These example projects are provided as examples of what is possible with ScanWorks FPGA Contolled Test (FCT) and ScanWorks Fast Flash Programming (FFP) tools. Within the folder are example instrument projects that are based upon the type of license they use either FCT or FFP.

The structure of the project file name is as follows: <Tool License Type>_<Hardware Target Platform or device>_<Number of embedded instruments>.zip.

The ETG projects support the Opal Kelly XEM6002 board but, this board is not needed for the SVF generation by ETG. The ScanWorks projects are based on the Opal Kelly XEM6002 board and provide for the flashing of the device(s). Some target an SPI Flash PMOD and some target a temperature controller PMOD which are additional hardware connected to the PMOD interface of the board.

File	Comment			
FFP_XEM6002_Two_Instrument_Example.zip	ScanWorks project with FFP			
	instruments			
FCT_XEM6002_Two_Instrument_Example.zip	ScanWorks project with FCT			
	instruments			

2. To Import ETG example project

a. With ScanWorks open







b. Select the Project tab and Select Import

ort a Project						O Help	G
Select the Import File	2. Specify Name 3. Impo	rt					
Import File		Browse					
5	Select a compressed ScanWorks Project						
S Open						×	
\leftarrow \rightarrow \checkmark \uparrow] \rightarrow This	PC > Windows (C) > ScanWorks > ETG > Examples			v ت	P Search Exa	amples	
Organize • New folder	r				1	- I 🕜	
Outle scores ASSET InterTech D Tech D To action Deschop Deschop	Name TG (T)	Date modified 5/18/2020 8:32 PM 2/1/2019 13:33 PM 5/18/2020 8:32 PM 5/18/2020 8:32 PM 5/18/2020 8:32 PM 5/18/2020 8:32 PM 5/18/2020 8:32 PM 5/18/2020 8:32 PM	Type zip Archive zip Archive zip Archive zip Archive zip Archive zip Archive zip Archive zip Archive zip Archive	Size 4.599 K8 4.599 K8 10.935 K8 3.601 K8 8.477 K8 8.510 K8 7.850 K8 7.736 K8			
File nan	ne:				ScanWorks Proje	sct (*.zip) ~ Cancel	

- c. Select Browse and browse to /ScanWorks/ETG/Examples
- d. Select the project of interest and explore the project, design, and actions.





