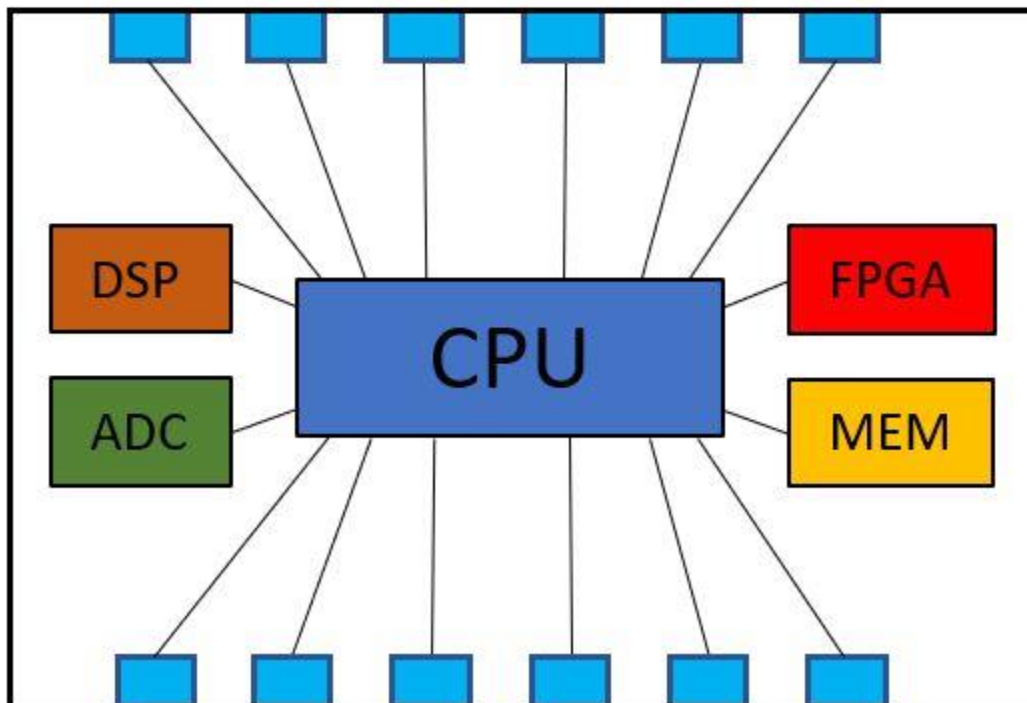
# Chiplet Interconnect Testing Using JTAG/Boundary Scan

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## Executive Summary

Chiplet-based multi-die devices, as products of a heterogenous integration design methodology, play an important role in today's chip design and implementation strategies. The drive to implement multi-die devices began in the 1970's with a packaging innovation approach consisting of placing multiple interconnected chips on a package-scale substrate. These devices became known as multi-chip modules (MCMs). Over time, additional packaging innovations emerged such as System in a Package (SiP), System on Integrated Chip (SoIC)™, 2.5D-Integrated Circuits (ICs) and 3D-IC packages. Multi-die packaging innovations has allowed the semiconductor industry to create smaller, faster, configurable, and lower power ICs.

Image courtesy of Cadence

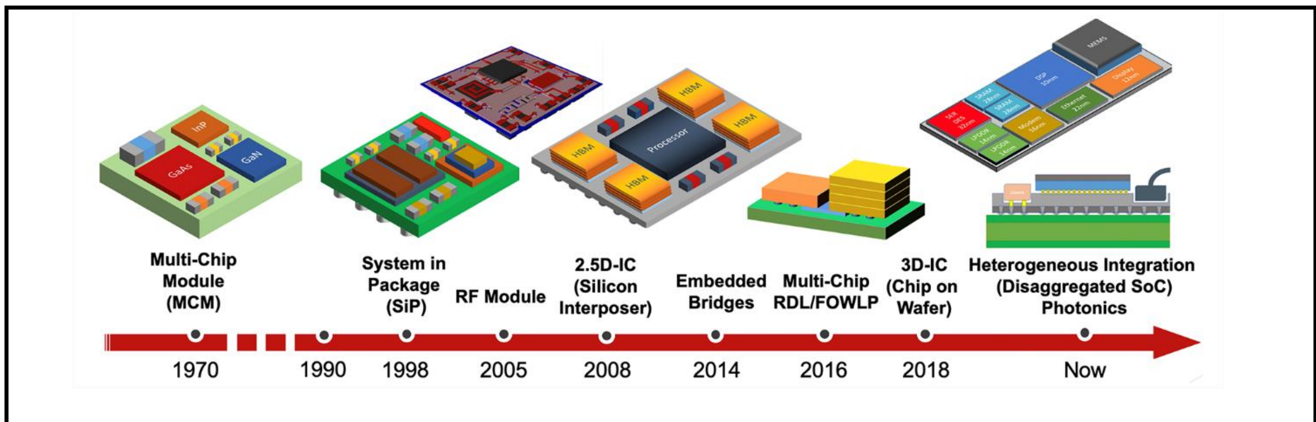



**Figure 1: Timeline of advanced packaging technologies**

Similar to packaged chips placed on a printed circuit board (PCB), interconnects between chiplets within multi-die packages must undergo testing for structural integrity. Structural testing is normally conducted during the manufacturing process on chip-level automated test equipment (ATE) before device shipment to the end user. Chiplet die-to-die (D2D) structural testing involves the application of digital test vectors that are formatted for use on chip-level ATE. These digital test vectors may be a product of the electronic design automation (EDA) tool used to design the chiplets. The test vectors are applied by embedded instrumentation using the input/output (IO) resources of the chiplets. This eBook will examine industry trends that have led to development of heterogenous integration designs in the semiconductor industry and D2D interconnect testing methodologies.

## Chiplet-based Multi-die Devices

As the semiconductor industry continues to move toward creating more efficient and less expensive chip fabrication and design methodologies, an innovative packaging trend has emerged that was originally proposed during the 1960's. This method proposed the packaging of multiple-die devices within a single chip package, a design method known as heterogenous integration.

Heterogenous integration involves the combination of diverse and separate elements, into a functional system. As applied to this use case, the diverse elements are silicon chips (herein referred to as chiplets); and when combined on an interposer or silicon substrate, constitute a structured functioning system. A chiplet is an integrated circuit block that has been specifically designed to work with other chiplets to form larger and more complex chips. Chiplets within multi-die devices can be selected, arranged, and assembled based on the desired chip functionality.

Heterogeneous integration allows for packaging chiplets with different functionalities, different process technologies, and sometimes, from different chiplet manufacturers. The combined chiplets can vary in functionality (e.g., processors, signal processors, cache, sensors, photonics, RF, and MEMS) and technologies (e.g., one optimized for die size with another one optimized for low power).[1] These assembled, diverse silicon chiplets can be packaged in a variety of options.

Monolithic dies are difficult to scale past a certain size and manufacturing large chips that contain more functions is more expensive. Taking these facts into account, the semiconductor industry needed a method to scale products to increase performance, deliver high silicon yields while lowering prices.

As an example of the progression of advanced packaging, AMD's 1st generation EPYC processor migrated from a monolithic design, to an MCM utilizing four interconnected 8-core processors.

Image courtesy of OC3D.net

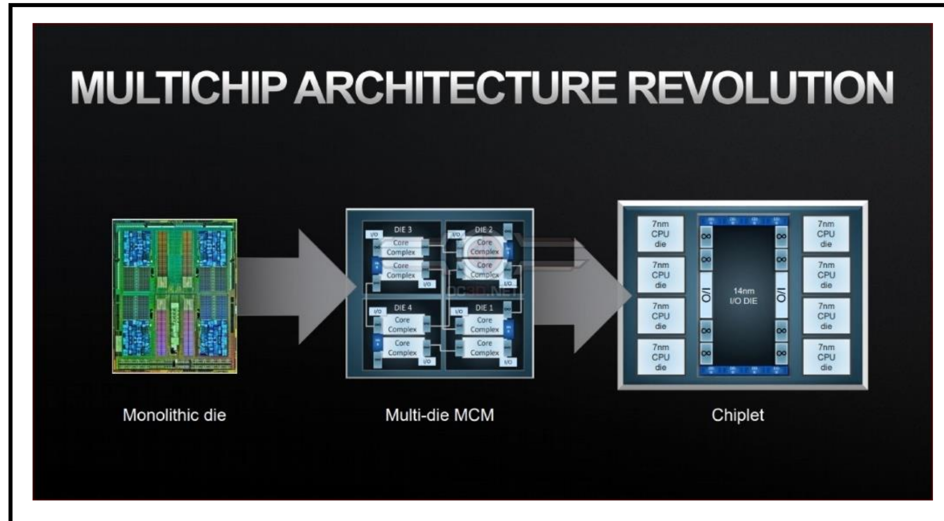



**Figure 2: Monolithic die to chiplet-based device architecture**

Moving forward, AMD designed chiplets to handle specific processor tasks. AMD's 2nd generation EPYC and 3rd generation Ryzen processor offered increased scaling and allowed each piece of silicon to be optimized to deliver the best latency and power characteristics using small 7nm and 14nm chiplets. Advanced packaging innovations has produced:

- Smaller package
- Lower power devices
- Greater chip configurability
- Faster chip time-to-market
- Reduced overall manufacturing cost

## Moore's Law — Extended

As mentioned, heterogenous integration is a design methodology that dates back to the 1960's. Gordon Moore theorized the movement toward multi-die devices within the semiconductor industry in 1965 within his groundbreaking paper, *Cramming more components onto integrated circuits*.[2]

Although his paper was very concise, 4 pages in length, it has become one of the most famous and widely shared within the semiconductor industry. Page 2 contains a statement that has become known as Moore's Law.[2]

*"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly, over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years."*

Moore's statement predicts the exponential increase in semiconductor technology that has now lasted, not for 10 years, but for more than 50 years. But now, Moore's Law is slowing…the cost for yielding large die continues to increase. As illustrated in the graphs created by ARM and AMD. The physical gate length of a transistor has decreased (at least plateaued) over time while the cost to produce usable die has increased. The cost-per-die yielded has doubled from producing 14/16nm die to 7nm die.

Image courtesy of ARM

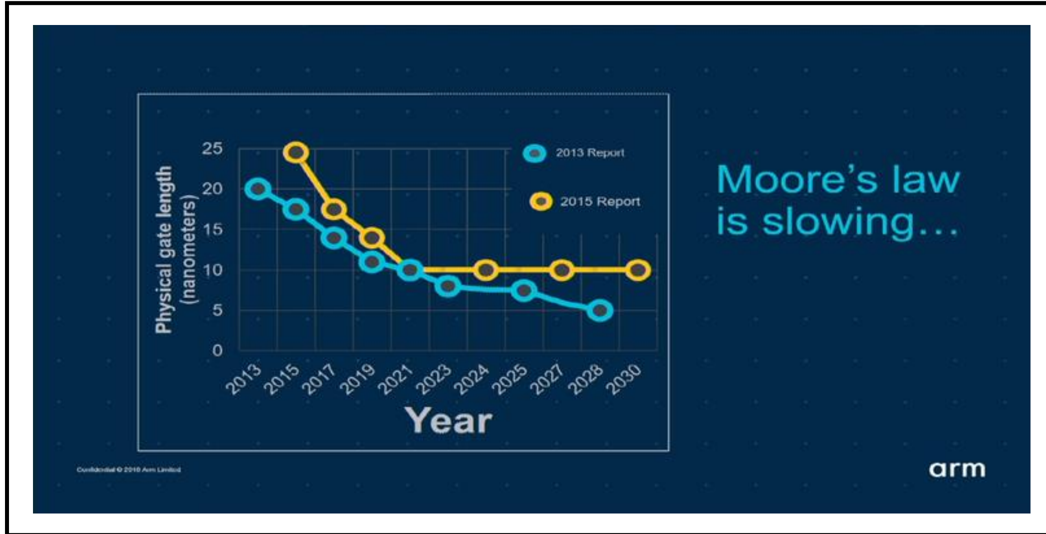



**Figure 3: Moore's law is slowing**

Image courtesy of AMD

**Figure 4: Moore's law slows while costs continue to increase**

Page 3 goes on to state that, just possibly, it might be better to build larger systems using smaller components integrated into a single package:

*"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."* [2]

Gordon Moore foresaw that heterogeneous integration would be a way to move the semiconductor industry forward. As Moore's law slows down, and number of transistors per die is no longer increasing, processing performance of chips will begin to plateau. The implementation of multi-die devices will further chip performance and allow for greater chip functionality and chip configurability.

## Multi-die Device D2D Interconnects

High speed D2D interconnects within multi-die devices can operate in the GHz range while providing GT/s of data. One of the challenges associated with heterogeneous integrated designs is accommodating the large amount of data moving between each chiplet when in operational mode. To accommodate this high-speed transfer, while minimizing noise, digital Serializer/Deserializer, also known as SerDes, are used as chiplet D2D interconnects.

While enormous strides have been made in advanced packaging solutions, choosing an interconnect technology that will accommodate large amounts of data, and is compatible with the packaging solution, is important. The ideal multi-die interconnect technology is scalable, low power, area-efficient, and buildable in a low-cost silicon and packaging technology.

There are three classes of D2D interconnect technologies used in multi-die devices:

- Medium-reach and long-reach Serializer/Deserializer (SerDes)
- Short-reach and ultra-short reach SerDes (USR/XSR)

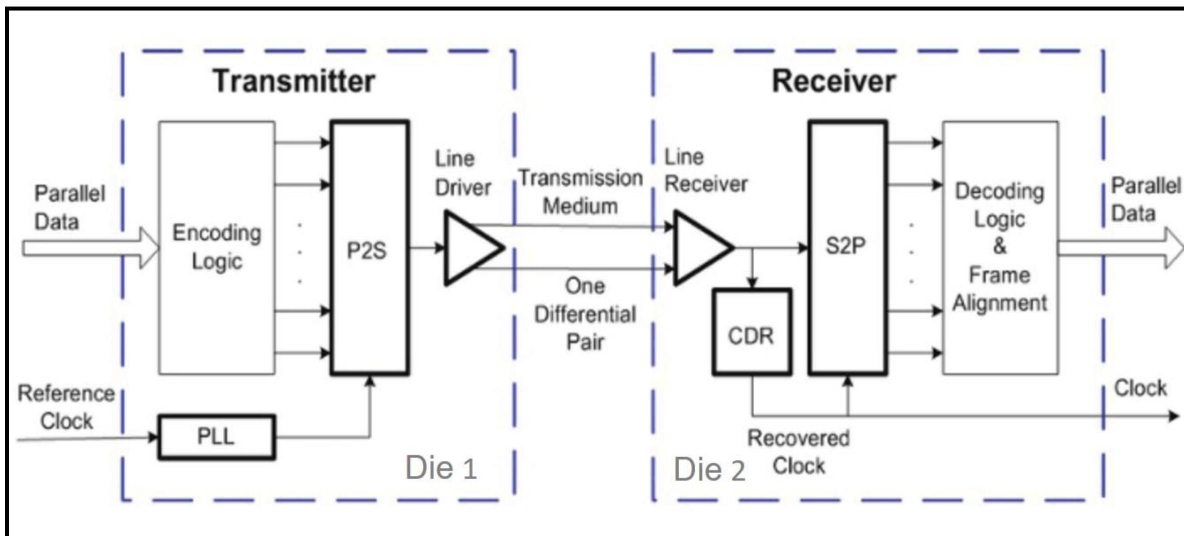



**Figure 5: SerDes D2D interconnect**

These D2D interconnects accommodate high-speed data transfer, while minimizing noise and minimizing the number of D2D interconnects. Parallel interface link technologies such as High Bandwidth Memory, Advanced Interface Bus, Bunch of Wires (HBM, AIB, BoW) are simple to implement and have high bandwidth; but may require many wires to completely implement.

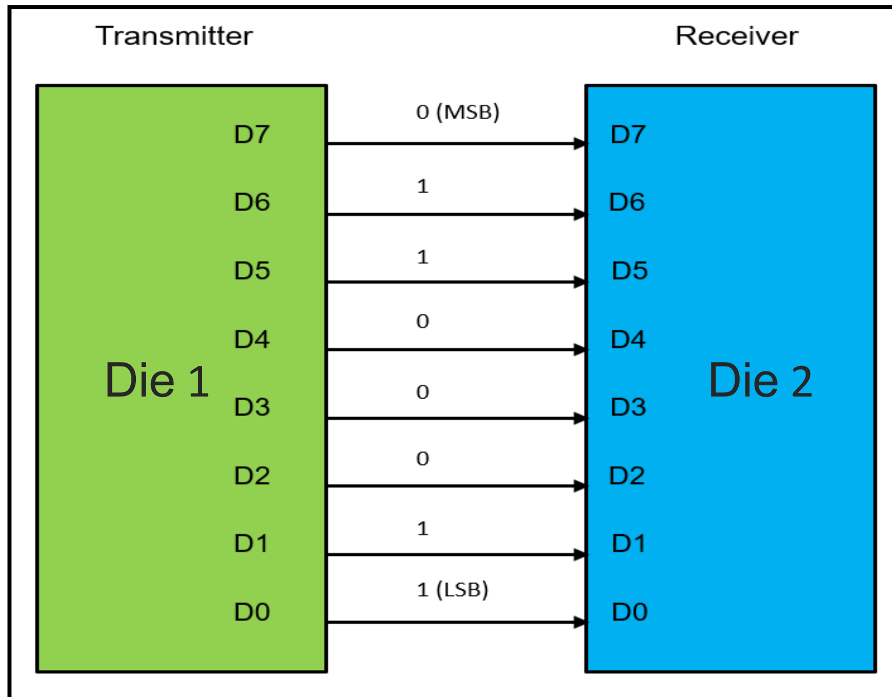



**Figure 6: Parallel D2D interconnect**

The MCM pictured is an Ethernet chip and has 8 surrounding chiplets that provide 6.4TB of data to the switch core when in operational mode. To accommodate this high-speed transfer, while minimizing noise, SerDes is used for the chiplet D2D interconnects. In terms of the signaling schemes, there are several technology options for D2D interconnects:

- Parallel
- Non-return to Zero (NRZ)
- Pulse Amplitude Modulation 4-level (PAM4)

Parallel interfaces are used when lower bandwidths are required. The NRZ and PAM4 signaling schemes are utilized when a SerDes methodology is selected which requires higher bandwidths.

The optimal D2D communications within a multi-die device lie in the desire to optimize six often competing but interrelated factors:

- Cost
- Die area available
- Power consumption
- Scalability
- Complexity

Image courtesy of Cadence

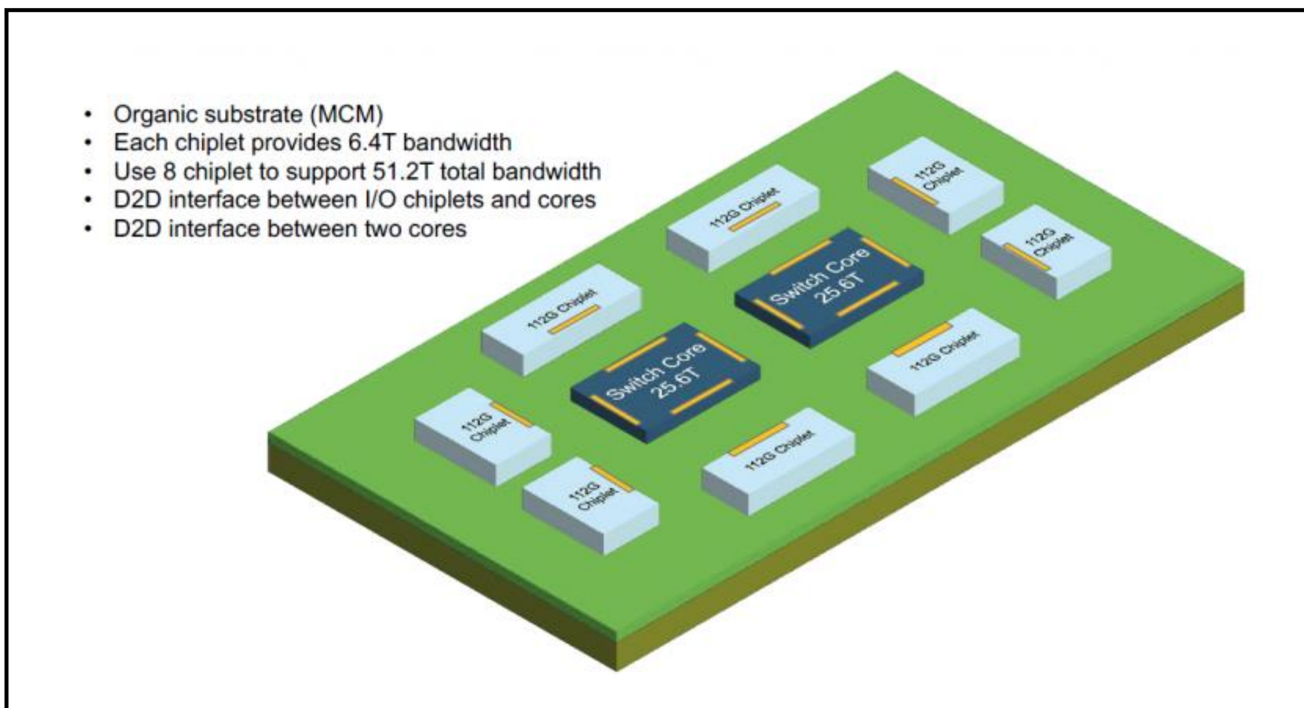
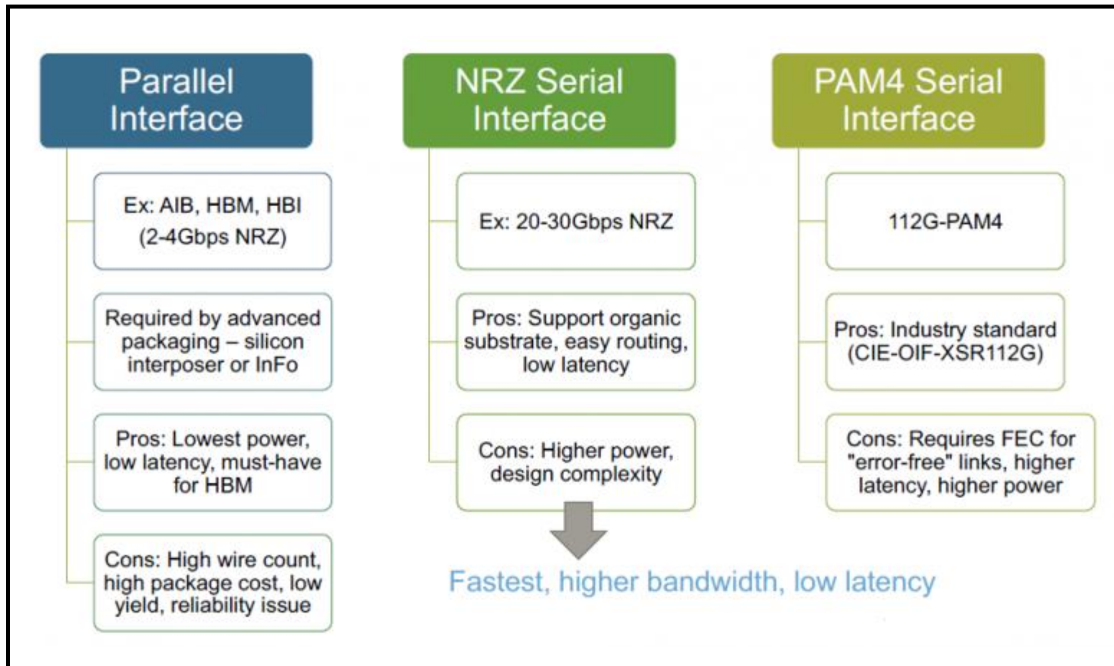



**Figure 7: Ethernet switch with 8 surrounding chiplets**

A key design consideration is the D2D interface on the package, highlighted in yellow in the figure above. The table below categorizes the technology options to evaluate for the D2D interconnect.

Distributed data processing in chiplets need high-speed data transfer between the chiplets. Parallel and serial are the two options of data transfer. Parallel data transfer requires multiple connections between chiplets compared to serial data transfer that only needs one pair of connections.[4] Serial D2D interconnect topographies have several advantages over parallel D2D interconnects.

**Table 1: Technology options to evaluate for D2D interconnects**




## Testing Multi-die Device D2D Interconnects

IEEE 1149.1 - Standard for Test Access Port and Boundary-Scan Architecture was conceived in the 1980s and adopted as a standard in 1990. Its adoption was accelerated in the mid-1990s because of factors leading to diminishing PCB test point access. Boundary-scan tests are applied to a PCB through a connector and a four-wire serial interface known as the Test Access Port (TAP). When implemented, this interface is commonly referred to as the “JTAG port”.

Since its development, the boundary scan standard has been adopted extensively by the industry and it is now deployed in chips, on PCBs, and in systems. Because of its widespread acceptance, the boundary scan embedded instrumentation has been appropriated by other applications and it provides the basis for other testing standards. A related standard, IEEE 1149.6 - Standard for Boundary-Scan Testing of Advanced Digital Networks, is used for testing high-speed differential and AC-coupled interconnects between chips on PCBs and systems.

IEEE 1838 - Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits is a die-centric standard; it applies to a die that is intended to be part of a multi-die stack. This standard defines die-level features that, when compliant dies are brought together in a stack, comprise a stack-level architecture that enables transportation of control and data signals for the test of (1) intra-die circuitry and (2) inter-die interconnects in both (a) pre-stacking and (b) post-stacking situations, the latter for both partial and complete stacks in both pre-packaging, post-packaging, and board-level situations. The primary focus of inter-die interconnect technology addressed by this standard is through-silicon vias (TSVs); however, this does not preclude its use with other interconnect technologies such as wire-bonding.

Since multi-die devices and D2D interconnects are reminiscent to interconnects between chips on a PCB, test methodologies that apply to PCB can apply to testing D2D interconnects. The test patterns generated by IEEE 1149.1 - Standard for Test Access Port and Boundary-Scan Architecture and IEEE 1149.6 - Standard for Boundary-Scan Testing of Advanced Digital Networks are suited for structural testing D2D interconnects comprising the multi-die device.

Boundary scan is a static vector-based test technology that uses on-chip embedded instruments to perform structural testing. As such, boundary scan can perform shorts, opens, stuck-at, and bridging fault testing and detection very quickly, whether the die is packaged and mounted on a PCB or stacked die in a multi-die device. The diagnostics provided are to the device/chip and net/pin level. Boundary scan provides a very effective means of detecting and diagnosing in-situ assembly defects since in many situations, access to nets are not available or probing nets is not prudent.[3] Boundary scan is suited to discover defects on single-ended and differential nets.

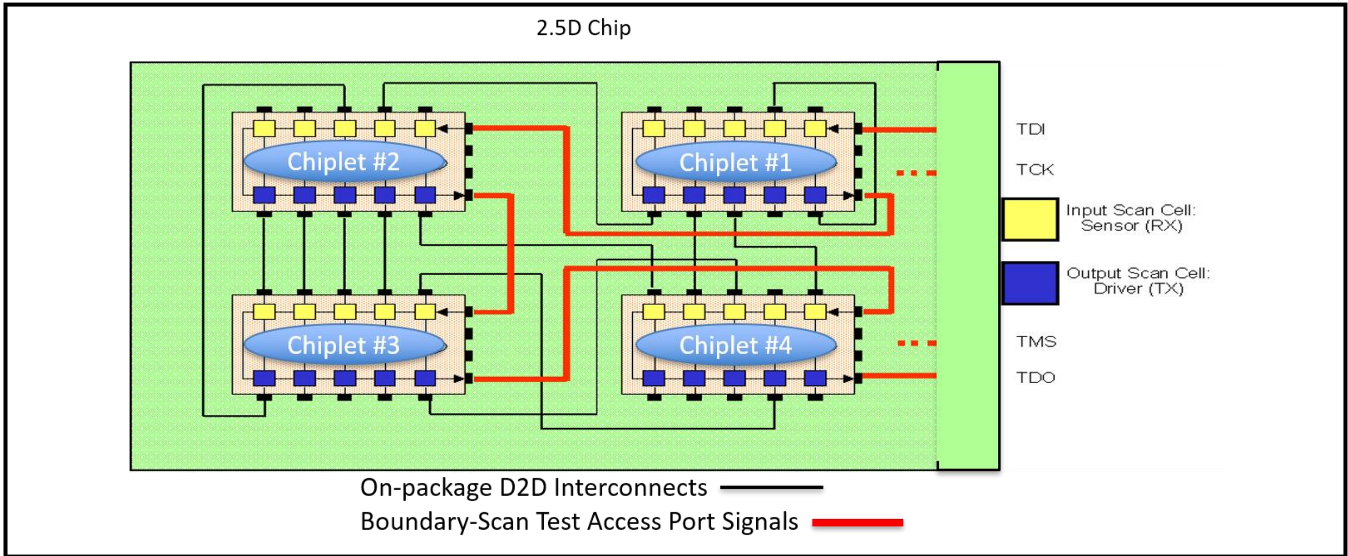



**Figure 8: 2.5D chip testable with IEEE standards**

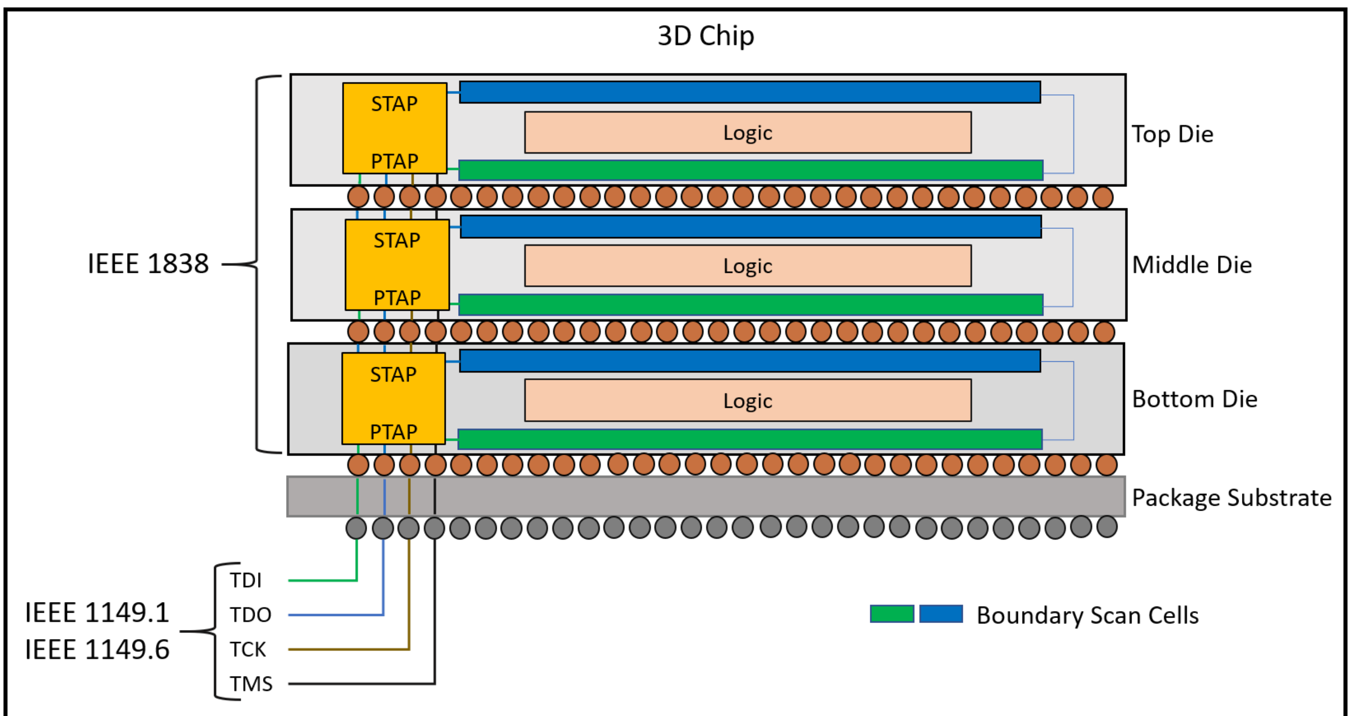



**Figure 9: 3D chip testable with IEEE standards**

## D2D Interconnect Test Patterns

Walking 1, walking 0, and Wagner patterns are used to test for shorts, opens, stuck-at, and bridging faults between D2D interconnects of multi-die devices. Today's boundary-scan tools, when provided with a netlist, Boundary Scan Description Language (BSDL) files, and device models, use their built-in automatic test pattern generator (ATPG) to create D2D interconnect test patterns for any size design. These D2D interconnect test patterns can be applied in seconds on the manufacturing floor.

### Walking 1

The walking 1 pattern can be applied to test D2D interconnects between chiplets of a multi-die device. This test derives its name from the bit values that are written during the test. The walking 1 test pattern involves transmitting a single "1" on a first net during the first vector step while the other n-1 nets are set to "0". At the second vector step, the "1" is applied to a second net while the other n-1 nets are set to "0". In this way, the "1" that is applied ("walks") across all n nets in as many steps.

Since the number of test steps grows linearly with the number of nets tested, more efficient algorithms may be preferrable.

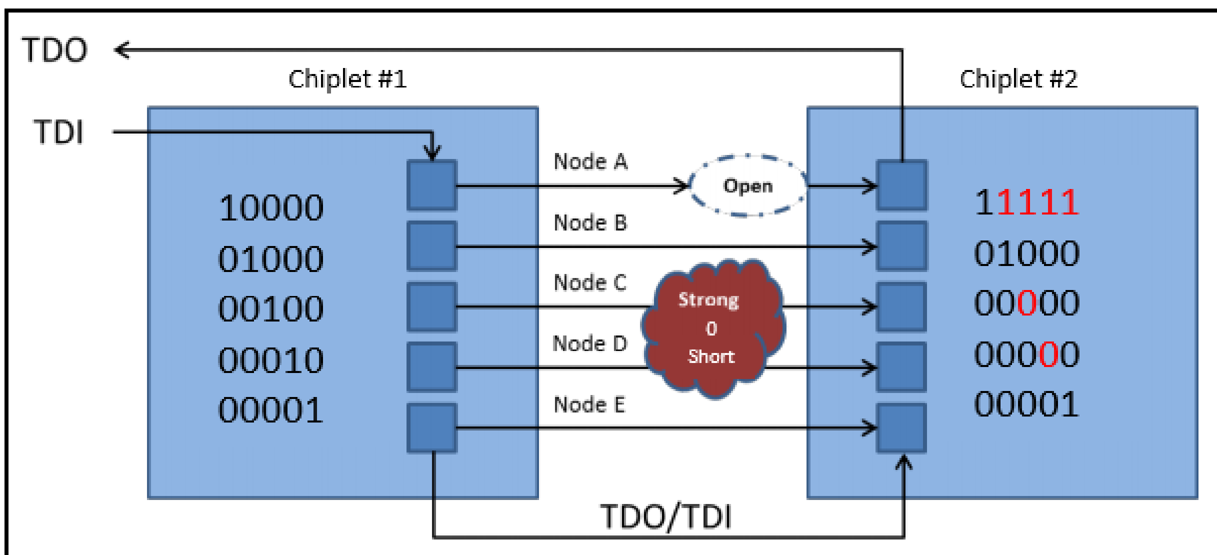



**Figure 10: Chiplet D2D test using a walking 1 pattern**

The figure demonstrates this concept of walking 1 patterns on a group of nets applied by transmit boundary-scan cells on the left and the value captured by the receiving boundary-scan cells on the right. The values in red indicate bit mis-compares due to detected faults.

## Walking 0

The walking 0 pattern can be applied to test D2D interconnects between chiplets of a multi-die device. This test derives its name from the bit values that are written during the test. The walking 0 test pattern involves transmitting a single "0" on a first net during the first vector step while the other n-1 nets are set to "1". At the second vector step, the "0" is applied to a second net while the other n-1 nets are set to "1". In this way, the "0" that is applied ("walks") across all n nets in as many steps.

Since the number of test steps grows linearly with the number of nets tested, more efficient algorithms may be preferrable.

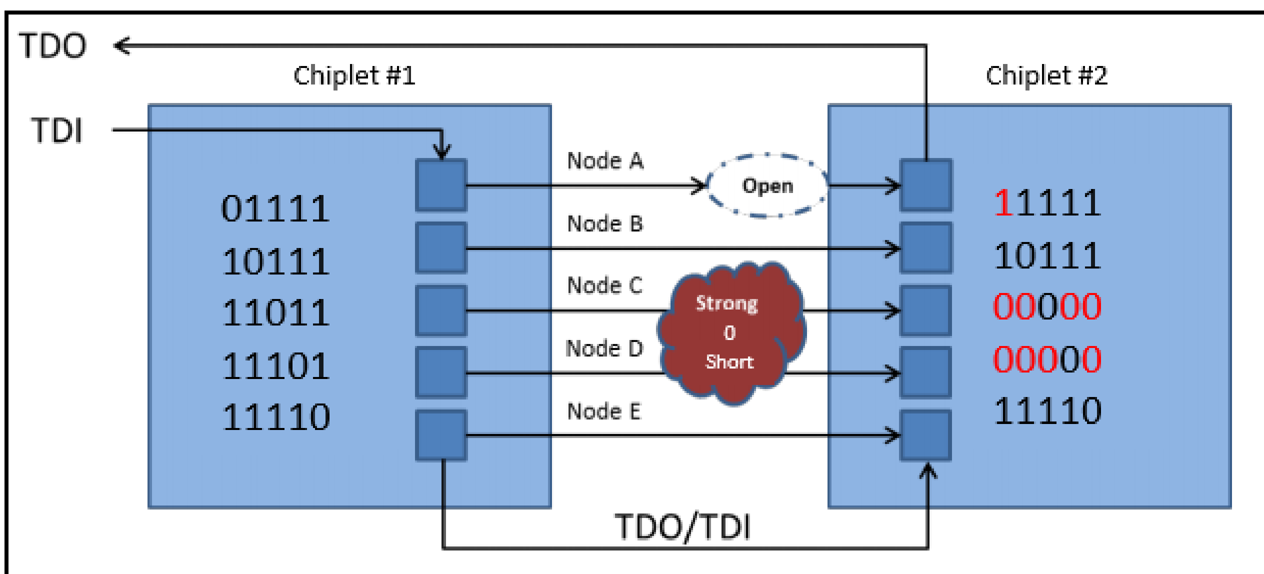



**Figure 11: Chiplet D2D test using a walking 0 pattern**

The figure demonstrates this concept of walking 0 patterns on a group of nets applied by transmit boundary-scan cells on the left and the value captured by the receiving boundary-scan cells on the right. The values in red indicate bit mis-compares due to detected faults.

## Wagner

Wagner patterns are an extended binary count pattern. Wagner patterns provide 100% fault coverage for shorts, opens, stuck-at, and bridging faults. The number of test steps grows logarithmically, not linearly, with the number of nets tested. Wagner patterns minimize the pattern size while ensuring full coverage and efficient diagnosis. Wagner patterns do not require pairing with other patterns to increase test coverage.

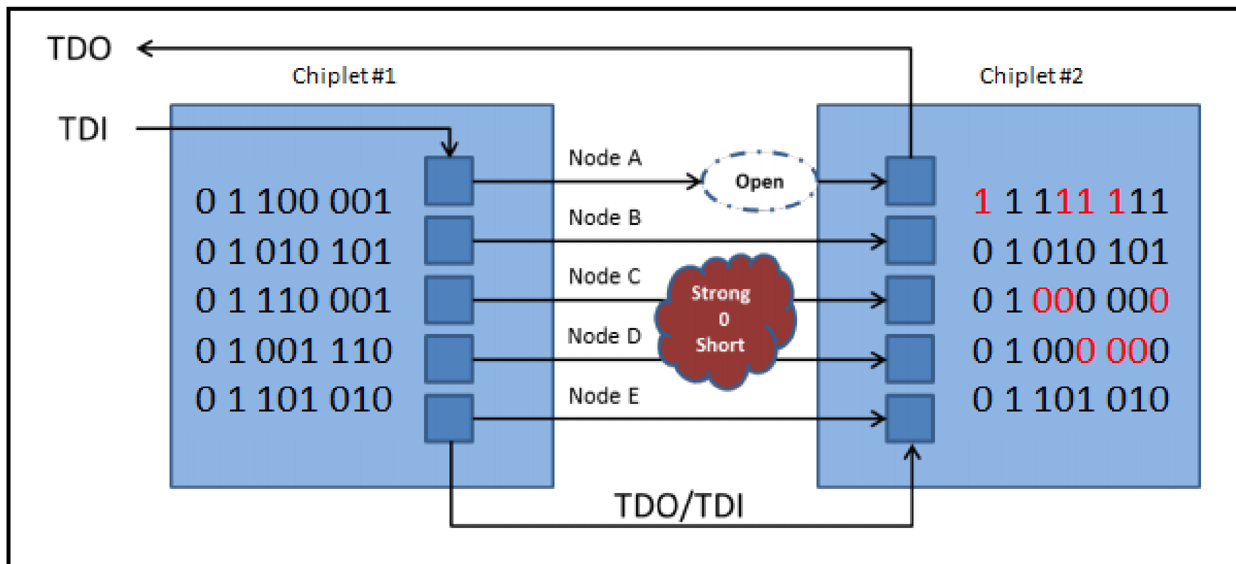



**Figure 12: Chiplet D2D testing using a Wagner pattern**

The figure demonstrates this concept of Wagner patterns on a group of nets applied by transmit boundary-scan cells on the left and the value captured by the receiving boundary-scan cells on the right. The values in red indicates bit mis-compares due to detected faults. Wagner patterns are the most efficient patterns for optimizing test coverage and diagnostics.

## Standard Test Interface Language

IEEE 1450 - Standard Test Interface Language (STIL) provides a means of describing digital testing patterns and waveforms as a common test language. Once described, these test patterns and waveforms can be ported to another test environment or ATE platforms for application to interconnects between multi-die devices. STIL test patterns and waveforms can be generated when simulating digital chips by EDA tools. STIL can also be created by postprocessing test patterns and waveforms output by third party tools.

The "EDA-to-Test" flow is filled with many different formats for test information. Different formats exist not only for the interface between EDA tools and chip vendors, but also for the interface between chip vendors and ATE.

Because of these differences, a standard language was needed. STIL, which was standardized in 1999 by The Tools and Tester Consortium and consisted of corporate leaders in both the chip and ATE industries. STIL test patterns and waveforms can be generated by EDA tools.

STIL was created in response to specifically address growing concerns in creating large volumes of digital test data by EDA tools and the ability to transfer that digital test data between various platforms. There was no direct interface between EDA tools and chip vendors, nor was there a direct interface between chip vendors and ATE.

Therefore, STIL is beneficial to the EDA vendors who create test data, the chip vendors who manipulate test data and the ATE vendors who accept test data. STIL can be ported to chip ATE for application to D2D interconnects and once ported, STIL patterns are applied to the D2D interconnects via the boundary-scan cells.

Test programs written in STIL generally consist of seven blocks that define STIL: Header, Signals, SignalGroups, Timing, PatternBurst, PatternExec, and the Pattern. Each block is created based on the design description of the chiplet D2D interconnects to be tested.[8]

```
Signals {
   "A_Jce1" In;
   "A_Jce2" In;
   "A_Tck" In;
   "A_Tdi" In;
   "A_Tms" In;
   "A_Tdo" Out;
   "B_Jce1" In;
   "B_Jce2" In;
   "B_Tck" In;
   "B_Tdi" In;
   "B_Tms" In;
   "B_Trstn" In;
   "B_Tdo" Out;
}
SignalGroups {
   "default" = '"A_Jce1" + "A_Jce2" + "A_Tck" + "A_Tdi" + "A_Tms" + "A_Tdo"
+ "B_Jce1" + "B_Jce2" + "B_Tck" + "B_Tdi" + "B_Tms" + "B_Trstn" + "B_Tdo"';
   "__ALL__" = '"A_Tck" + "A_Tdi" + "A_Tms" + "A_Tdo" + "B_Tck" + "B_Tdi" +
"B_Tms" + "B_Trstn" + "B_Tdo"';
}

Timing {
  WaveformTable "default" {
    Period '100ns';
    Waveforms {
      "A_Jce1" { 01xz { '10ns' D/U/N/Z;  } }
      "A_Jce2" { 01xz { '10ns' D/U/N/Z;  } }
      "A_Tck" { 01xz { '50ns' D/U/N/Z; '100ns' D/D/N/Z; } }
      "A_Tdi" { 01xz { '10ns' D/U/N/Z;  } }
      "A_Tms" { 01xz { '10ns' D/U/N/Z;  } }
      "A_Tdo" { LHXZ { '10ns' X; '80ns' L/H/X/T; } }
      "B_Jce1" { 01xz { '10ns' D/U/N/Z;  } }
      "B_Jce2" { 01xz { '10ns' D/U/N/Z;  } }
      "B_Tck" { 01xz { '50ns' D/U/N/Z; '100ns' D/D/N/Z; } }
      "B_Tdi" { 01xz { '10ns' D/U/N/Z;  } }
      "B_Tms" { 01xz { '10ns' D/U/N/Z;  } }
      "B_Trstn" { 01xz { '10ns' D/U/N/Z;  } }
      "B_Tdo" { LHXZ { '10ns' X; '80ns' L/H/X/T; } }
    }
  }
}
```

**Figure 13: STIL produced by ScanWorks**

## Using ScanWorks to Produce STIL

Since its inception, ASSET's ScanWorks for Boundary-Scan Test has provided board-level shorts, opens, stuck-at, and bridging fault testing of interconnects between boundary-scan devices using its Automatic Test Pattern Generation (ATPG) feature. With recent enhancements, ScanWorks now generates STIL patterns that can be applied by chip ATE to test for shorts, opens, stuck-at, and bridging faults of D2D interconnections between chiplets.

The ScanWorks STIL option produces test patterns based on the chiplet BSDL's and the netlist describing how the chiplets are interconnected. Using the ScanWorks STIL option has several key values for chip manufacturers and board designers:

- Multi-die device suppliers can provide the ScanWorks project used to generate the STIL patterns to downstream board designers and contract manufacturers
- Board designers can apply D2D interconnect tests to the board and to the multi-die device to confirm quality
- Problems found with the multi-die device can be traced back to the package supplier who has the same test on their ATE to help debug whether it is a board or multi-die package issue

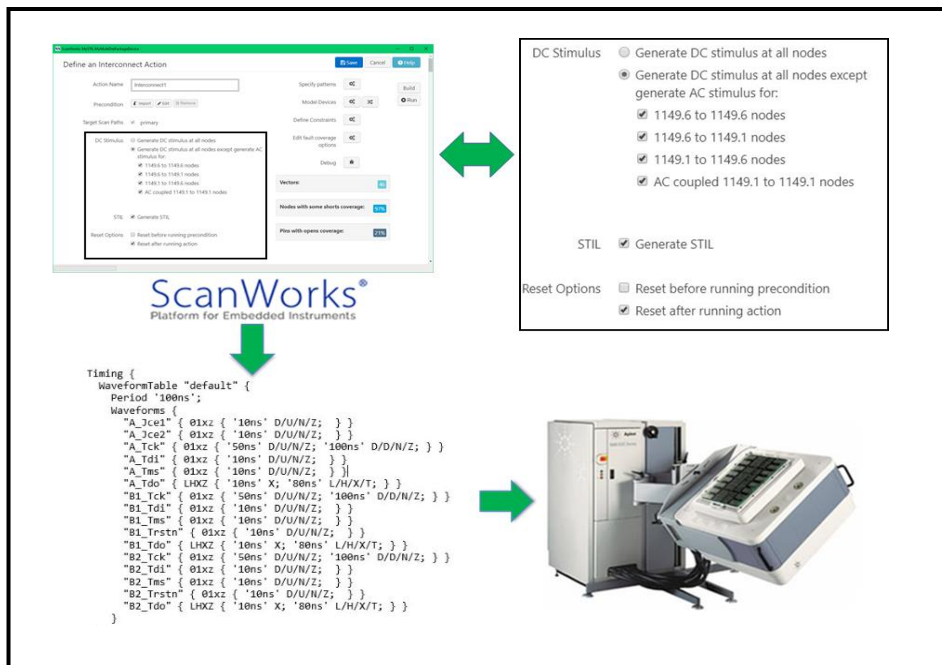



**Figure 14: ScanWorks STIL process flow**

## Summary

Chiplet-based, multi-die packaging innovations has allowed the semiconductor industry to create smaller, faster, configurable, and lower power chips. Heterogeneous integration has been a driving force in the construction of chiplet-based, multi-die devices. Advanced packaging innovations have been adopted by the semiconductor industry to achieve the economic advantages that were previously met with silicon scaling. Multi-die devices are an important approach towards diverting from monolithic die designs to more manageable and less expensive chiplet designs.

D2D interconnect testing can be accomplished using the IEEE 1149.1 - Standard for Test Access Port and Boundary-Scan Architecture along with IEEE 1149.6 - Standard for Boundary-Scan Testing of Advanced Networks. Each standard takes advantage of pattern generation schemes to uncover shorts, opens, stuck-at, and bridging faults on die-to-die interconnects between chiplets. Boundary-scan testing takes advantage of the embedded boundary-scan cell infrastructure of the silicon chiplets. D2D interconnect testing yields structural results in-situ. IEEE 1838 - Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits defines test access infrastructure for testing interconnects between multi-stacked-die chips.

IEEE 1450 - Standard Test Interface Language is used to define test patterns in one common language. STIL patterns can be used to facilitate digital IEEE 1149.1 and IEEE 1149.6 shorts, opens, stuck-at, and bridging faults between D2D interconnects chiplets in multi-die devices. ASSET has implemented STIL support beginning with the ScanWorks 4.8 release. STIL patterns generated by ScanWorks can be applied by chip-level ATE without the need for ASSET hardware.

Using ScanWorks STIL for D2D interconnect testing fits in the overall multi-die device manufacturing test flow. With this enhancement, ScanWorks provides an automated and scalable D2D interconnect test authoring solution deployable throughout the lifecycle of a multi-die device.

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