ScanWorks®
Platform for Embedded Instruments

SPI Flash IP -
FPGA-based Fast Programming Instrument

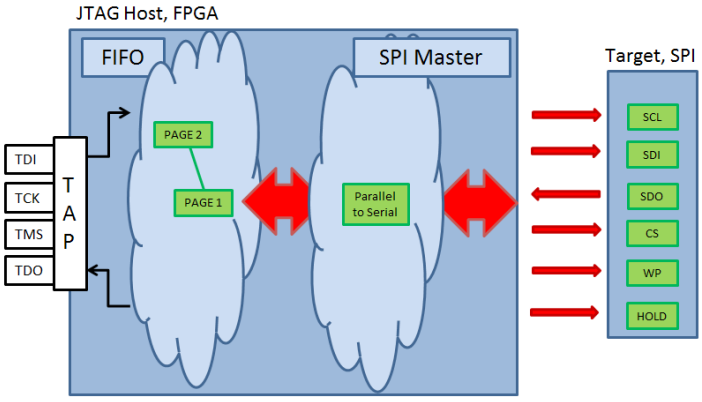
Fact Sheet

Introduction

The SPI Flash Player IP (SPI Flash IP) is an easy-to-use instrument providing at-speed programming of Flash/EEPROM devices based on the Serial Peripheral Interface (SPI) Bus in a board test FPGA environment.

The SPI Flash IP is used within the ScanWorks® FPGA-based Fast Programming (FFP) Development software. When you select and configure the SPI Flash IP instruments, ScanWorks® automatically connects it with other instruments of your choice and turns them into a cohesive, on-chip tester architecture.

The SPI Flash IP is included in the FFP Development software. For more information about FFP and other FPGA-based Fast Programming Instrument IPs from ASSET visit our website at: https://www.asset-intertech.com/products/fpga-fast programming.



Functional Description

The SPI Flash IP consists of two major parts, a FIFO (First In – First Out) register and a SPI Master. The FIFO receives page size data from the boundary-scan controller. The SPI Master will program those pages into the Target SPI Flash. This two-step architecture maximizes programming speeds and can reach the limit of the SPI device depending on the application. The SPI Master operates in full duplex mode and communicates in master/slave mode where the master initiates the data frame.

The SPI Flash IP is pin-mapped and synthesized into the FPGA using the Embedded Tester Generator (ETG) together with the FPGA vendor tools. The ETG, a standard part of the FFP Development Software, outputs the following files to be imported in ScanWorks:

- A Serial Vector Format (SVF) file for configuring the FPGA
- A custom Boundary-Scan Description Language (BSDL) file
- An Instrument Map file used for automatic configuration access between the FPGA and SPI device

Key Benefits:

- Program SPI devices with large amounts of data faster than standard boundary scan access methods
- Faster programming increases manufacturing through-put while reducing manufacturing costs
- In-system programming eliminates need for using pre-programmed parts or removing soldered parts for re-programming
- Can be combined with other structural and functional test as a part of the overall test sequence

Key Features:

- At-speed SPI Flash Programming
- Model-based development
- Complete development environment
- Synthesizing and pin-mapping

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Frequency Measure IP (FM IP) Instrument

Embedded Tester Generator Configurable Parameters

The Embedded Tester Generator (ETG) software will automatically wrap an IJTAG IEEE 1687 network around the IP and guide you in the parameter setting, pin mapping, and synthesis processes. The following parameters can be set when synthesizing the IP into an FPGA.

Configurable Parameter		
Name	**Description**	**Description**
SPI_POLARITY	Controls SCLK polarity relationship of SPI interface.	Target Device Dependent
SPI_PHASE	Controls SCLK polarity relationship of SPI interface.	Target Device Dependent

The following IO ports can be configured and pin-mapped when synthesizing the IP into an FPGA.

Configurable IO				
Name	**IO Type**	**Parameter Control**	**Description**	**Pin Mapping**
sysclk	Input	n/a	IP system clock input.	Required
miso	Input	n/a	SPI data input.	Required
mosi	Output	n/a	SPI data output.	Required
sclk	Output	n/a	SPI clock output. Based on this formula: sclk = sysclk / 2	Required
ssel	Output	n/a	SPI slave select output.	Required

ScanWorks SPI Flash Action

The SPI Flash Action has user-selectable operations for checking manufacturer and device id, blank check and erase, program, secure, and verification of the programmed image. It is possible to use multiple source files in the same action and map each source file to different location in the memory map of the flash. The source files can be of binary, S-record, or Intel-Hex type.

Application Examples

Application Examples				
Customer Industry	**Access Method**	**TCK**	**File Size**	**Program Time**
Defense	Embedded SPI Flash IP	10 MHz	10 MB	25 seconds
Communication	Embedded SPI Flash IP	7 MHz	8 MB	20 seconds

ASSET Contacts:

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