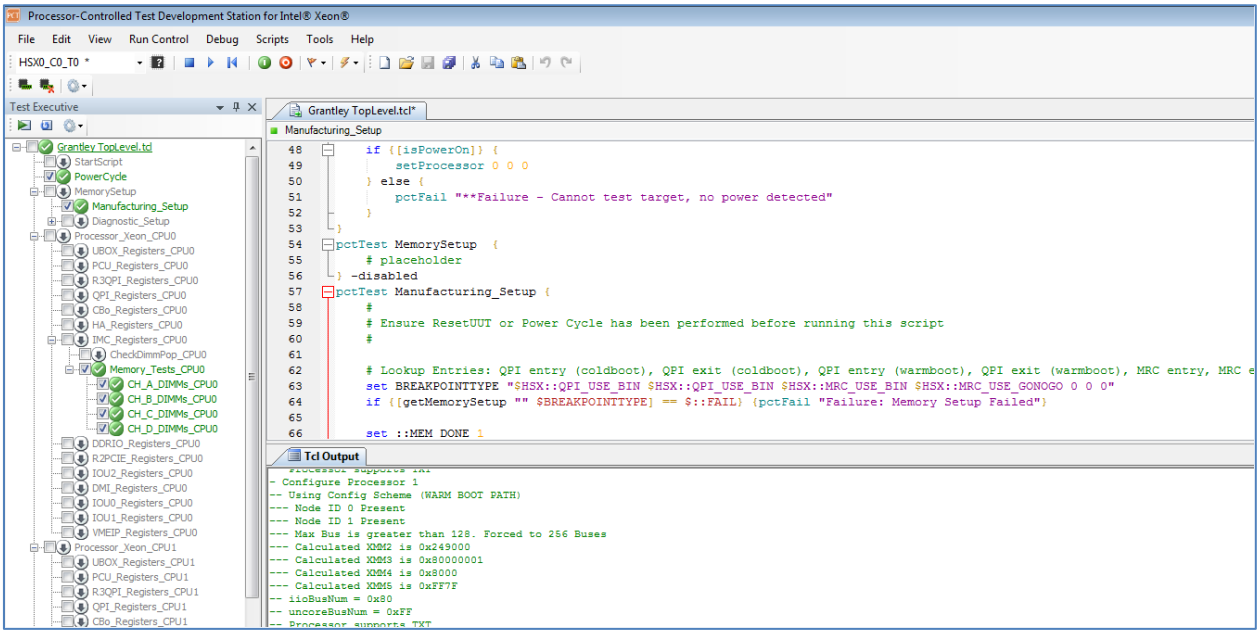
ScanWorks® Processor-Controlled Test Development for Intel® Processors

You chose the most powerful Intel® processor for your board design. Now you need a tool that simplifies the complexity that came with your processor to simplify your board test task.

ScanWorks® Processor-Controlled Test (PCT) gives you a single tool for prototype board initialization, prototype debug, structural test and functional test with diagnostics, all without a BIOS.

Overview

Today's Intel board designs are as complex as the processors from Intel creating a challenge to maximize test coverage for test engineers. Whether you are using an Intel Core™ or Intel Xeon® processors, you must have tools that deal not only with the processor architecture, but the chipset as well. ScanWorks Processor-Controlled Test (PCT) lets you see what the silicon sees and control the behavior of the chip for both prototype board debug and later for production test. With power comes complexity and today many of Intel's processors contain multiple cores, while others are implemented as a system-on-a-chip (SOC). To open a path to design insight, you need to put the processor to work as soon as board power-on is complete. ScanWorks PCT is a tool for hardware developers that shortens time-to-insight through the entire product development life cycle, from prototype to manufacturing. PCT provides prototyping debug via a powerful scripting language (TCL) and test development via tool automation.



PCT provides for automated test setup without the need for the BIOS being present on the board. The goal of the tool is to maximize test coverage and provide robust diagnostics. It achieves this by:

a) Configuring the platform (Unit Under Test or UUT) via device initialization models
b) Configuring the memory controller via Intel Customer Reference Board models
c) Using PCT's test library to generate and apply board specific tests
d) Creating Diagnostic reports

This provides Better, Faster and More Precise results than traditional test methodologies.

Memory Tests Overview

The most common complaint with testing memories on an Intel designs is "I cannot diagnose faulty memory to the bit level". To address this PCT has a two-stage approach. Stage 1 involves memory setup and stage 2 tests the memory devices. In the first stage, PCT uses a proprietary instrumented Memory Reference Code (MRC) to ensure that all channels and memories are visible (which is not the case in many BIOS's as the default is "boot at all costs", which means some memories potentially will not be accessible). This instrumentation allows the test to halt and report the error early in the test cycle when training errors are present. Then stage 2 is simple: by applying the PCT built-in memory test the tool can report bit level problems on Intel Core designs automatically and with a little extra effort bit-level can be achieved for the more complex Xeon designs.

IO Tests Overview

PCT's methodology for IO testing is similar to that for memory testing. First the device is initialized and then built-in device tests are executed. The device initialization starts by extracting data from a known UUT, ensuring that all IO devices are enumerated. This data provides the device id which is used to index into the PCT device model library and then extract the test for this type of device. Additional data for device initialization that was gathered from the known UUT is merged into the platform library to create a custom, yet automated test for a specific platform.

Device Programming Overview

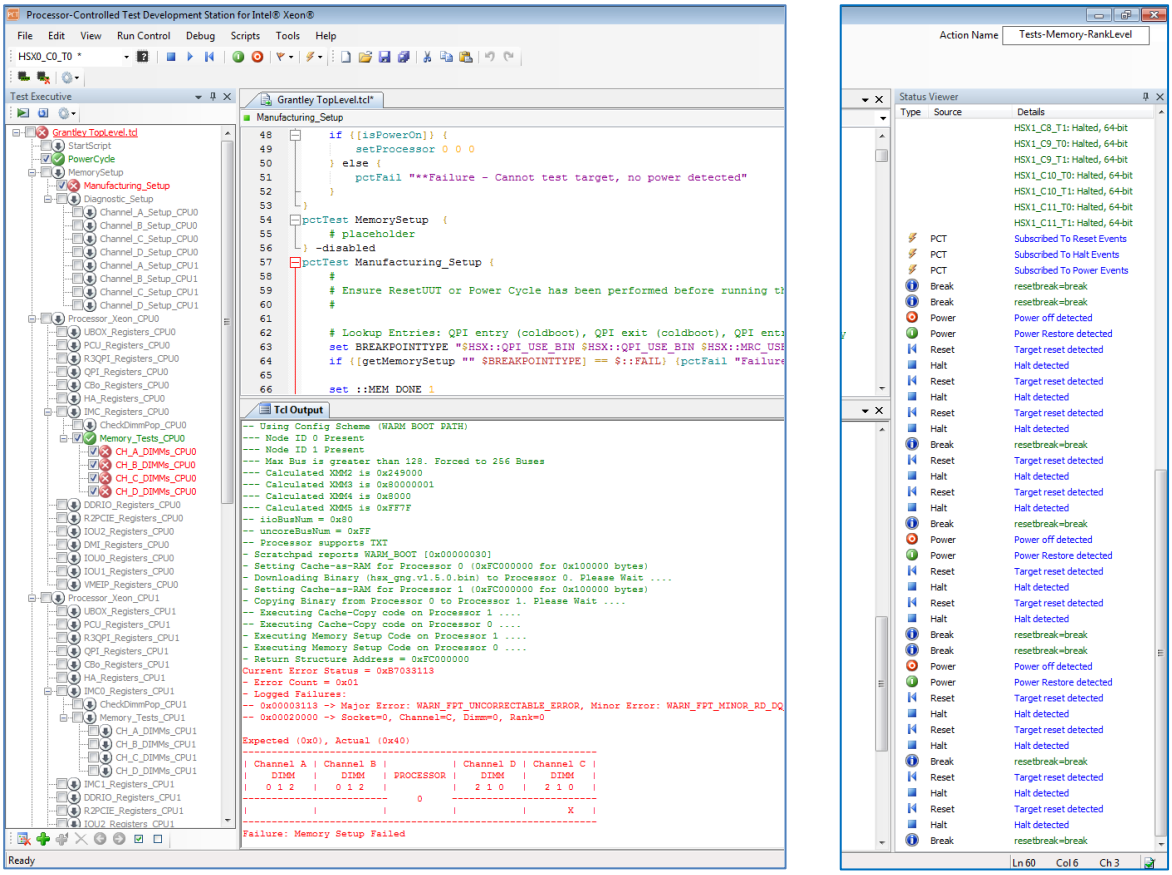
Changing content on Intel designs is often required to match the particular configuration of the board and changing out tools to accomplish this task can be painful and time-consuming. To eliminate the problem, PCT provides the ability to program flash and SPI devices. PCT has a device library and provides the ability for the user to configure unique device parameters. To ensure the fastest programming for a given device, PCT uses device-specific programming algorithms.

Manufacturing vs Offline Diagnostics Overview

ASSET looks at board test from two different perspectives and then provides the user of the tool a choice. For manufacturing, speed is of the essence to manage the beat rate of the production floor while still providing the maximum diagnostic resolution possible without sacrificing speed. For Intel designs that is challenging, but for Intel Core designs, PCT provides platform failure data to the device level and for memories to the bit level all within the manufacturing setting. For the more complex Intel Xeon designs the process is slightly different: PCT provides platform failure data to the device level and for memories to the rank level so speed is maximized. With the additional complexity of the memory architecture on Xeon designs, to achieve bit-level diagnostics, the beat rate would be unacceptable. However, to address the need for bit level memory testing on Xeon, PCT provides for an Offline Diagnostics mode that ensures the correct configuration of the memory controller in multi-socketed designs.

Manufacturing Tests without BIOS

Execution of the BIOS for test can create problems for manufacturers. Problems with the wrong version of the BIOS installed can cause false failures, or worse, passes that should fail. Also, with the desire for booting at all costs, the

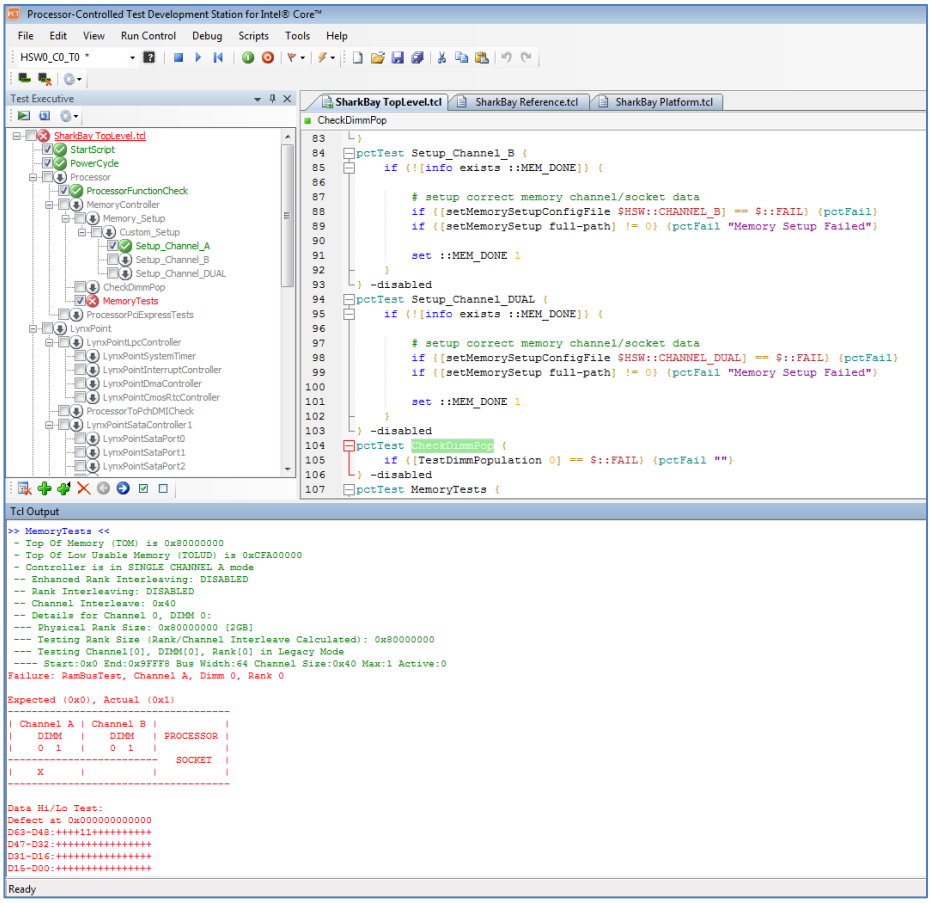


BIOS will often disable the suspect channel, leaving the memories associated with that channel inaccessible. PCT replaces the BIOS by conducting the same device setup as the BIOS, but tracks failures and stops the test early in

the test cycle. PCT provides a test instrumented MRC to ensure that no memories are omitted in the memory setup, thus enabling 100% confidence in the memory test results.

Offline Diagnostics Tests

As previously mentioned, due to the complexity of Xeon designs, diagnostics to the bit-level, (or beyond rank-level diagnostics), takes an additional step. This is achieved by having a test profile target a specific memory channel. The profile will ONLY configure and test the channel using a special sequence created by PCT that is tied to the processor and memory devices. This is the methodology for testing Intel Xeon designs due to their complexity and the length of time necessary to get bit-level granularity, which may not be suitable for manufacturing.



Test Development - A Simple 4 Step process

PCT is all about maximizing test coverage and diagnostics in an automated fashion. To that end, the four step process is designed for maximum efficiency of the test developers' time.

Step 1 begins by connecting to a known golden board.

The golden board is the test engineering standard with all devices and memories populated and is totally functional.

Step 2 is where PCT then learns the setting of the devices.
(Chipsets, platform, IO and memory) to construct a platform library.

Step 3 is running the Automated Test Generation (ATG) tool to construct a test profile.
The ATG takes device initialization data and merges it with built-in test routines. The test routines have built-in diagnostic message templates that cover the fault spectrum possible for the specific test.

Step 4 executes the test and generates the diagnostic results.

Processors Supported

ScanWorks PCT supports Intel Xeon and Core processors for servers, desktops, notebooks, and other embedded systems. Supported processors are:

- 4th General Intel Xeon E7/E5/E3 Processors
- 5th Generation Intel Xeon E3/D Processors
- 4th Generation Intel Core i7/i5/i3 Processors
- 5th Generation Intel Core i7/i5/i3 Processors

For a comprehensive list of Intel product names and SKU by family see http://ark.intel.com/

ScanWorks Platform for Embedded Instruments

The ScanWorks platform for embedded instruments is a seamless software environment that validates, tests and debugs circuit boards, chips and systems. The ScanWorks platform includes tools for Boundary-Scan Test (BST), Processor-Controlled Test (PCT), High-Speed I/O (HSIO) validation, FPGA-Controlled Test (FCT) and IJTAG test (IJTAG).

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