# SCANWORKS® IJTAG DEVELOPMENT

IJTAG for Chip or Board Design Debug and Non-intrusive Board Test benefits both design and test.

#### **OVERVIEW**

ScanWorks® IJTAG Development (IJTAG-DL) software makes it easy to develop IJTAG-based embedded instrument tests. The software supports both standard data formats defined as part of the IEEE P1687 IJTAG standard; Procedural Description Language (PDL) and Instrument Connectivity Language (ICL). Once imported into the IJTAG-DL, an easy drop and drag user interface is available to select operations to build your IJTAG test. The IJTAG tests developed during prototype debug or new product introduction can easily be re-used during the entire product life-span.



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Run_MBIST	Si	ave ca	ance
ouild run rename	Instruments edit ICL edit PDL module:INIT PEEK MBIST		
Davisas iMa	D IEEE1687_NETWORK.IPM_1.INIT_PEEK_MBIST_0	▼ 5 items	
U1 (XC3S400_PQ208)	Operations for IEEE1687_NETWORK.IPM_1.INIT_PEEK_MBIST_0		
	BIST_Done_Monitor(WATCH_LIMIT)		
Data Handling	bitslice(msblsb bitrange)		
Fail on 0 miscompare(s)	Dump_RAM		
Stop on 0 miscompare(s)	INIT_Done_Monitor(WATCH_LIMIT)		
Contraction of this compare(s)	INIT_Reset		
Collect data  Precondition: import edit delete	INIT_Start		
	INIT_Stop		
	MBIST_Clear_Fail		
	MBIST_Reset		
	MBIST_Start		
	MBIST_Stop		
	Peek_ADDR(ADDR_Sbit)		
	Record_Message( logfile text_message )		
	(Drag and drop operations to add them)	filter	4
Selected Operations			
J1IEEE1687_NETWORK.MFP_1.MMODE_FMODE_POKE_0.	MMODE_FMODE_POKE::Set_NoFault	8	
J1.IEEE1687_NETWORK.IPM_1.INIT_PEEK_MBIST_0.INIT_PE	EK_MBIST::Dump_RAM		
J1.IEEE1687_NETWORK.MFP_1.MMODE_FMODE_POKE_0.	MMODE_FMODE_POKE::Set_MBIST_Mode	8	
J1.IEEE1687_NETWORK.IPM_1.INIT_PEEK_MBIST_0.INIT_PE	EK_MBIST::MBIST_Reset	6	
JIEEE1687_NETWORK.IPM_1.INIT_PEEK_MBIST_0.INIT_PE	EK_MBIST::MBIST_Start	8	
JIEEE1687_NETWORK.IPM_LINIT_PEEK_MBIST_0.INIT_PE	EK_MBIST::BIST_Done_Monitor(100)	/ 8	
JIJEEE1687 NETWORK IPM 1 INIT PEEK MBIST 0 INIT PE	EK MBIST::MBIST Stop	8	
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#### VECTOR AND PROGRAM CREATION

Test vector creation begins with the instrument creation during the design cycle. The instrument operations are described in PDL models, written by the instrument designer or test developer. Once the instruments PDL models are created they can be archived and easily reused in the automated model-based environment the ScanWorks Platform provides.

When the instruments are placed into an IJTAG design, an ICL file will be generated that describes the scan path access to the embedded instrument. The IJTAG development software then uses the instrument's corresponding PDL file(s) to operate the instrument. Multiple instrument operations can be organized in a single IJTAG action. In fact, multiple instruments can be operated at the same time providing excellent throughput and test times.





#### DIAGNOSTICS

The use of PDL and ICL provides far more flexibility and better resources for diagnosing the IJTAG tests than what can be achieved by running the tests from standard SVF (serial vector files). Advanced diagnostics can be generated in PDL for each specific instrument. The limitation on the resolution of diagnostic granularity is only down to the actual instrument's intrinsic hardware capabilities.

# **DEBUGGING IJTAG TEST PROGRAMS**

The ScanWorks IJTAG Development software can be used to apply the IJTAG test program to validate instrument execution, data collection and diagnostic resolution in preparation for manufacturing deployment. Once the functionality of the instruments operations and actions are validated, the project may be exported to manufacturing through the normal ScanWorks platform process.

# IJTAG TEST HARDWARE

ScanWorks come with a wide range of controllers on buses like PCI, PCIe, Ethernet, USB, PXI. The controllers typically support voltage levels from 0.8 to 3.3V (5V), TCK speed up to 50 MHz. All active controllers are Windows 32/64-bit compatible, and come with a number of digital IO channels for custom applications.



#### SCANWORKS PLATFORM FOR EMBEDDED INSTRUMENTS

ScanWorks Platform for Embedded Instruments is a seamless software environment to access, run and collect data from any instrument in your chips, circuit boards or systems. The ScanWorks Platform includes products for Boundary-Scan Test (BST), Processor-Controlled Test (PCT), High-Speed I/O (HSIO) Validation, FPGA-Controlled Test (FCT) and IJTAG test.

# **ASSET CONTACTS:**

Please contact your ScanWorks sales representative for more information.

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