ScanWorks®
Platform for Embedded Instruments

Boundary-Scan Test Input/Output IP (BST_IO IP) - FFP Instrument

Introduction

The Boundary-Scan Test Input/Output IP (BST_IO IP) instrument reduces the size of the Boundary-Scan Register within an FPGA, thus shortening the overall board Scan Chain. The BST_IO IP is used to significantly reduce erase, programming, and verify times of NOR/NAND, SPI, and I2C memory as compared to the same operations using the FPGA's entire boundary register.

The BST_IO IP is used within the ScanWorks® FPGA-based Fast Programming (FFP) Development software. When you select and configure the BST_IO IP instruments, ScanWorks® facilitates connectivity of them with other instruments of your choice and turns them into a cohesive, on-chip tester architecture. BST_IO IP is included with the FFP Development software. For more information about FFP and other FPGA-based Fast Programming Instrument IP from ASSET visit our website at: https://www.asset-intertech.com/products/fpga-fast programming.

Functional Description

Instantiation of a BST_IO IP instrument creates the equivalent of a JTAG test data register interface to user selected FPGA I/O pins and is accessed serially through the FPGA's built-in JTAG interface. The customization available in the instantiation of BST_IO instruments allows the user to create an interface specific connection from the target FPGA to the device under test, or device under programming. Multiple instantiations of the BST_IO IP can be created in the FPGA to facilitate interfaces to isolated pin groups and are connected in an IJTAG IEEE 1687 network for easy and effective access (Figure 1).
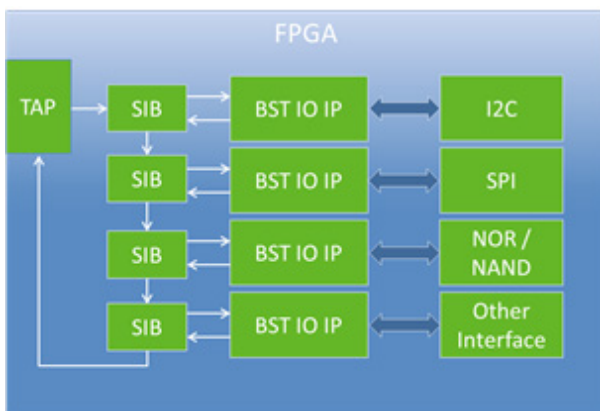

Figure 1: IJTAG IEEE 1687 Network

Embedded Tester Generator Configurable Parameters

The Embedded Tester Generator software will automatically wrap an IEEE 1687 network around the IP and guide you in the parameter setting, pin mapping, and synthesis processes. The following parameters can be set when synthesizing the IP into an FPGA.

Key Benefits:

- Program NOR/NAND/I2C devices with large amounts of data faster than standard boundary scan access methods

- Faster programming increases manufacturing through-put while reducing manufacturing cost

- In-system programming eliminates need for using pre-programmed parts or removing soldered parts for re-programming

- Can be combined with other structural and functional test as a part of the overall test sequence

Key Features:

- Creats JTAG register to pin interface

- Automatic insertion of Input/Output/Bidir/Control cells

- Seamless integration with ScanWorks Boundary-Scan Test programming actions

- Assign custom names/busses to FPGA pins

- Significant reduction in access time

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Configurable Parameters	
Name	**Description**
INPUT	Comma separated list of INPUT signal names. Use square brackets for bus range (e.g., addr[15:0]). Base signal name must match this regular expression /^[A-Za-z_][A-Za-z0-9_]+$/.
OUTPUT2	Comma separated list of OUTPUT2 signal names. Use square brackets for bus range (e.g., LED[3:0]). Base signal name must match this regular expression /^[A-Za-z_][A-Za-z0-9_]+$/.
OUTPUT3	Comma separated list of OUTPUT3 signal names. Specify signal busses with square brackets (e.g., LED[3:0]). Base signal name must match this regular expression /^[A-Za-z_][A-Za-z0-9_]+$/. Create OE groupings with curly braces (e.g., sig1, {sig2, sig3}, sig4). Signals that are not listed inside of curly braces will get their own OE.
BIDIR	Comma separated list of BIDIR signal names. Specify signal busses with square brackets (e.g., LED[3:0]). Base signal name must match this regular expression /^[A-Za-z_][A-Za-z0-9_]+$/. Create OE groupings with curly braces (e.g., sig1, {sig2, sig3}, sig4). Signals that are not listed inside of curly braces will get their own OE.

As seen in parameter descriptions in the above table, the I/O signal names to be pin-mapped when synthesizing each instance of the BST_IO IP into an FPGA are completely customizable by the end user. Here are some example values:

```
OUTPUT2: RW, LED[3:0]
OUTPUT3: cmd, {addr[15:0]}
BIDIR:   {data[31:0]}
```

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BST_IO IP Instrument

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