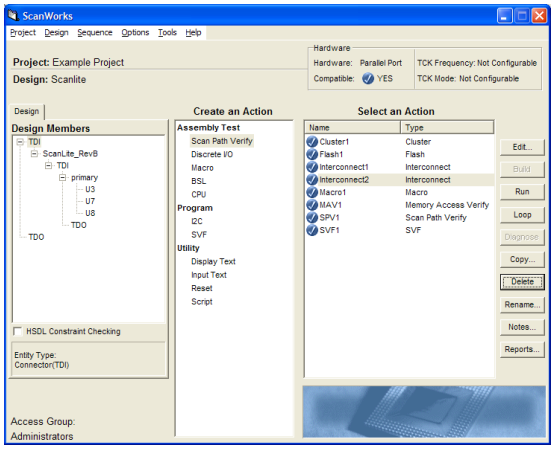
# SCANWORKS® BOUNDARY-SCAN TEST DIAGNOSTIC & REPAIR

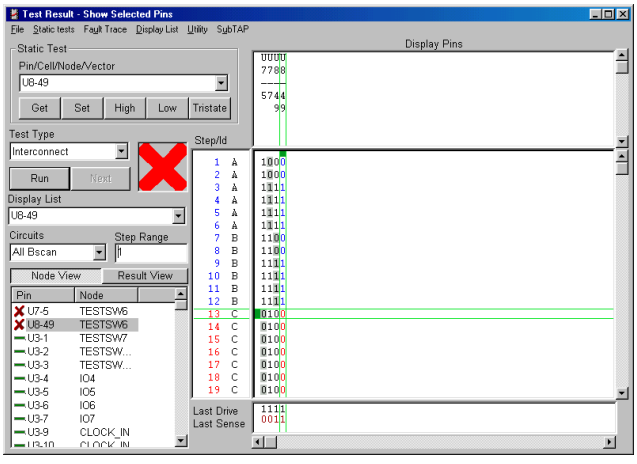
## OVERVIEW

ScanWorks Boundary- Scan Test (BST) Diagnostic & Repair software provides all the features necessary to quickly and easily diagnose and repair defects detected on boards during manufacturing. A separate repair station allows your development and manufacturing operations to continue uninterrupted while boards are repaired off-line. The Diagnostic & Repair software provides access to the built-in debug features of each test type but restricts the ability to modify designs or regenerate ScanWorks tests, protecting the integrity of the ScanWorks projects. Several of the major benefits of the Diagnostic & Repair software are:




- Project Management — Import and run the same tests used in manufacturing, using either the ScanWorks sequencer or a custom user interface
- Comprehensive test application — Apply and diagnose any test created with an BST Development software, including PLD and flash memory programming
- Consistent, intuitive user interface — Uses the same basic user interface as the BST Development software
- Maintain test integrity — By limiting access to test generation tools, you maintain safety of test and are assured the same tests are used for debug as were used for detection in manufacturing
- Quick defect isolation with pin-level diagnostics for interconnect test — Pin-level diagnostics to isolate a defect to the most likely device pin are included
- Graphical views of the board layout and schematic are linked directly from the fault reports, enabling you to quickly pin point the most likely location of the defect.

# DIAGNOSTICS

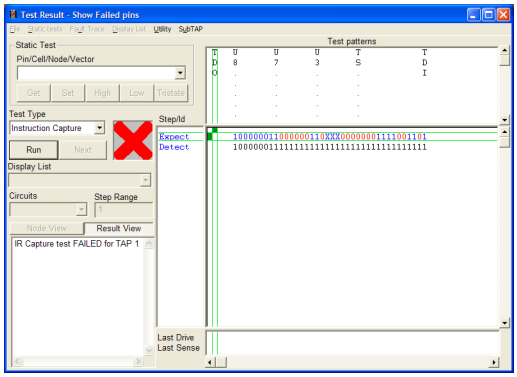



## SCAN PATH VERIFY DIAGNOSTICS

The boundary-scan design description used in ScanWorks is based on the IEEE 1149.1 standard Boundary-Scan Description Language (BSDL) files provided by the device vendors. The design management software imports these descriptions and creates a description of your design that includes all of the information needed to perform scan operations on the design. Once the design is described, tests to verify the design description against your actual board and tests to verify the scan path is actually working are automatically created.

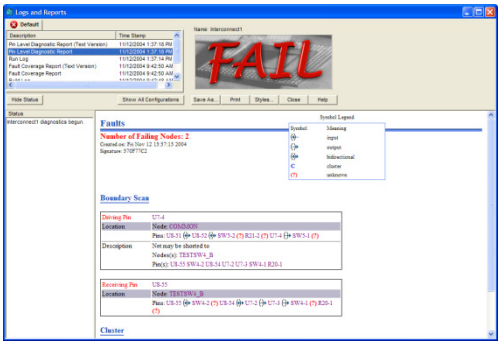
The full scan path verification generation dialog is provided to give the repair technician full access to the diagnostic features. Selecting or deselecting the optional tests enables the technician to quickly isolate scan path defects. Scan path verification tests include options to specify alternate Device IDCODES or USERCODES to support second source devices or different versions of the same device. A test results dialog is included to provide a sate table view of the actual response data during test application.

## INTERCONNECT TEST DIAGNOSTICS




Interconnect test diagnostic tools includes net- and pin-level diagnostic reports and a built-in test results dialog. The diagnostic report provides all the information available about any net on which an unexpected response is detected, including the most likely type of defect, (open or shorted) and the device and pin information about all other connections to the net.

The test results dialog provides a state table view of the results of applying interconnect tests. Each scan operation is shown for selected pins or nets, enabling you see exactly what conditions lead to miscompares. Miscompares are highlighted and the driving pins are clearly indicated. You can rerun the tests from within the test results dialog and also observe specific pins or set them to specific logic levels.

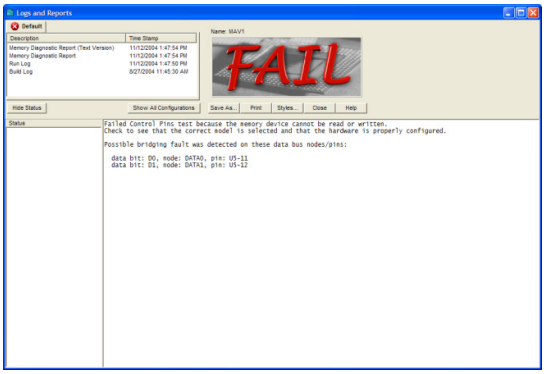



## INTERCONNECT PIN-LEVEL DIAGNOSTICS

The Diagnostic & Repair software includes diagnostics to the pin-level for interconnect tests. The report generated provides the type of fault detected, the most likely source of the fault, information about the net to which the pin is connected, and links to specific nets or pins in the design browser layout view. The report indicates the type of connection for each pin on the net using symbols to indicate input, output, or bi-directional and if the device is a cluster (non-boundary-scan), or unknown.

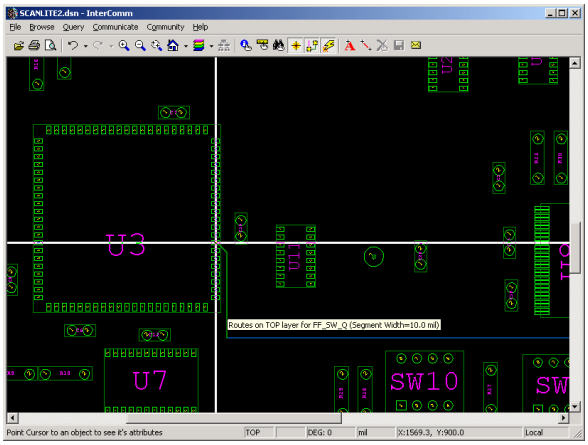
## MEMORY ACCESS VERIFICATION DIAGNOSTICS

Tests created with the memory access verification, feature found in the BST Development software, can detect defects on data, address and control signals connected between boundary-scan device and non-boundary-scan memory devices. Defects can be diagnosed to the data or address signal, and in some cases to a specific control signal. A diagnostic report that



indicates the signal and the specific memory pin involved is generated. Pins are linked to the board layout view provided by the graphical fault highlighting feature, making it easy to locate the suspected pin on the actual board being tested.

A test results dialog is also provided. Like the interconnect debugger, it provides a state table view of the scan operations needed to execute the read/write operations necessary to complete the test. Data is displayed in two modes: A cycle mode that shows only the significant scans for reading and writing to the memory and a vector mode that shows every scan.




## GRAPHICAL FAULT HIGHLIGHTING

The graphical fault highlighting feature gives you access to a graphical view of the board layout using the powerful design browser. Interconnect test and memory access verification test reports are linked to the layout view by clicking on a pin or net in the report. Cross hairs pinpoint the location of the pin or net in the layout view where the design browser gives you access to all the available information about that pin, and shows you the exact routing of the net connected to that pin. You can easily locate the suspected pin on the actual board being tested and quickly inspect it for obvious defects. You can cross-highlight the layout view to a schematic view to see the functional logic associated with the pin.

## SCANWORKS PLATFORM FOR EMBEDDED INSTRUMENTS

ScanWorks Platform for Embedded Instruments is a seamless software environment to access, run and collect data from any instrument in your chips, circuit boards or systems. The ScanWorks Platform includes products for Boundary-Scan Test (BST), Processor-Controlled Test (PCT), High-Speed I/O (HSIO) Validation, FPGA-Controlled Test (FCT) and IJTAG test.

## ASSET CONTACTS:

Please contact your ScanWorks sales representative for more information.

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