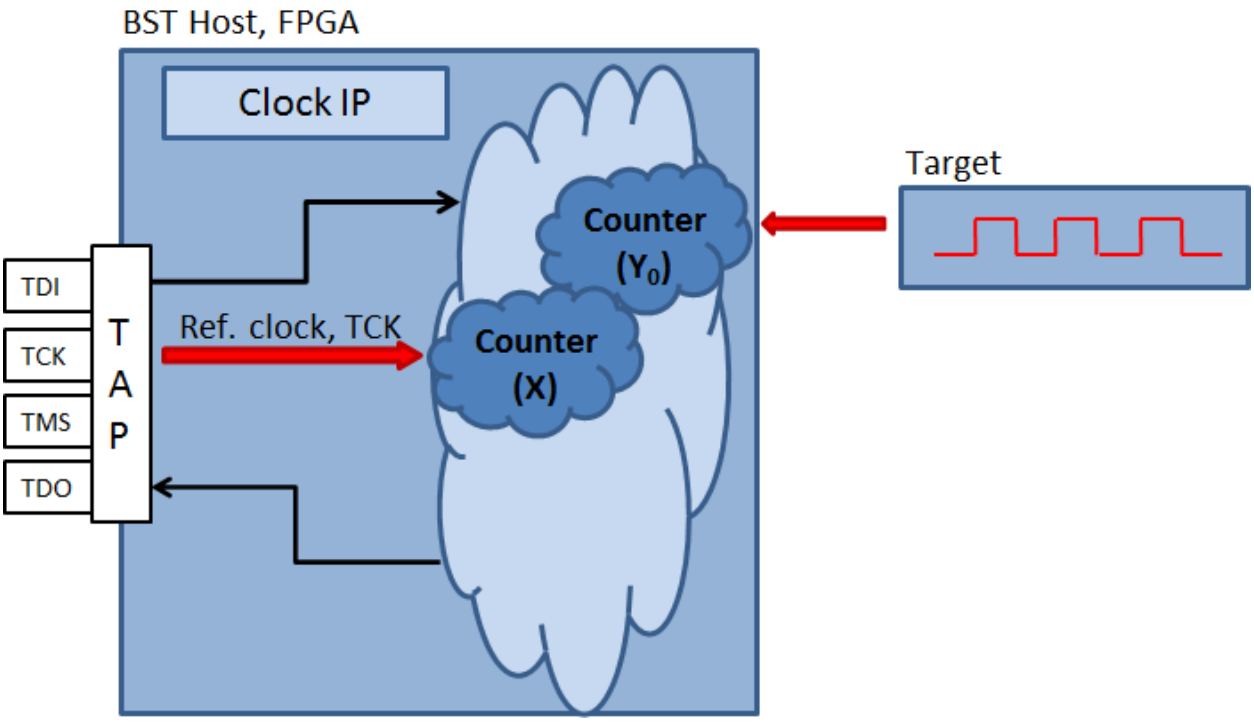
TESTING SYSTEM CLOCKS WITH BOUNDARY SCAN (JTAG) AND AN FPGA



BY KENT ZETTERBERG

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By Kent Zetterberg – Product Manager

Kent Zetterberg started his career in the automation industry, working with systems from ABB, Siemens and others. Following graduation from the University of Gävle with a Bachelor's of Science Degree in Computer Engineering, he worked 15 years in the telecom industry where he held various positions involving hardware test and debug. He joined Ericsson AB in Sweden in 1997 where he developed functional test programs for processor boards, and designed interface boards and test fixtures. At Ericsson he became an expert in boundary scan and eventually led the boundary scan team. With ASSET Kent has held several positions in support, serving as a customer trainer and European support team leader. Currently he is the technical product manager for ScanWorks boundary-scan test products.

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Executive Summary

System clocks are fundamental to booting prototypes of a printed circuit board (PCB) design or fully assembled boards on the manufacturing line. Faulty clock operations will simply prevent processors, chipsets, ASICS, FPGAs and all other functional devices from bringing up their respective operational states, the operating system or the system's firmware environment. In addition, the expectations of very high speeds, data transfer rates and throughput rates from so many systems today only increases the criticality of fully functional system clocks.

As a result, savvy engineers will often seek to quickly rule out faulty system clocks from their list of possible causes for non-booting prototypes or assembled PCBs. By functionally verifying the clocks first or relatively early on in the test sequence, the engineer can reduce the time needed to bring up prototypes and allow adequate time for more robust functional testing during manufacturing.

The question then becomes which methodology is most cost-effective for verifying that the system clocks are functional? The emergence of non-intrusive board test methods employing instrumentation embedded in the chips on the circuit boards that are being tested has presented engineers with an abundance of new and less costly alternatives. Now, engineers should ask themselves:

- Is that expensive oscilloscope, frequency counter or logic analyzer really needed or are there more cost-effective methods for verifying system clocks?
- Can I replace legacy methodologies requiring expensive capital equipment and external instrumentation with much less costly non-intrusive, software-driven embedded instrumentation methods, such as boundary-scan test (IEEE 1149.1 JTAG)?
- What will be the cost savings if the number of test points on PCBs is reduced and the nails on complex probe-based test fixture slashed by transitioning to non-intrusive probe-less test methods?

This eBook explains how system clocks on PCBs can be quickly verified with simple and cost-effective, yet powerful and precise methods based on non-intrusive embedded instrumentation.

Testing a Clock without Probes

Structural boundary-scan test (BST) tools (based on the IEEE 1149.1 Boundary-Scan Standard and commonly referred to as JTAG) provide an effective, probe-less, non-intrusive way to verify that the clocks on a circuit board are functional. In addition, embedded instrumentation intellectual property (IP) could be loaded into an FPGA on the board design to the measure clock frequencies. Measuring frequencies with this method will in most cases provide enough confidence that the clocks are running at the right frequencies. This eBook discusses several methods for testing system clocks with boundary scan or by combining boundary scan with an FPGA-based IP embedded instrument for measuring clock frequencies. These methods are based on the assumption that the system clocks are connected to a boundary-scan pin with an input cell. For more information about boundary-scan, IEEE 1149.1, also known as JTAG, go to the ASSET InterTech website and look under the eResources.

Testing a Clock via the Boundary Scan Chain

When a clock is connected to an input pin on a device with boundary-scan resources on-chip (Figure 1), the device's clock input can be sampled and then scanned out of the device by way of its boundary-scan Test Access Port (TAP). If the clock is not running, a static value will be scanned out. If the clock is running and an adequate sample of clock inputs is captured and scanned out, then the clock input values can be read as either the high or the low side of the clock signal. Based on this data, one can determine whether the clock is functional or not.

If the clock is stuck-high, or stuck-low, a capable boundary-scan tool will be able to detect the stuck-at value. It should be noted that the frequency at which the clock input samples can be scanned out of the boundary-scan device will depend on the boundary-scan Test Clock (TCK) and the length of the scan chain on the circuit board. As a result, this method will typically not calculate the frequency of the clock.

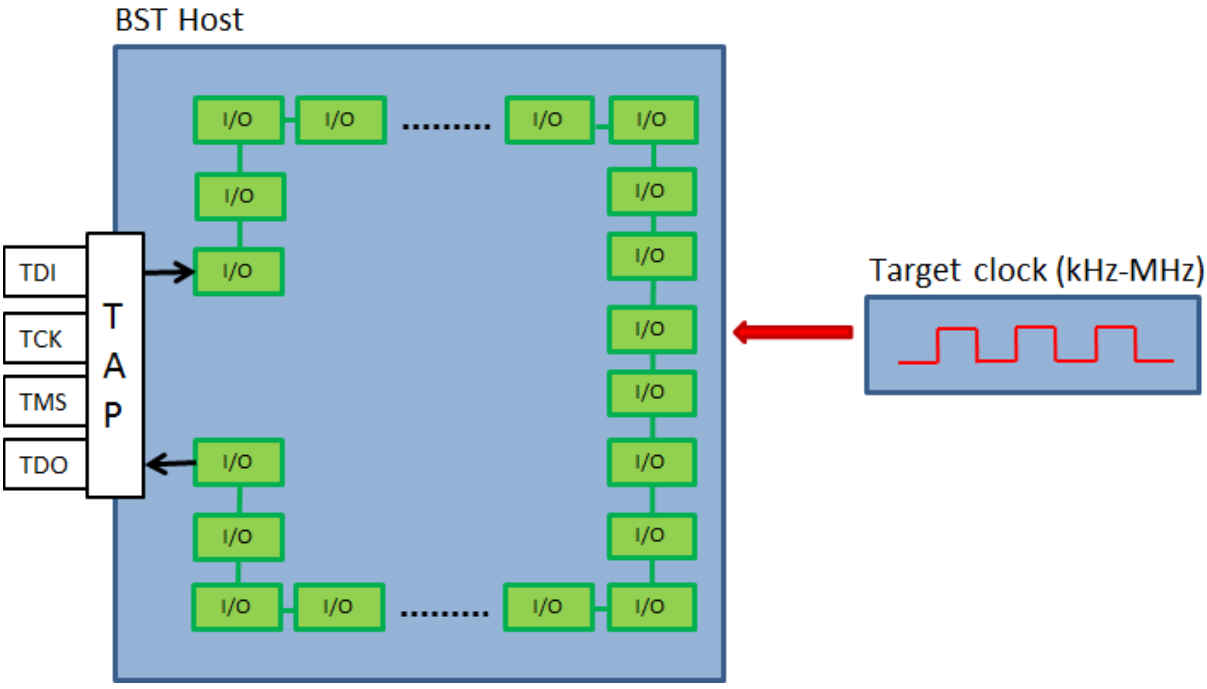


Figure 1: Testing a clock via a boundary scan chain

The boundary-scan chain method is best suited for determining whether clocks are functional at all and for detecting any stuck-at problems on the clock nets.

Testing Clocks with an FPGA IP Instrument and a System Clock Reference

If the system clocks are connected to an FPGA, their frequencies can be measured by an IP instrument embedded into the FPGA (Figure 2). In some cases, this can be accomplished by boundary-scan tools. To calculate a clock's frequency, the measuring instrument must have access to a reference clock that is running at a known frequency. One way, and perhaps the most flexible way, to measure clock frequencies with this method is to program two counters into the FPGA. Over a certain time period, one of the counters will count transitions on the reference clock while the other monitors transitions on the clock that is being measured. The time period for the measurements can be set through the reference clock counter and defined as a certain number of transitions of the reference clock. The counters are started simultaneously and stopped at the expiration of the measurement period.

The frequency of the measured clock is then calculated by dividing the sampled frequencies of each clock by the other and since the reference clock has a known frequency, the frequency of

the measured clock can be calculated. The accuracy of the calculated speed of the measured clock will depend on the speed of both the reference and the measured clocks. For example, the reference clock is a 1 MHz clock and the clock that's being measured is supposed to be a 32 kHz clock. If a measurement window of one million cycles on the reference is established and the measure time is one second, then the counter should count 32,000 cycles (plus or minus one cycle, depending on where in a cycle the measurement window begins and ends). This would verify that the clock in question is indeed a 32 kHz clock.

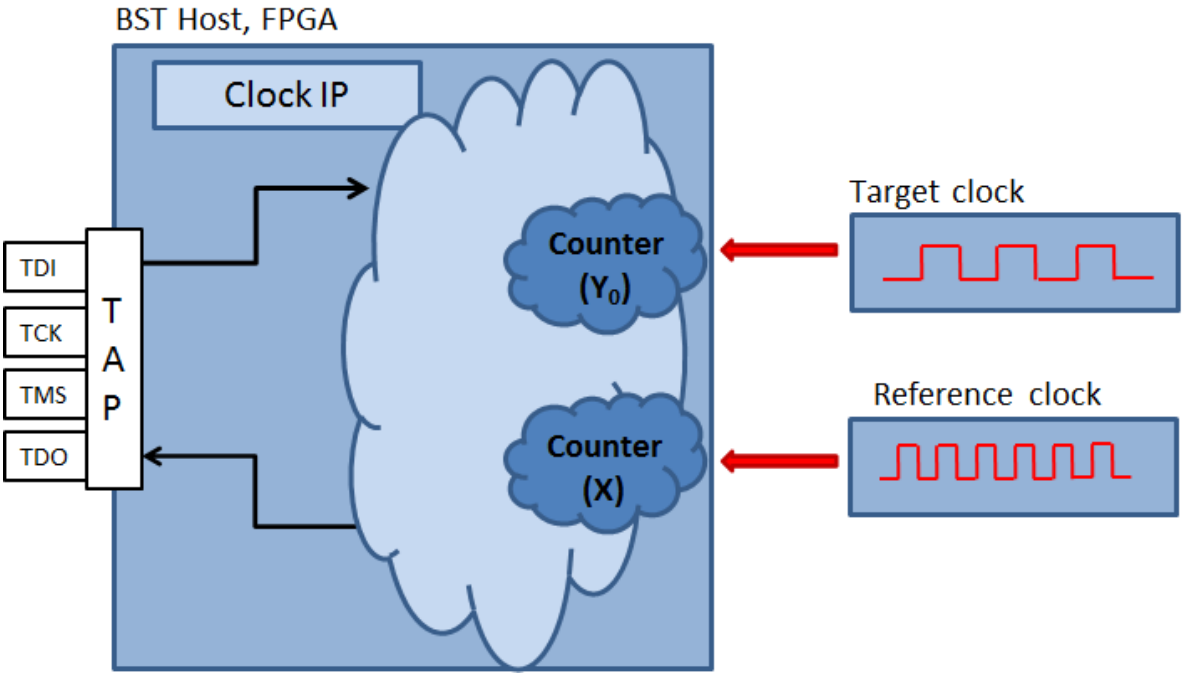


Figure 2: Testing clocks with an FPGA IP instrument and system clock reference

This method is only applicable when a known good reference clock is present. In addition, it is not precise, insofar as it will only provide a certain level of confidence that the clocks are functional and that the frequency of each clock is in the correct or expected order of magnitude. Depending on the IP instrument embedded in the FPGA, more than one clock can be measured at the same time, saving production time.

Testing Clocks with an FPGA IP Instrument and TCK as a Reference

The most effective way to measure a clock's speed is with an external reference clock. When boundary scan is present and boundary-scan tools are available, the TCK clock is always

available as a reference clock to measure system clocks (Figure 3). In most cases, the boundary-scan clock is free-running and stable. With TCK as the reference any system clock can be measured by the same means as described in the previous method. As above, the first step is to establish a measurement window by defining the number of TCK transitions which should comprise the time period when measurements are gathered. The IP instrument embedded in the FPGA will require as an input the frequency of the TCK. With this, measuring the target clock and reporting its approximate frequency to the boundary-scan tool can commence.

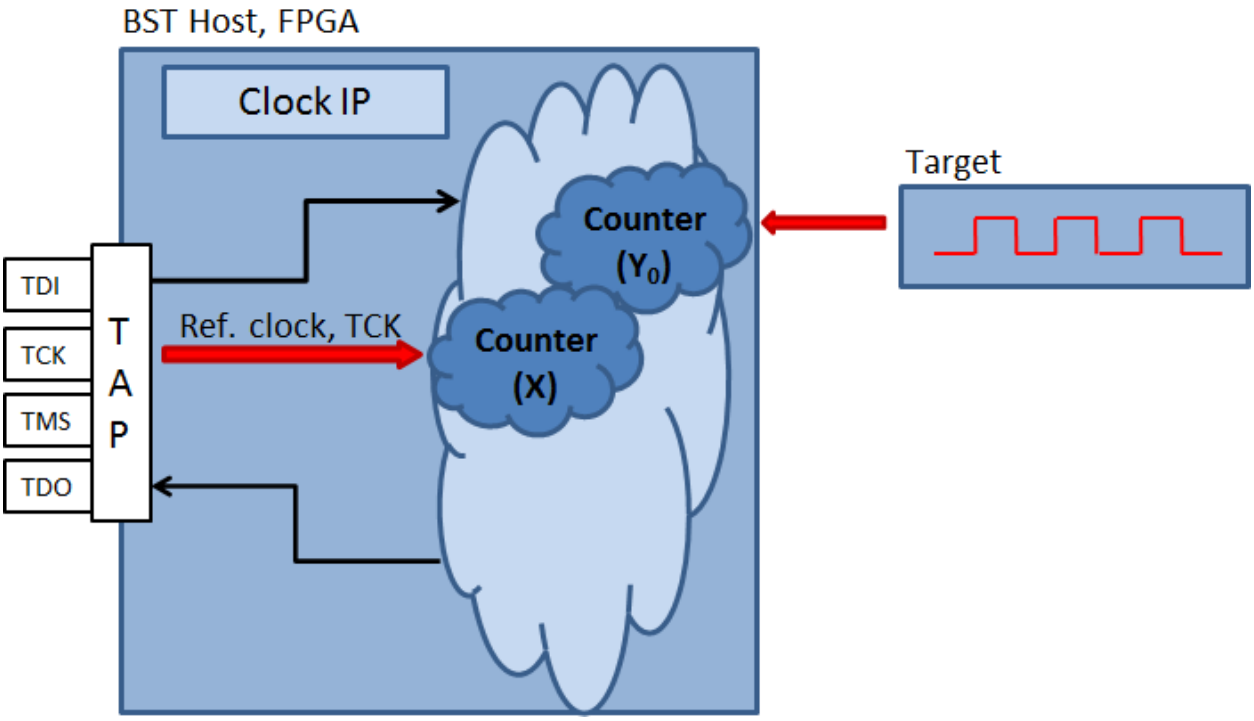


Figure 3: Testing clocks with an FPGA IP instrument and TCK as a reference

This method requires a free-running and stable TCK reference clock that can be made available internally in the FPGA for use by the IP instrument. In addition, this way of testing the clock is not precise, insofar as it will only provide a certain level of confidence that the clocks are functional and that the frequency of each clock is in the correct or expected order of magnitude. Depending on the IP instrument embedded in the FPGA, more than one clock can be measured at the same time, saving production time.

Testing Duty Cycle of slow clocks via the Boundary-Scan Chain

For slow clocks like the 1-PPS (pulse per second) clock commonly deployed in the telecom industry, duty cycles can be verified with boundary-scan test methods (Figure 4). The accuracy of this method will only be in the millisecond range. This is not a highly accurate validation tool, but it is a rather low-cost alternative that will yield a relatively high level of confidence that the clock is running at approximately the right speed and duty cycle. Measurements are taken by sampling a clock input on a boundary-scan chip. When an edge of the clock signal is found, a timer in boundary-scan tool running on an attached host PC is kicked off. Then the timer value is captured at the next two edges, thereby capturing a full duty cycle period. An approximate duty cycle can be calculated from the timer values at each edge of the clock signal.

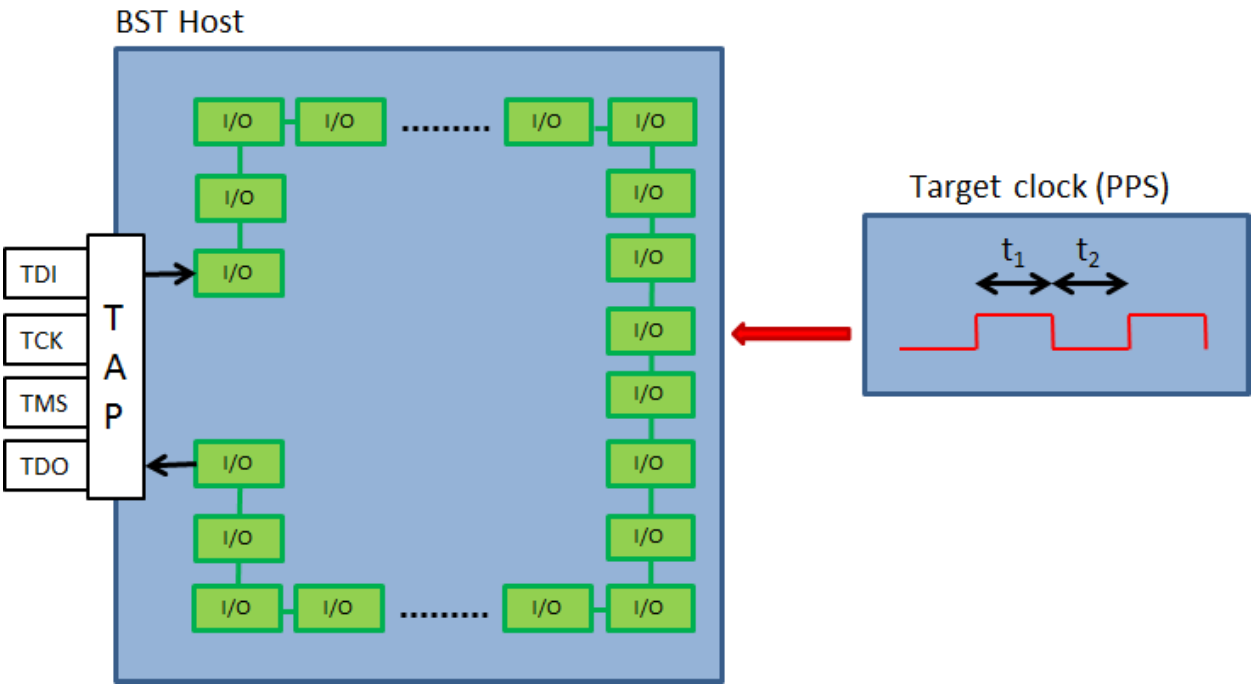


Figure 4: Testing the duty cycle of slow clocks via the boundary scan chain

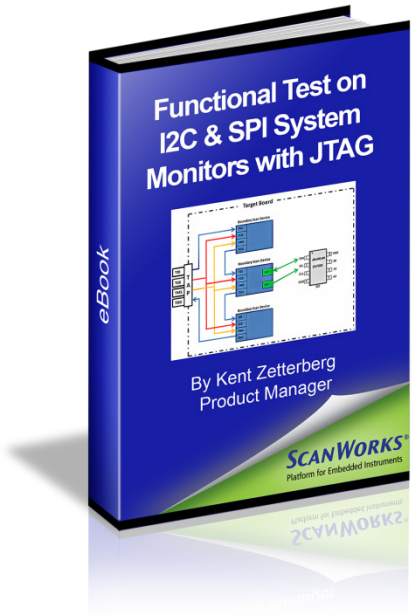
This method should be used for functional confidence verification, and not functional device validation or characterization. It provides a very cost-effective, but low resolution test alternative to highly priced capital equipment that is otherwise often employed.

Conclusions

Expensive and cumbersome oscilloscopes, frequency counters and logic analyzes that rely on probing PCBs are no longer the most cost-effective or efficient means for testing system clock frequencies. Probe-free, non-intrusive test methods can take advantage of instrumentation embedded in the chips on the PCBs to test clocks early in the prototype board bring-up phase just prior to transitioning a design into manufacturing or during volume manufacturing.

Learn More

In addition to testing system clocks, maybe you would like to configure and setup PLLs over the SPI or I2C buses but don't have an operating system yet. Fortunately, with boundary scan on a well-designed FPGA circuit board you can. Check out this eBook to find out how.



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