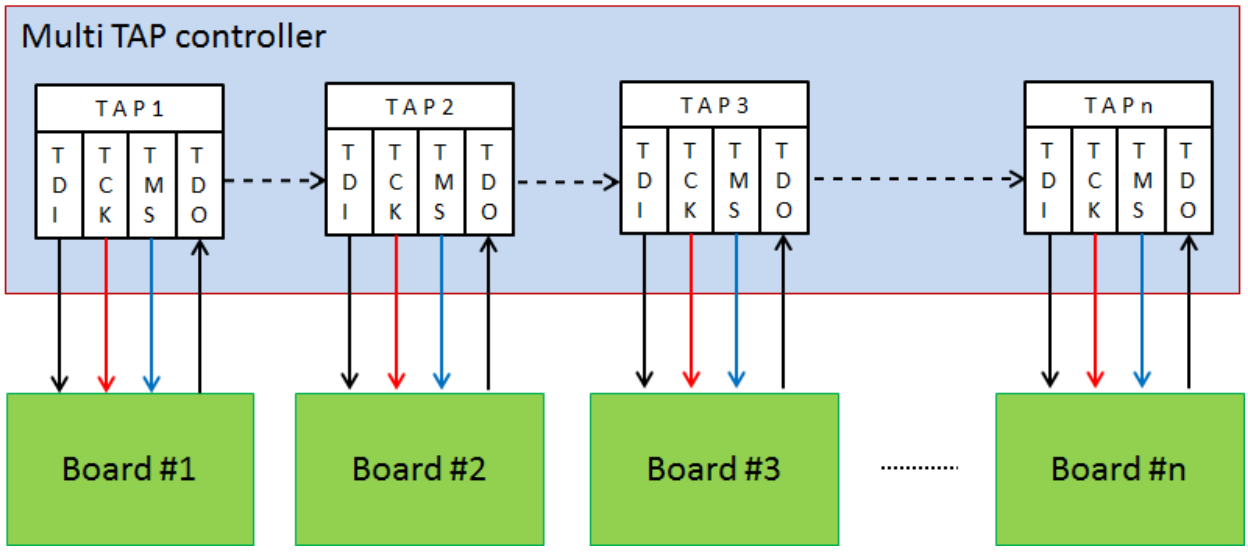
# System Test with Boundary Scan (JTAG)




By Kent Zetterberg

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# JTAG and System Test

*By Kent Zetterberg – ScanWorks BST Product Manager*

Kent Zetterberg started his career in the automation industry, working with systems from ABB, Siemens and others. Following graduation from the University of Gävle with a Bachelor's of Science Degree in Computer Engineering, he worked 15 years in the telecom industry where he held various positions involving hardware test and debug. He joined Ericsson AB in Sweden in 1997 where he developed functional test programs for processor boards, and designed interface boards and test fixtures. At Ericsson he became an expert in boundary scan and eventually led the boundary scan team. With ASSET Kent has held several positions in support, serving as a customer trainer and European support team leader. Currently he is the technical product manager for ScanWorks boundary-scan test products.



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## Executive Summary

The boundary-scan family of standards – IEEE 1149.1/6/7 and also referred to as JTAG after the Joint Test Action Group – is most often thought of as a board-level test method, but new hardware and software techniques make system-level test with boundary scan not only feasible, but quite effective. In fact, system-level tests with boundary scan can save a significant amount of time and effort troubleshooting systems that have failed functional test. Ultimately, boundary-scan system tests ensure a high-quality system.

Many different types of faults can arise when systems are assembled. JTAG testing techniques are well suited to finding and diagnosing many of these problems. In addition, the usefulness of boundary scan at the system level extends well beyond what is usually thought of as test functions. Besides structural integrity tests internal to the boards and even between boards in a system, boundary scan (JTAG) can also perform on-board programming of NOR and NAND flash memory, in-system configuration of programmable logic devices (PLDs) and field programmable gate arrays (FPGAs), on-board programming of I2C and SPI EEPROM memories and emulated functional testing of devices like DDR2, DDR3, SPI, I2C, UART, Ethernet, USB and others through the boundary-scan register of associated devices.

Some, if not all, of these test functions can be re-used throughout a product's life cycle, beginning in design, moving into manufacturing and eventually in systems installed in the marketplace. Boundary-scan system tests can be very helpful to support and maintenance personnel long after a system has been assembled in a manufacturing environment and deployed at a user location. Boundary-scan system tests can be developed in a matter of hours with model-based boundary-scan tools to provide fault diagnostic and programming solutions for the most common challenges faced by the design, manufacturing and support departments at system suppliers.

## What is system test and why would you want to do it?

For the purposes of this discussion, system will mean more than one printed circuit board or subassembly connected together. This could be a system assembly as simple as a motherboard with daughtercard or an extremely complex backplane-based computer with hundreds of boards. So, an electronic system is a group of interrelated devices, circuit boards and subassemblies that function together to accomplish a task. Although the components that comprise an electronic system may be tested individually without regard to the task of the entire system, the overarching goal of system test is to verify the structural integrity and/or functionality at the level of the complex whole. At a fundamental level, testing a system's structural integrity would involve verifying that each component is properly connected to all other components that require such connections.

## Why System Test?

Most electronic products can be seen as a system. Even if all of the system's components are fully tested individually, the system still may not function properly. Many problems can arise when systems are assembled. Boundary-scan testing procedures are well suited to finding and diagnosing these problems. For example, a connector may not be making good electrical contact or the connector's pins might have been damaged during assembly. Boards on a backplane may be missing, out of place or simply not functioning properly. Functional tests might identify that the system is not functioning as expected, but isolating and diagnosing the fault with functional tests would be very time consuming and often would require high-level system expertise to troubleshoot the cause.

In addition, the usefulness of boundary scan/JTAG at the system level extends well beyond what is usually thought of as test functions. Besides structural integrity tests, boundary scan can also perform on-board programming of NOR and NAND flash memory, in-system configuration of programmable logic devices (PLDs) and field programmable gate arrays (FPGAs), on-board programming of I2C and SPI EEPROMs and emulated functional testing through the boundary-scan register of devices like DDR2, DDR3, SPI, I2C, UART, Ethernet, USB and others.

Beginning with system-level debug and production test, boundary scan provides many other system benefits when it is extended to field support. For example, boundary scan can be used for quick and easy updates to programs stored in flash memory or updates to system functionality by reconfiguring on-board devices after the system has been installed in the field.

## How is system test implemented with boundary-scan?

All four of the primary methods for implementing boundary-scan-based system tests involve connecting an external boundary-scan test tool to the system.

The first external method connects all of the boundary-scan paths on all of the boards in the system to a single scan path with one point of access for the boundary-scan test system (Figure 1). This method requires that the configuration of the system must be exactly the same in every assembled product. Also, any break in the single scan path will disable all boundary-scan test access. One very long scan path can also result in slow access times.

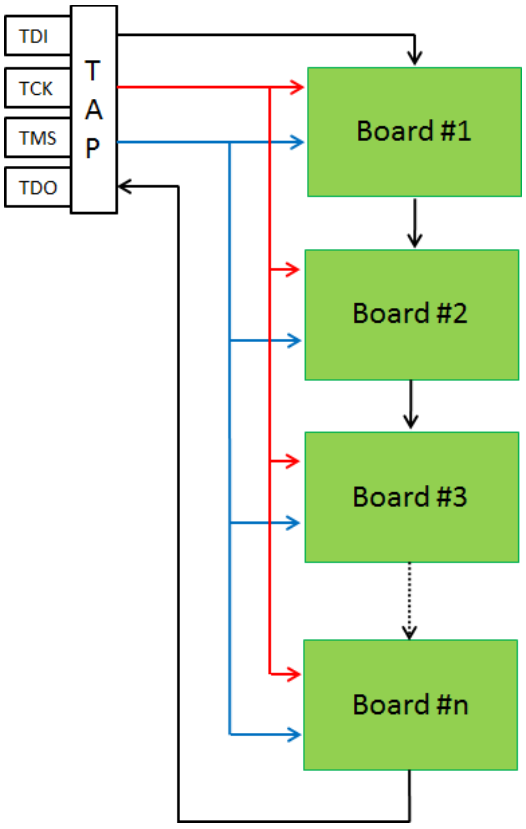


**Figure 1: Single Scan Path**



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The second external method is to link each scan path in the system to external connectors where the boundary-scan tool will have access to all scan paths (Figure 2). With this method, physical access to each JTAG connector must be available when the system is operating. Additional test system hardware is also needed to connect the test system and the system-under-test. However, with this method, the configuration of the system can change and the test system is able to manage test access for each new or different configuration of the system. Also, systems that were not designed with system-level testing in mind may still be tested with this method.

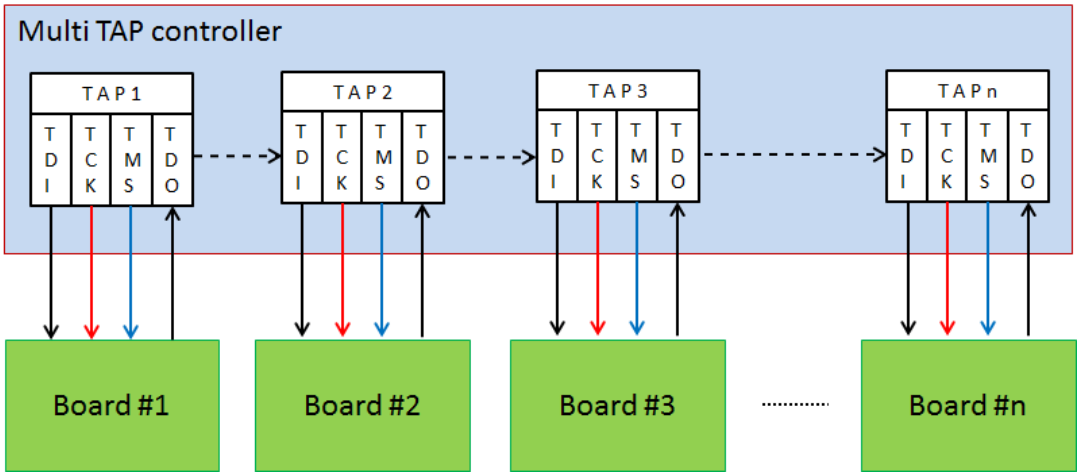


**Figure 2: Multiple Scan Paths/Multiple Access Points**

The third method involves accessing the scan paths on the individual boards from one external JTAG port (Figure 3). This is most commonly accomplished with multidrop gateway devices that control the board for the purposes of testing the system. These gateway devices typically are controlled by the test system. They can be mounted on each board or on the backplane where the boards are installed. If installed on-board, gateway devices will require board real estate. In any event, they will add to the cost of the system. Also, distinct tests must be developed for each configuration of the system.



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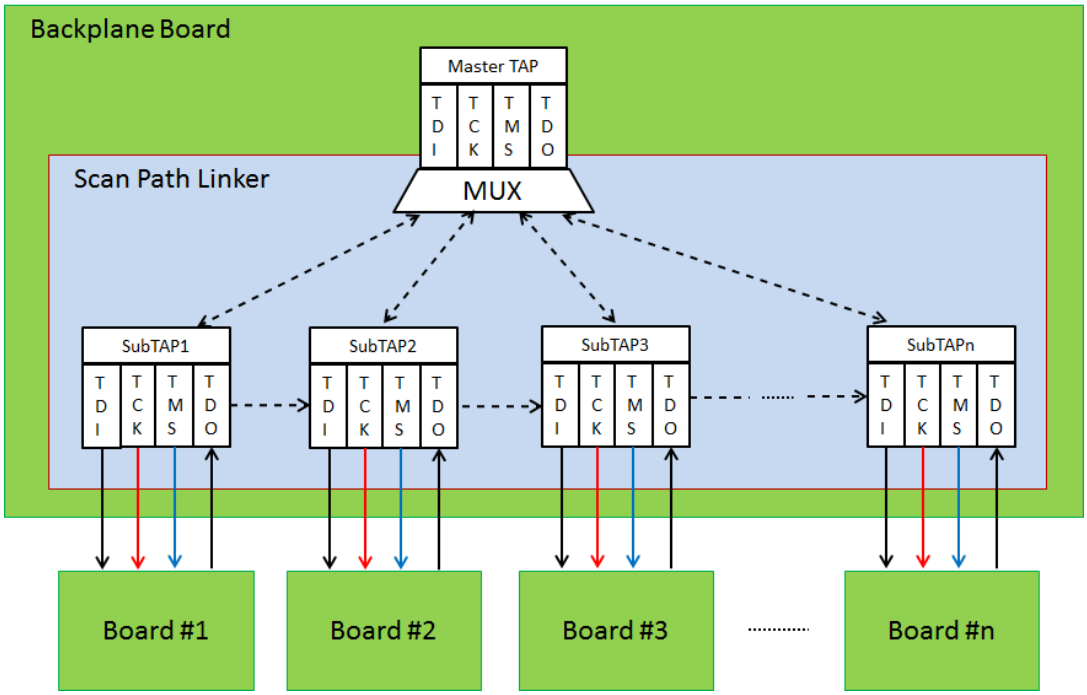


**Figure 3: Multiple Paths/One-Access Point**

A fourth method would be for the development team to design boundary-scan access into the system by way of a break-out board, buffer board, concatenation board or some combination of the three that would incorporate custom switch matrix logic onboard allowing to concatenating the scan chains of the boards under test (Figure 4). Advanced concatenation boards can multiplex the boundary-scan Test Access Port (TAP) signals from the connected boundary-scan test system and target one board at the time in the unit-under-test (UUT), or two or more UUTs could be concatenated so that cross-backplane testing could be performed similarly to method two. Selection of active TAP ports are commonly made by external digital I/O (DIO) signals on the boundary-scan controller, or, in the case where the concatenation is made by an addressable scan port device (ASP), SCAN Bridge or a gateway device, the boundary-scan test system will address devices and set up its sub-paths automatically.



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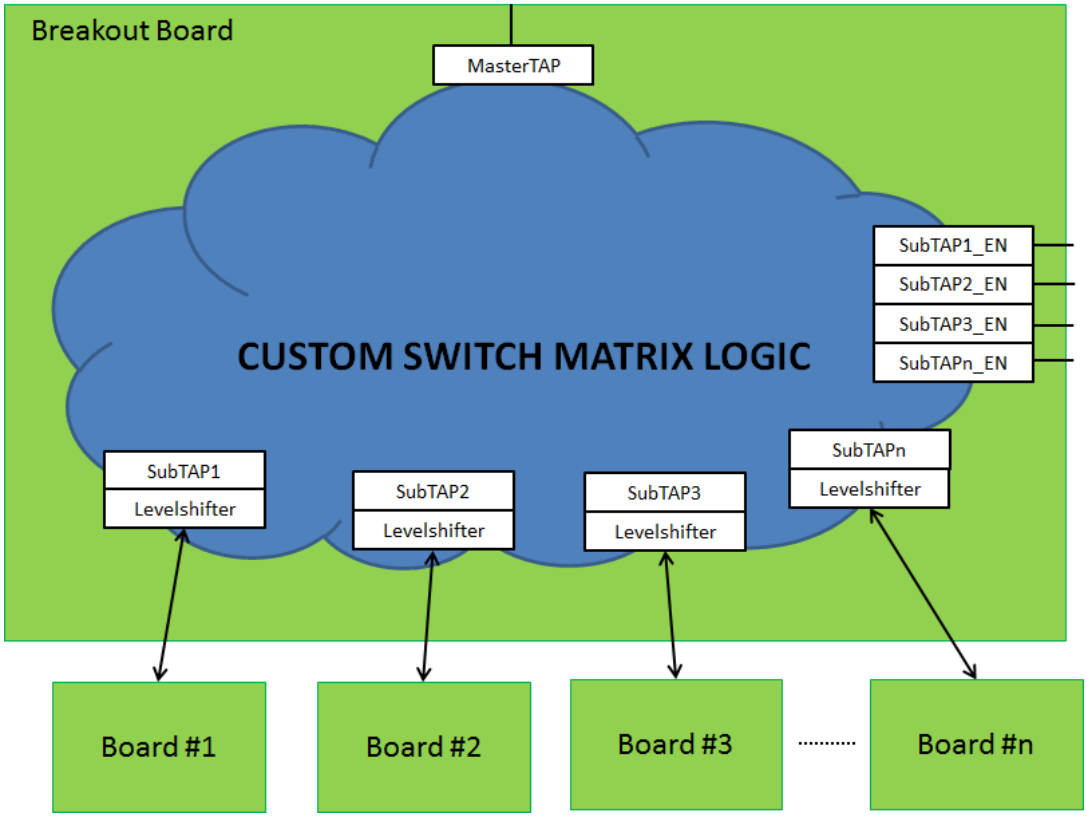


**Figure 4: Custom designed breakout board**

The table below provides a summary of the advantages and disadvantages of the three external and one designed-in boundary-scan system test methods.

**Table 1: Advantages and Disadvantages of Various System Test Methods**

| Implementation Method | Advantages | Disadvantages |
|---|---|---|
| One path per system / one access point | Simple, single point of access | System configuration must never change. One break in the scan chain will disable all boundary-scan operations. Slow access times. |
| Multiple paths per system / separate access to each scan path | Tests can adapt to changes in the system's configuration. Already-designed systems can be retrofitted with boundary-scan system tests. | Physical access to each path needed. Additional hardware needed to connect system-under-test and test system. |
| Multiple paths per system / one control point per board | Tests are controlled by multi-drop gateway devices. Straightforward interface with test system. | Gateway devices require board or backplane space and add to the cost of the system. Each system configuration requires its own test suite. |
| Multiple paths per system / access though breakout board, concatenation board, etc. | Flexible system where the break-out board can adapt and concatenate different JTAG port standards. | Breakout boards for complex architectures can grow in size and complexity. |



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## Boundary-scan access to each system component

Many boards that are well designed for board-level boundary-scan test are often easily integrated into system-level test processes that use boundary scan. However, several restrictions must be overcome to build on board-level boundary scan and achieve effective system test. These restrictions include the following:

1. The JTAG connector on each board must be accessible when the boards are installed in a system.
2. The system must be able to operate with a boundary-scan test system connected to each board or UUT. (For example, connecting each board to a boundary-scan test system may require removing the enclosure or cabinet covers and this may affect the system's cooling.)
3. The boundary-scan tool must be capable of managing several scan paths and generating tests for the connections between the boards.
4. A system-level net list is required to generate interconnect tests between boards.

Most boundary-scan test tools support system-level boundary-scan operations with hardware that connects to multiple scan paths and software that manages the access to those scan paths. Each scan path can be accessed individually or scan paths can be concatenated together in groups to enable interconnect testing among the boards in a system.

## System Test with Multidrop Devices

Multidrop gateway devices on the boards in a system can also be used for system-level tests. In this case, the multidrop devices would control access to one or more scan paths on a board, providing access for these multiple paths to a primary source for the boundary-scan TAP signals. The boundary-scan tool connected to the primary TAP on a board sends commands to the multidrop device, configuring it for test operations. Multidrop devices use either of two methods for communicating with the boundary-scan tool.

1. The boundary-scan tool uses the standard IEEE 1149.1 protocol to write data to registers internal to a multidrop device. The contents of these registers determine which of the multiple scan paths controlled by the device will be active. Each active path is included in

the overall scan path along with the board's primary scan path. If more than one multidrop device is present on the primary scan path, the tool must be able to target each multidrop device.

2. The boundary-scan tool uses a proprietary protocol to place a command on the primary TAP signals. Each multidrop device on the primary scan path examines the command to determine for which multidrop device it is intended. These commands will open or close one or more secondary scan paths, adding or removing them from the overall scan path that is connected to the boundary-scan tool. The boundary-scan tool must always know the exact configuration of the scan path before any scan operation can be executed. The following are some of the major, commercially available multidrop gateway devices:

Texas Instruments

- Scan Path Linker (SPL) – SN54ACT8997
- Addressable Scan Port (ASP) - SN54ABT8996
- Linking Addressable Scan Port (LASP) – SN54LVT8986
- SCAN Bridge (SCANSTA111, SCANSTA112)

Firecron (Alliance Semiconductor)

- Gateway (JTSxx, JTLxx, JTXxx)

Lattice Semiconductor

- BSCAN2 (Multiple Scan Port Linker)

Boundary-scan operations are usually based on a design description. This design description is built from the BSDL files for the devices in the design and from information describing how the devices are connected together in scan paths. Scan paths on a board can be permanent or they may be reconfigured dynamically by way of commands sent to multidrop devices in the design. Some boundary-scan tools retain the status of the scan path configuration so that it always knows the exact makeup of the scan chain or chains.

There are several methods for controlling multidrop devices and the secondary scan paths associated with them. In some cases, a certain scan path configuration may be needed for several



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test operations. Or, the scan path may be dynamically reconfigured before a boundary-scan action can be applied. In either case, the devices in a design maintain a particular scan path configuration until it is explicitly changed by the boundary-scan tool or until a JTAG Test Logic/Reset operation occurs. Many boundary-scan tools will define the system's preconditions that prepare the board or system for the application of the tests or programming operations that comprise the action. This precondition is applied to the board or system before the scan operations are applied. Preconditions also communicate the configuration of the scan path to the test pattern generation tool before it generates test vectors. In this way, the boundary-scan tool can ensure that the test vectors it creates are the required vectors for the current configuration of the scan path.



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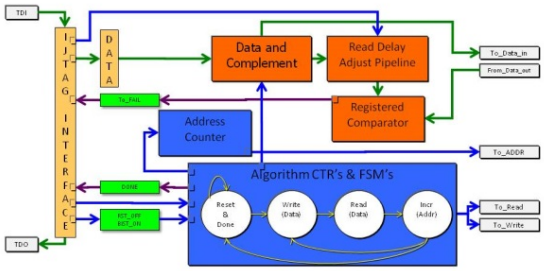
## Considering System Test

Over the course of the last decade, boundary scan has established a firm foothold at the level of board test, but it also plays a critical function at the system level. Indeed, as more board-level boundary-scan tests and programming operations are developed and deployed, the feasibility of implementing system-level boundary-scan operations increases because the developmental work done for individual boards can be leveraged against system-level objectives. Moreover, any additional effort to implement boundary-scan test operations at the system level is merely marginal when boundary-scan tests have already been deployed at the board level. The board-level infrastructure is already in place for system-level boundary-scan tests. As a result, the payback for system-level boundary scan can be quite rapid because of the limited amount of development time required to implement system-level boundary-scan test as an add-on to board-level boundary-scan operations.

## Learn More

*Learn more about how boundary scan and other non-intrusive test technologies can test high-speed memories like DDR3 devices.*

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