SIGNAL INTEGRITY VALIDATION FOR INTEL® XEON® PLATFORMS

PART 1

The signal integrity on high-speed I/O and memory buses is critically important because of its effects on design margins on all electronic products. For example, on Intel® Xeon® platforms, which are used in server, storage, telecom and high-end gaming machines, poor operating margins can lead to uncorrectable errors or system crashes, costly field repairs and even product recalls. A design with good signal integrity will perform at its potential; at best, a design that fails to stay within its operating margins because of poor signal integrity will perform at a lower level than expected or required.

Performing signal integrity validation with traditional high-end capital equipment such as oscilloscopes is a very expensive proposition. Fortunately, Intel® Interconnect Built-In Self Test (Intel® IBIST) technology now allows designers to simply, effectively and inexpensively margin their designs through a wide range of process/voltage/temperature (PVT) variables without employing an oscilloscope. This new '5x5' approach (5 runs on 5 systems) allows OEMs and ODMs to hit the sweet spot between not enough testing, which can result in field repairs, warranty replacements and lost customers, and too much testing, which is overly expensive, resulting in lost profit, reduced sales and could lead to missing a market window (Figure 1).

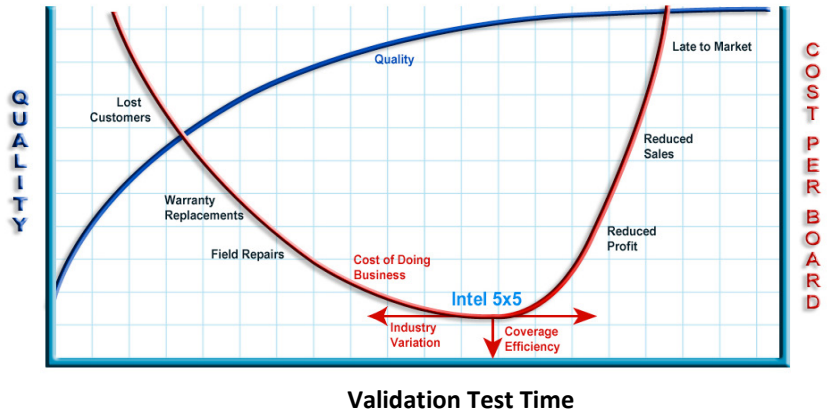

Figure 1 : Validation tradeoffs

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This new validation procedure is the result of collaboration between Intel® and ASSET®, and utilizes ASSET's High-Speed I/O (HSIO) toolkit; part of the ScanWorks® platform for embedded instruments. For more information on how to implement this economical '5x5' validation procedure and increase confidence in system margins within the server, storage, telecom and other Intel Xeon markets, access the documents referenced below that can be found on the Intel® Business Link site.

For assistance with your validation needs, and to verify that this validation methodology applies to your Xeon design, please contact your ASSET representative, or register for Part 2 of this document below.

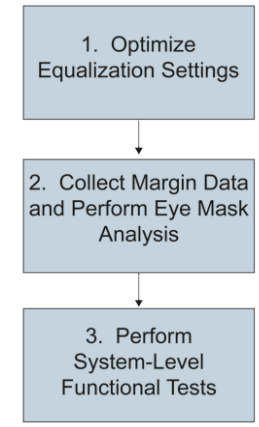
References

IBL document #456593, *Intel QuickPath Interconnect, CPU Rx PCIe* 3.0, and DMI2 Recommended Validation Procedure, September 2012*

IBL document #487010, *DDR Methodology for ASSET InterTech Inc's ScanWorks High-Speed I/O (HSIO) for IA Tool, October 2011*

Learn More

Learn more about the 5x5 methodology by registering for our technical paper, "**Signal Integrity Validation Procedure for Intel® Xeon® Platforms – An HSIO White Paper**".



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