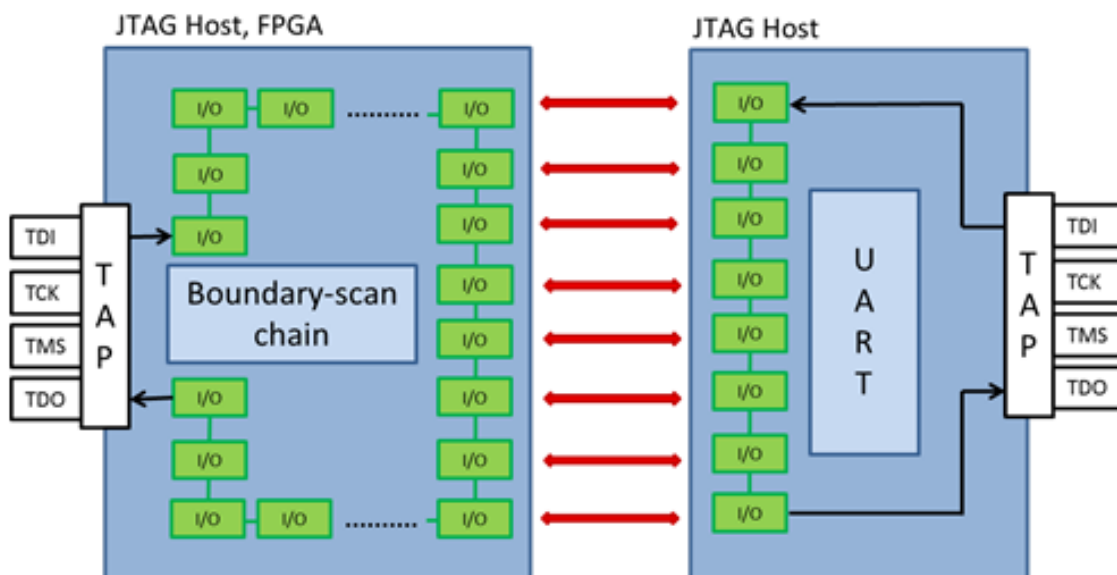


# SERIAL PORT FUNCTIONAL TEST WITH FPGA UART IP AND JTAG



**EBOOK**

**BY KENT ZETTERBERG**

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Kent Zetterberg started his career in the automation industry, working with systems from ABB, Siemens and others. Following graduation from the University of Gävle with a Bachelor's of Science Degree in Computer Engineering, he worked 15 years in the telecom industry where he held various positions involving hardware test and debug. He joined Ericsson AB in Sweden in 1997 where he developed functional test programs for processor boards, and designed interface boards and test fixtures. At Ericsson he became an expert in boundary scan and eventually led the boundary scan team. With ASSET Kent has held several positions in support, serving as a customer trainer and European support team leader. Currently he is the technical product manager for ScanWorks boundary-scan test products.

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## Executive Summary

It may not make sense, but it is possible – and quite cost-effective – to do at-speed functional verification testing of serial port interfaces long before a circuit board design can do anything. That is: before the board can boot and even before the design’s functional software has been completed by the development department. In other words, you can do functional tests without the design’s functional firmware. And, in addition, you won’t have to spend a lot of time and effort developing those traditional functional tests for the serial port interfaces because you won’t need them.

Instead, the boundary-scan-based (JTAG) methods described in this eBook give you several options for serial port testing, beginning with first-pass physical layer tests that detecting shorts and opens and then moving up to at-speed verification testing of the interface’s transmit and receive drivers as well as its communications engine. This at-speed testing takes advantage of embedded instrumentation intellectual property (IP) inserted into an on-board field programmable gate array (FPGA).

In the end, you’ll be able to benefit from concurrent engineering, a best practice in the industry today. You won’t have to wait to do functional serial port tests while the software development department is still programming the product’s functional firmware. Both can happen at the same time. Essentially, you’ll be able to de-couple functional test of the serial interfaces from any dependency on firmware development. Ultimately, you’re able to get your product to market faster so it can start generating revenues sooner. And you can cut your test costs too since you won’t have to develop new tests for each design because the test IP inserted into a board’s functional FPGA can be replicated and re-used on succeeding designs.

## Introduction

When first prototypes of a new printed circuit board (PCB) design are being brought up to verify the functionality of the design prior to the product moving into volume manufacturing, engineers must verify serial communications interfaces such as UART (Universal Asynchronous Receiver/Transmitter), SPI (Serial Peripheral Interface), I2C (Inter-Integrated Circuit) and others. Engineers are under constant pressure to verify the functionality of prototypes as soon as possible. Faults in the design must be identified and promptly corrected before it can move into

manufacturing. The sooner the design of a new product can be fully verified, the sooner it will be manufactured and delivered to the marketplace where it can start generating revenues.

Unfortunately, the functional firmware needed to boot prototype PCBs so that functional tests can be performed is often not complete when the first prototype hardware is available. In addition, functional test programs must also be developed, possibly lengthening the test phase even more. Ideally, the product's functional firmware and all test programs would be fully developed and available when first prototypes arrive. This is seldom, if ever, the case.

Now though, solutions are emerging which allow serial interfaces like UART to be functionally tested at their operational speeds without the need for any of the system's functional firmware or functional test programs. These interfaces can be tested with re-usable test embedded instruments inserted into an on-board FPGA. Not only would these methods allow prototypes to be verified sooner without firmware, but they could also reduce the amount of test-specific software test engineers have traditionally developed for each and every design. In general, the boundary-scan-based test methods are reproducible from one design to the next. Moreover, the embedded instrumentation IP, which is central to the at-speed functional test method, is portable and can be re-used in the same FPGA device on other designs, further shortening the time-to-market for multiple designs.

## **On-Board Structural Test**

Many, if not most, digital chips today are compatible with the boundary-scan/JTAG standard (IEEE 1149.1) and include a boundary-scan Test Access Port (TAP). Some devices with a UART interface, like processors, GPS (global positioning system) devices, application-specific integrated circuits (ASIC) and microcontrollers also include boundary-scan resources on-chip. As a result, boundary-scan interconnect tests can be employed as an initial first-pass test method on the UART interfaces that provide chip-to-chip interconnection for two devices on a PCB. These tests will take advantage of the boundary-scan resources on each chip to test and verify the structural connections between the two devices via their UART interfaces. (Figure 1) Structural tests typically identify shorts and opens, and verify fundamental electrical connectivity.

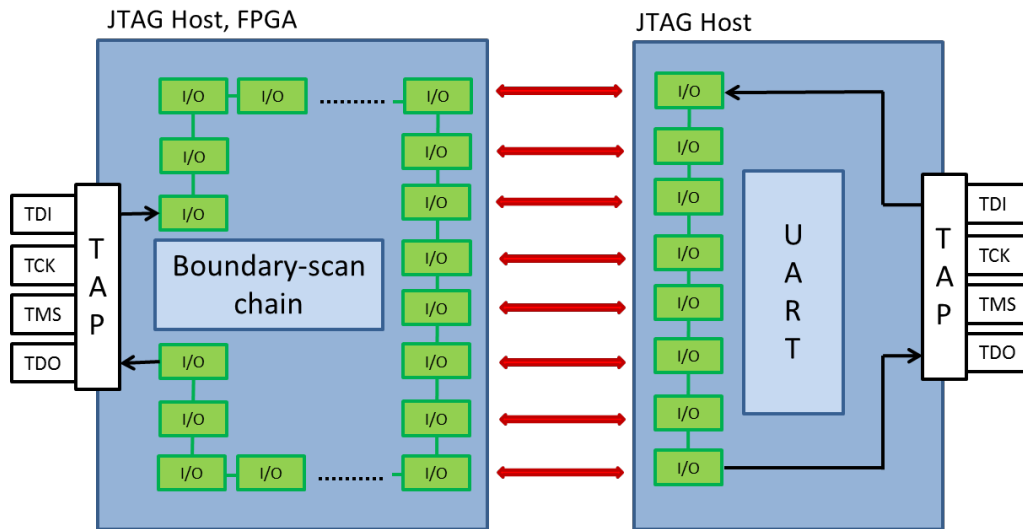


Figure 1: UART on-board interface testing with boundary-scan (JTAG)

## Off-Board Structural Test

Boundary-scan interconnect tests can also be employed via a PCB's edge connectors. This can be accomplished by either looping back the transmit signal (TX) to the receiver signal (RX) in the UART interface, or by testing the interface from external off-board boundary-scan resources located on an interface board. (Figure 2) In both cases, these tests will take advantage of a chip's boundary-scan resources to test and verify the structural connections. As with the previous method, the fault coverage will include shorts and opens and it will provide an excellent first-pass verification of the electrical physical communication layer of the UART interface. In addition, any other connections to boundary-scan-compatible devices on the PCB can also be tested during this process. These first two test methods will neither exercise nor test the UART interface's transmit and receive functional drivers or the receivers in the UART communication engine.

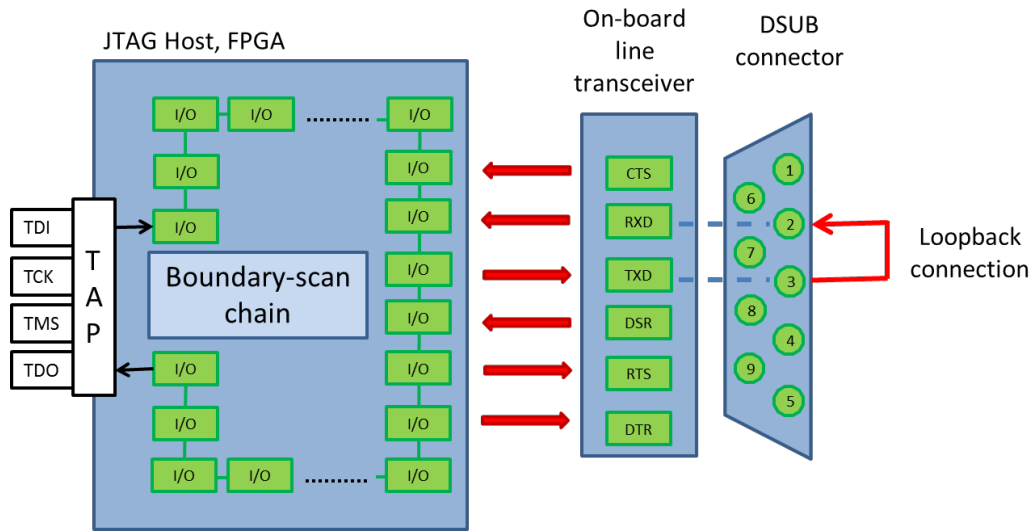


Figure 2: UART off-board interface testing with boundary-scan (JTAG)

### At-Speed Functional Test

Unlike the previous two methods that were based strictly on boundary scan/JTAG testing techniques, a UART interface can also be verified at-speed from an embedded instrument IP inserted into an on-board FPGA. (Figure 3) The embedded instrument is able to exercise the UART interface at the system's baud rate. In addition, the device's transmit and receive (TX/RX) drivers and the UART communication engine can also be tested with this FPGA-based IP.

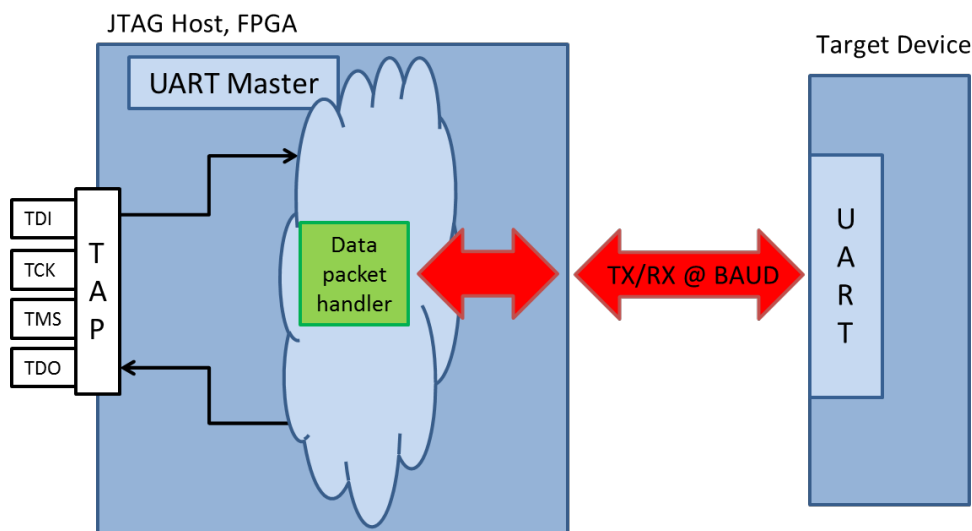


Figure 3: At-speed testing of a UART interface from an embedded instrument in an FPGA

Before testing can begin, the FPGA must be configured with a UART Master embedded instrument that can communicate through the boundary-scan/JTAG TAP interface on the FPGA. The UART Master is typically configured in an on-chip network of embedded instruments, which is made possible by the IEEE P1687 Internal JTAG (IJTAG) standard. This standard allows other types of embedded instruments in addition to the UART Master to be inserted into the same FPGA and operated by a test engineer. Examples of other types of test embedded instruments might be I2C Masters, SPI Masters, SPI flash programming IP, frequency measurement IP and others.

The UART verification test will consist of test data being communicated across the UART interface, but first the data must be placed into a buffer in the FPGA's UART Master IP. When the data has been loaded into the buffer, at-speed UART communications can be started by a command to the UART Master IP.

Similarly, the UART Master IP can be instructed to wait to receive data. Once the data has been received and stored in its buffer, the UART Master embedded instrument can then transmit the data across the JTAG scan chain on the PCB and deliver it to a boundary-scan test tool for analysis. (Figure 3) The data to be transmitted or received can be collected into batches of different sizes, such as bytes, words or pages. When the data is received by the boundary-scan tool, it can be manipulated, decoded and analyzed. The tool can then validate whether the communications through the UART interface was successful or not. Unsuccessful communications could indicate a faulty interface.

### **Application Example: Testing a GPS UART**

In this example, the entire test of a UART interface on a GPS module requires less than two seconds. The GPS module was tested so that a one pulse-per-second (PPS) clock on the board could be started. The following is a high-level description of the steps that were taken during the test sequence.

First, the baud rate of the UART interface on the GPS device being tested must be set to its default speed. This is accomplished by sending UART commands via the on-board FPGA's JTAG-to-IJTAG link to the UART Master embedded instrument in the FPGA. Once this connection is established, the UART Master can communicate commands to the GPS module.



Next, a receiver ID command is sent to the GPS device.

The UART Master embedded instrument should then be instructed to wait for data. In this case and with this particular GPS module, the data returned to the UART Master through the UART interface was a 2k-byte data packet. When the entire data packet had been received, it was transferred by the UART Master IP over the FPGA's JTAG-to-IJTAG interface to a boundary-scan test tool or other user-specific test executive application, which would typically be running on a connected personal computer. The boundary-scan test tool or test application could then examine and analyze the contents of the packet.

In this particular example, the data packet held the following information:

- Copyright message
- Software version
- Software date
- Manufacture date and serial number

This data was extracted by the boundary-scan test tool and verified for accuracy against known data on the GPS module.

The sequence described above validated that the UART serial link between the FPGA and the GPS device-under-test was functional and that the UART interface was operating at the speed expected by the test or design engineer. This test also verified some of the internal functionality of the GPS module.

## Conclusions

To keep up with the fast pace of the electronics industry – where the window of opportunity in the marketplace for new products continues to shrink – design and test engineers, as well as engineering managers, must constantly search for new methods which will shorten a product's overall time-to-market. In general, concurrent engineering, where multiple engineering tasks are performed in parallel rather than sequentially, is one such method. A particular example of an effective concurrent engineering method would be performing functional at-speed testing of serial communications interfaces on prototype PCBs while the design's functional firmware is being developed in parallel. Previously, functional tests could not be performed on prototype PCBs without functional firmware already running on the hardware. Now, several boundary-scan/JTAG-based methods can be deployed to test the structural integrity and at-speed functionality of selected UART interfaces without the benefit of functional firmware, greatly shortening the product's time-to-market.

Embedded instrumentation IP inserted into an on-board FPGA can perform a range of tasks during development and production. For example, an embedded instrument might perform high-speed programming of SPI flash or EEPROM memory connected to an FPGA.

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