Memory Fault Insertion and Detection on Intel® 4th Generation Core i3/i5/i7-4xxx Series

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Table of Contents

Introduction

This eBook provides insight into unique memory fault diagnostic capabilities that can be applied to the latest Intel platforms to help engineers with both board bring-up and production test. Feedback from the marketplace is that memory testing continues to be a big challenge for customers. Thus the purpose of this eBook is to describe a unique solution to that problem. The current Processor-Controlled Test (PCT) functional test tool within the ScanWorks® platform delivers the unique features needed to help solve the memory test challenge.

The PCT capabilities discussed in this paper can be applied to most Core™ and Xeon® designs. The paper is targeted at memory setup and testing on an Intel Customer Reference Board (CRB) using the Intel® 4th Generation Core Processors (Haswell desktop and mobile) to demonstrate the capabilities of PCT. Memory testing requires two distinct steps. The first is the memory controller setup and the second is the actual testing of the memory devices. The memory setup will be discussed at a high level to establish a foundation for the paper.To illustrate the abilitiesies of PCT, the DIMMs were modified to simulate hardware faults. Both shorts and opens were inserted on data pins, data mask pins, and data strobes pins of several DIMMs.

The Platform Memory Setup

Intel provides for almost all platforms the Memory Reference Code (MRC), which is required to make the memories work. The MRC executes from the BIOS, to provide the initialization of memory devices and the training of the memory devices to operate at the most efficient performance level. However, using this methodology for production test has some significant inherent problems. These problems, consisting of boot-costs, memory controller obfuscation, and others are discussed in the eBook "*Testing Memories without BIOS on the Latest Intel Platforms*." Suffice it to say, we need to simulate the execution of the MRC as part of the test but eliminate the inherent problems mentioned to have a viable, deterministic solution. PCT overcomes these problems by combining a model-based test profile, with a run-control engine, and a special proprietary MRC. The profile is a sequence of register writes to the memory controller to accomplish the task of lane training. Should the lane training fail, PCT provides a detailed diagnostic error message. Once the memory setup is successful, the memory testing can begin. Note that for the purposes of this study, from a functional test perspective, the memory

controller does not see a difference between SO-DIMMs and soldered memory. In fact, an SO-DIMM has just soldered memory on a separate PCB that is inserted into the SO-DIMM socket.

The Platform Background

The memory tests were conducted on an Intel Shark Bay platform, specifically the Grays Reef Customer Reference Board (CRB). The Grays Reef CRB has the facility for a 2 SO-DIMM population, to place the memory controller (CPU) into dual-channel or single-channel operation.

This study was targeted at diagnosing a faulty SO-DIMM, memory device or failing bit for manufacturing test. Each fault injected consisted of modifying an SO-DIMM to allow fault detection with PCT. For soldered-down memory, the diagnosis will be identical to the method for SO-DIMMs. The PCT test profile uses a variety of built-in memory test routines. The profile starts at the highest level of test abstraction to isolate the grossest memory errors, and successive testing narrows the scope until at the lowest level the resolution is at the bit level. The reason for this approach is to minimize the test time for the quickest error detection with the focus being on production test. These profiles can be manipulated by the test developer to allow for a shift in focus as dictated by any particular situation.

Fault Insertion 1: SODIMM with DQS7# and DQS7 Short Circuit

A fault was added by shorting pins 186 and 188 on an SODIMM (DQS7# and DQS7). The physical fault is shown in Figure 1:

Figure 1: DQS7#/DQS7 Short

After inserting the faulty DIMM, the PCT test profile was executed. The memory setup completed indicating no memory controller issues but failed the memory tests. The PCT error information is shown in Figure 2:

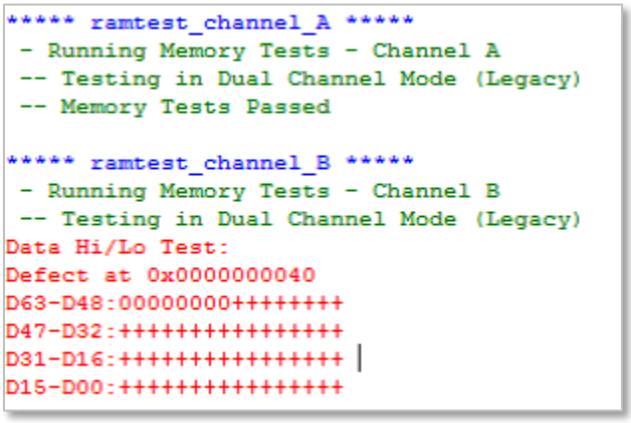

Figure 2: DQS7#/DQS7 Failure Detail

This diagnostic information points to the failing Channel (B), and that the data bus test has failed while running the Data Hi/Lo Test and highlighted the failing data bits DQ63-DQ56 (0 indicating stuck low). This error is pointing to either a Data Mask Fault with DM7 or a Data Strobe fault with DQS7 as these are the only two possible pins that exercise control over this portion of the data bus. Functionally, a fault with DM or DQS will have the same failure signature, so PCT cannot distinguish between these two failures. However, the operator should now know the fault is either DM7 or DQS7#, and if soldered memory is being used, the relevant device can be isolated. If the operator is not familiar with DIMM memory designs to failure types, additional informational hints may be added to the diagnostic message by the test developer to assist the operator as necessary.

Fault Insertion 2: SODIMM with DQ18, DQ19, and DQ24 Short Circuit

A fault was added by shorting pins 51, 53 and 57 on an SODIMM (DQ18, DQ19, and DQ24).

The physical fault is shown in Figure 3:

Figure 3: DQ18/DQ19/DQ24 Short

Again the PCT test profile was executed on the target. The memory setup completed but failed the memory tests. The PCT error information is shown in Figure 4:

```
***** ramtest_channel_A *****
 - Running Memory Tests - Channel A
 -- Testing in Dual Channel Mode (Legacy)
Data Bus Shorts Test:
Defect at 0x0000000000
D63-D48:++++++++++++++++
D47-D32:++++++++++++++++
D31-D16:+++++++++S++++++
D15-D00:++++++++++++++++

***** ramtest_channel_B *****
 - Running Memory Tests - Channel B
 -- Testing in Dual Channel Mode (Legacy)
 -- Memory Tests Passed
```

Figure 4: DQ18/DQ19/DQ24 Failure Detail

This information points to the failing CHANNEL (A), and Data Bus Shorts Test failed. The failure signature is highlighting data bit DQ22 (shorted) as failed. Once the "swizzling" decode (see Figure 5) has been performed on the failure, the correct bit (DQ18) is the first failing bit on the bus.

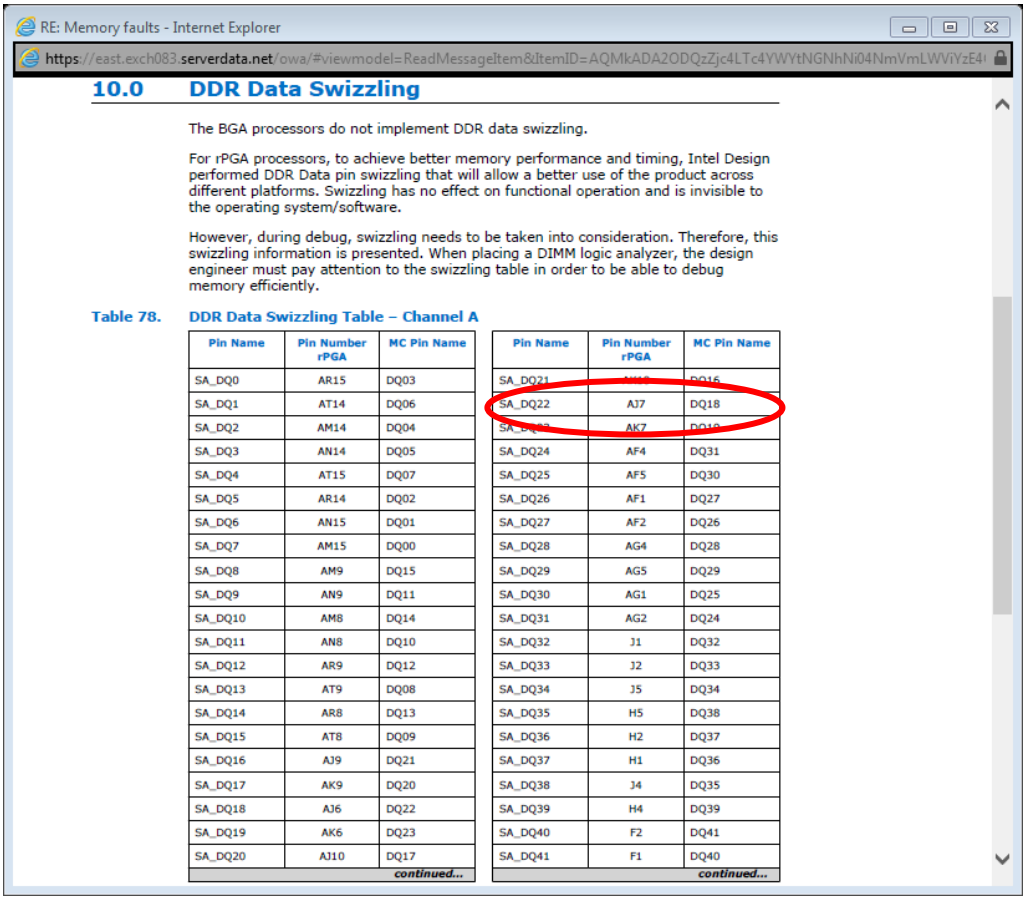

Figure 5: Swizzling Data

It should be noted that it appears PCT has missed the other failing bits (DQ19 and DQ24), as they had not been reported. This is due to the PCT memory Data Bus Shorts test reads the state of the bus with the expected data value. In this example, the first data pattern read from the bus found the fault on data bit DQ22; that specific pattern on DQ19 and DQ24 read correctly, and no failure would have been detected. However, subsequent patterns on the data bus would detect and report the additional failing bits. This implementation is by design. PCT starts with the highest level of test abstraction to isolate the grossest memory errors, and successive testing narrows the scope. The operator is expected to cure the initial fault before moving on to the next. In this case, removing the short will effectively fix the other fault.

Fault Insertion 3: SODIMM with DQ38, DQ39, DQ44 and DQ45 Open Circuit

A fault was added, by removing a resistor pack, to create an open circuit on pins 140, 142, 146 and 148 on an SODIMM (DQ38, DQ39, DQ44, and DQ45). The physical fault is shown in Figure 6:

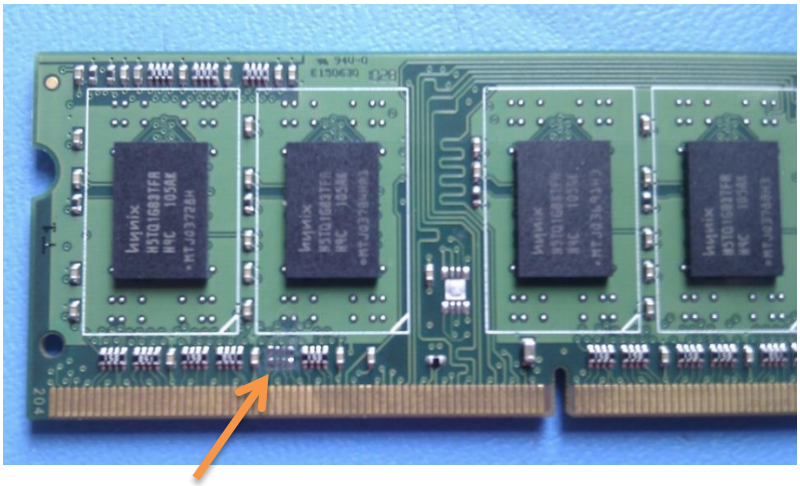

Figure 6: DQ38/DQ39/DQ44/DQ45 Open Failure Detail

After the PCT script was executed on the target, the memory setup completed but failed the memory tests. The PCT error information is shown in Figure 7:

```
***** ramtest_channel_A *****
 - Running Memory Tests - Channel A
 -- Testing in Dual Channel Mode (Legacy)
Data Hi/Lo Test:
Defect at 0x0000000000
D63-D48:++++++++++++++++
D47-D32:++11++++1+++1+++
D31-D16:++++++++++++++++
D15-D00:++++++++++++++++

***** ramtest_channel_B *****
 - Running Memory Tests - Channel B
 -- Testing in Dual Channel Mode (Legacy)
 -- Memory Tests Passed
```

Figure 7: DQ38/DQ39/DQ44/DQ45 Open Failure Detail

This diagnostic information points to the failing Channel (A), and that the databus test has failed by highlighting the failing signature of data bits DQ45, DQ44, DQ39 and DQ35 stuck high. Once the "swizzling" decode (see Figure 8) has been performed on the failure, the correct bits

(DQ45, DQ44, DQ39, and DQ38) are identified as failing on the bus. The stuck high, in functional terms, depicts an open circuit.

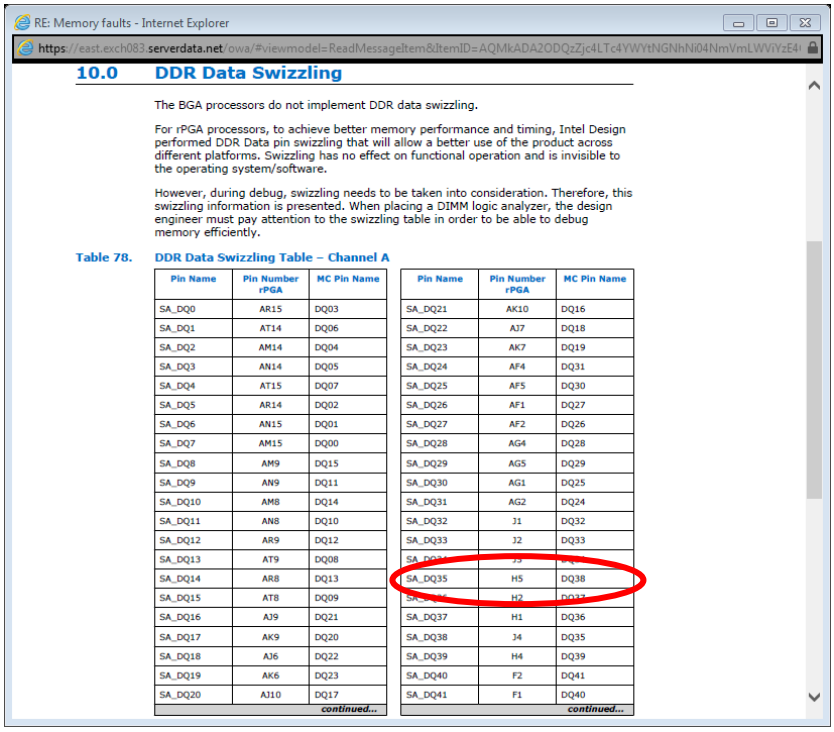

Figure 8: Swizzling Data

Fault Insertion 4: SODIMM with DM3, DQ26 and DQ27 Open Circuit

A fault was added, by removing a resistor pack, to create an open circuit on pins 63, 67 and 69 on an SODIMM (DM3, DQ26, and DQ27). The physical fault is shown in Figure 9:

Figure 9: DM3, DQ26 and DQ27 Open

The PCT profile was executed on the target. The memory setup completed but failed the memory tests. The PCT error information is shown in Figure 10:

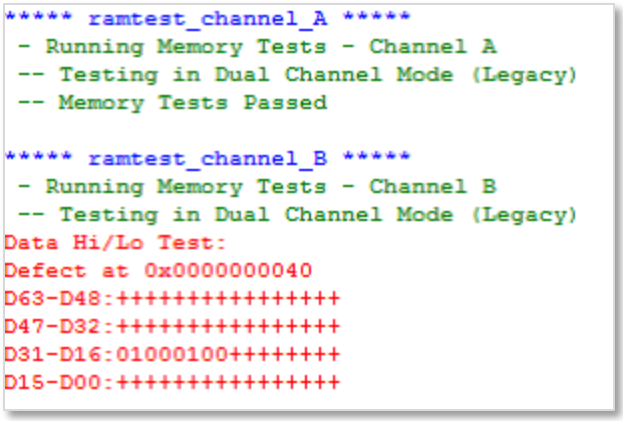

Figure 10: DM3, DQ27, and DQ27 Open Fault Detail

This error information points to the failing Channel (B), and that the data bus test has failed. The fault signature is highlighting failing data bits in the 8-bit block of DQ31-DQ24 are stuck low and high. The error is pointing to either a Data Mask Fault with DM3 or a Data Strobe fault with DQS3. Functionally a fault with DM or DQS will give the same failure signature, so PCT cannot distinguish between these two failures. However, the operator now knows the fault is DM3 or DQS3 (#), and if soldered memory is being used, this can isolate to the relevant device.

It should be noted that it appears PCT has missed diagnosing the data bits DQ26 and DQ27. However, if the bit failure pattern is examined, it can be seen (with the "swizzle" decode in place for the failing bits DQ26 and DQ30), that the other failing bits (DQ25 and DQ27) are stuck high. In functional terms, this depicts an open circuit.

Summary

This document covered short and opens on memory DIMMs and in each case the tool identified the rank, device and bit level where the failure occurred. The memory test development is automated based upon the Intel CRB models provided with the tool. PCT can also test buses and I/O devices for shorts and opens. All these functional tests are created using TCL as the scripting language and can be modified by the developer as necessary.

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