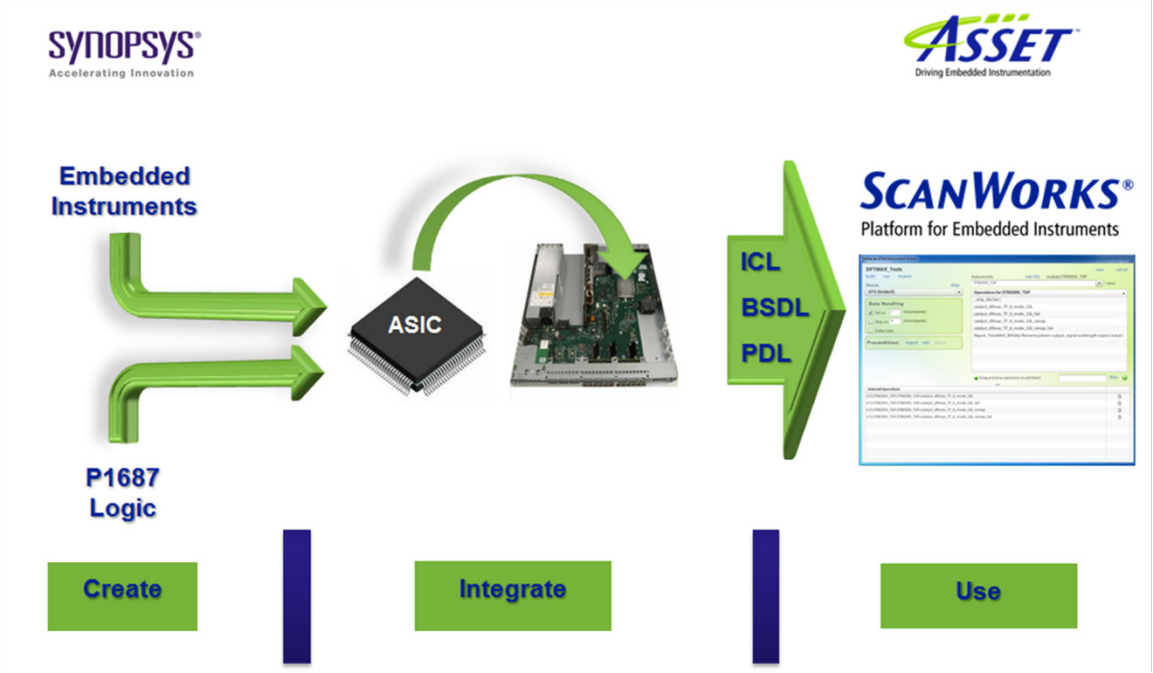
IEEE P1687 IJTAG Tools Ecosystem – A Case Study



BY ADAM CRON, AL CROUCH, JOHN POTTER

SCANWORKS®
Platform for Embedded Instruments

Adam Cron – Synopsys Principal Engineer

Adam Cron, Principal Engineer at Synopsys, is part of the Test Automation Implementation R&D Group and has been with the company for over 16 years. A Syracuse University graduate, Adam has also worked in test-related fields at Motorola and Texas Instruments for 30 years in the industry. Adam is vice-chair of IEEE Std P1838, chaired the IEEE 1149.4 Working Group, and has worked on IEEE-1149.1, 1149.7, 1532, 1450, 1500, 1149.8.1, P1687, etc. Adam is also chair emeritus of the Test Technology Technical Council's Test Technology Standards Group which oversees the development of test standards, and is an IEEE Golden Core recipient.

Al Crouch – Chief Technologist, Embedded Instrumentation Methodologies and IJTAG

Al investigates the use of embedded instruments for IC test and debug, board test and debug, and software debug. He is a Senior Member of the IEEE and serves as the vice chairman of the IEEE P1687 IJTAG working group that is developing this standard for embedded instruments. He has contributed significantly to its hardware architecture definition. Al is also a member of the P1838 Working Group on 3D test and debug, and co-chair of the iNEMI BIST group, which is defining the use of embedded instruments for board test. Al's previous experience includes design-for-test and debug at various semiconductor companies, including TI, DEC and Motorola, as well as chief scientist at startup companies DAFCA and INOVYS.

John Potter – Senior Principal Technologist and IJTAG Development Manager

John has 23 years of industry experience in semiconductor test development including ASIC DFT, methodology automation, FPGA firmware, embedded instruments, software and new product development. He is a member of the IEEE and is involved with IEEE P1687 and IEEE P1838 working groups as well as a member of the IEEE Standards Association. He received both a BSEE and MSEE from West Virginia University.

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Executive Summary

The objective of this proof-of-concept case study was to demonstrate the ecosystem supporting the IEEE P1687 IJTAG standard for embedded instrumentation. Specifically, this case study highlights the interoperability of currently available IJTAG tools and how these tools enhance the efficiency and re-use of IJTAG-compatible embedded instruments. Other benefits of IEEE P1687 IJTAG include the portability from one design to the next of the debug, validation and test vectors or patterns associated with any IJTAG embedded instrument. Ultimately, these factors and others, significantly reduce design and manufacturing costs, shorten design cycles and deliver more robust, high quality systems to the marketplace.

The IEEE P1687 Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device (commonly referred to as Internal JTAG or simply IJTAG) is a standard for managing, accessing and operating instruments that are embedded in semiconductor chips (embedded instruments) to serve purposes such as design validation, design debug and manufacturing test of chips, circuit boards and systems. The standard's website is http://grouper.ieee.org/groups/P1687/.

The IJTAG standard was developed to facilitate, simplify and increase the efficiency of tasks associated with embedded instruments, including the access, management and operation of these instruments. Embedded instruments can be deployed during several phases of the life cycle of an electronic system, such as:

- Chip, board and system development
- Wafer probe during the fabrication of integrated circuits (IC)
- Circuit board test
- Field support and service

Most of the instruments that are being embedded into chips today do not share a common access technology or any operating processes or procedures for managing and scheduling their operations.

To demonstrate the interoperability of the tools in the IJTAG ecosystem, a complex embedded instrument was developed, implemented and operated by tools from several of the companies

that currently participate in the ecosystem. Specifically, the companies that collaborated on this project were a chip vendor who architected and implemented the chip, Synopsys who developed and supplied the EDA tools (DFTMAX™ product and TetraMAX® ATPG) to the chip vendor for synthesizing the embedded instrument and its access infrastructure, a system manufacturer who made use of the chip with the embedded instrument in a JTAG (IEEE 1149.1 boundary scan) chain, and ASSET® InterTech who supplied the ScanWorks® platform to access and operate the embedded instrument. (Figure 1).

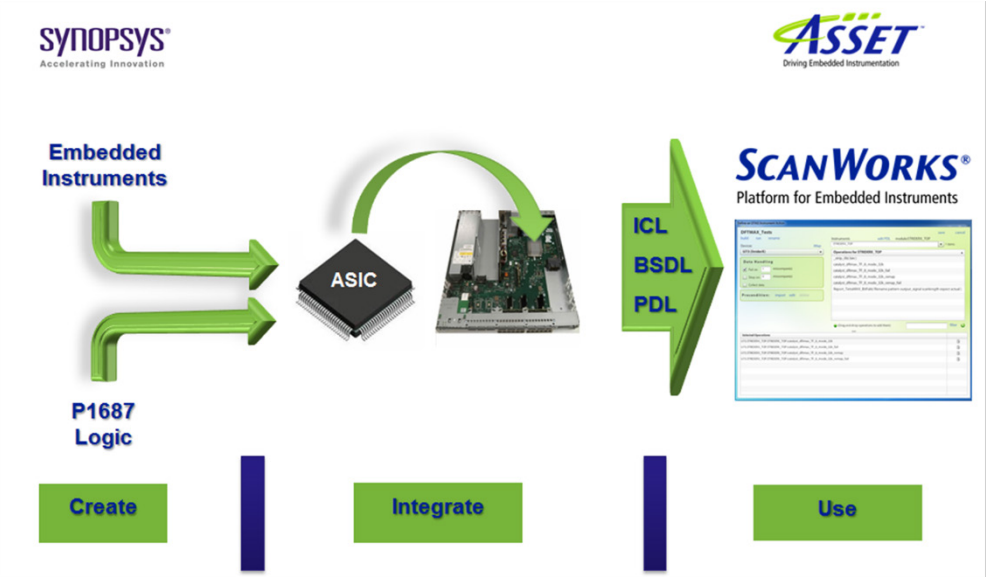


Figure 1: Example portions of the IJTAG Ecosystem

Overview of Proof-of-Concept

This case study showed the importance of re-use of embedded instruments and how this re-use spans every phase of an electronic system's life cycle from chip creation, through circuit board development and manufacturing, onward to system manufacturing, and eventually into operational systems in field service applications. Embedded instruments and their tests can be employed in several areas in the life cycle, such as:

- Chip test and verification
- Circuit board design validation
- Board-level manufacturing test
- System test and diagnostics

- Troubleshooting in the field

ASSET and Synopsys collaborated on this case study to demonstrate that IJTAG achieves these objectives and to show the interoperability of the respective tools that make up an IJTAG ecosystem. (NOTE: Other IJTAG tools in addition to those included in this proof-of-concept are also currently available.)

The collaboration between ASSET and Synopsys was initiated by a request from engineering management at a major system-manufacturing firm. Some of the goals of the system supplier were to determine how well IJTAG-based strategies would meet certain validation, test and debug challenges. Specifically, the system supplier wanted to reduce development cycle times and deliver new products to market faster. In addition, cost reductions through re-use of embedded instrument intellectual property (IP) across chips, circuit boards and systems was also of interest. Although this case study involved an FPGA, the system developer was interested in eventually deploying IJTAG-compatible embedded instruments and processes in application-specific integrated circuits (ASICs). The debug, validation and test challenges the system manufacturer faced were driven by the increasing complexity of its ASICs and the consequent effects this was having on system-level complexities and manufacturing costs. Engineers at the system manufacturer believed that a standard method for managing and coordinating the test operations of the exploding number of embedded instruments could result in greater efficiencies and cost savings over the life cycle of new products.

Subsequent to the success of this proof-of-concept project, the case study was extended to operating the same embedded instrument type in a real-world ASIC that was used in a productized system board.

A Short Introduction to IJTAG (IEEE P1687 Internal JTAG)

Why IJTAG is needed

The major objectives that prompted the development of IEEE P1687 IJTAG were:

- Standardize how embedded instruments are managed, organized, accessed and operated.

- Decouple the operation of embedded instruments from any one physical access method. To date, most embedded instruments have been accessed via the IEEE 1149.1 Boundary-Scan Standard. The new IJTAG standard would allow embedded instruments to be accessed by any physical method as long as it conformed to the requirements of the IJTAG standard. As a result, the capabilities of the IEEE 1149.1 Boundary-Scan Standard would be retained for board test, the original intent of the standard, while still providing access to embedded instruments via the IJTAG standard.
- Enable the re-use and portability of instruments embedded in semiconductors.
- Enable the re-use and portability of test vectors or patterns developed for these instruments.
- Create a technology that would allow embedded instruments to be designed and integrated into chips based on engineering tradeoffs and operational budgets.
- Provide a more efficient method for documenting the needs and operations of embedded instruments.

Examples of Embedded Instruments:

- Memory BIST (MBIST)
- Logic BIST (LBIST)
- Temperature Monitor
- Voltage Monitor
- Power Control
- Clock Control
- Serdes Validation
- Interconnect Testing

The IJTAG standard was developed because engineers were struggling with methods for managing, scheduling and automating the operations of the many different types of instruments that are being integrated into chips. Chip design engineers had discovered that embedded instruments were, in most cases, a more effective and cost-efficient means of verifying and characterizing their designs as opposed to strict reliance on external automatic test equipment (ATE). Several methods have been employed to access these embedded instruments, but eventually the IEEE 1149.1 JTAG boundary-scan standard emerged as the *de facto* access method because most chips include the JTAG Test Access Port (TAP) and its corresponding finite state machine (FSM).

Because the number of instruments embedded in chips can range into the tens, hundreds, and even thousands, it has become apparent that the JTAG standard, which had been developed for board test, was too limited to efficiently manage these instruments. Since the IEEE 1149.1 JTAG standard relies on centralized instructions, its scalability and test scheduling flexibility is insufficient to accommodate the rapidly proliferating number of embedded instruments.

In essence, the movement toward embedded instruments has driven the functionality of expensive ATE testers into the chips themselves, and this was never the intended use space for

JTAG/boundary-scan board testers. JTAG testers were never meant to rival the large-scale ATE testers. Instead, the development of the JTAG/boundary scan standard was originally driven by the need for more cost-effective non-intrusive testers that could be deployed in board and system test applications.

IEEE P1687 IJTAG was developed to meld a chip-level hardware access method like JTAG with a software- and data-driven configurable network of embedded on-chip instruments. What this means is that data flowing through the network would configure the network. By decoupling the hardware access method from the embedded instrumentation access and control network, neither one would limit or unduly restrict the other. Chip designers would then be liberated to design their on-chip access architectures in response to their engineering tradeoffs and operational budgets. Other aspects of IJTAG also help engineers upstream from chip design. IJTAG ensures that the embedded instruments and their operational procedures (i.e. test vectors) can be re-used by circuit board designers and board-level engineers in validation, test and debug applications. Some JTAG/boundary-scan board test tools have integrated IJTAG capabilities. As a result, they are able to manage, schedule and automate IJTAG embedded instrument functionality in chip-level, board-level and system-level applications.

What the IJTAG standard creates, and which this proof-of-concept is intended to demonstrate, is an ecosystem for the efficient re-use of embedded instrumentation throughout the entire life cycle of an electronic system, beginning with discrete chips, moving to prototype and assembled circuit boards, and culminating in operational systems in the field.

Basic IJTAG Architecture

The figure below (Figure 2) illustrates four concepts: [1] a hardware access method for embedded instruments, [2] the software-driven IJTAG network connecting the embedded instruments, [3] the embedded instrument IP on a chip, and [4] the instrument's test targets. In this case, the chip's hardware port and controller that provide access to the IJTAG network is the JTAG TAP and TAP Controller, as defined in the IEEE 1149.1 Boundary-Scan Standard. However, once the IJTAG AccessLink instruction is installed (in this case, a JTAG-IR Opcode), all accesses, configurations, operations and applications of embedded instrumentation procedures

(vectors) are simply JTAG data register scans (DR-Scans) using the data side of the JTAG finite state machine (FSM).

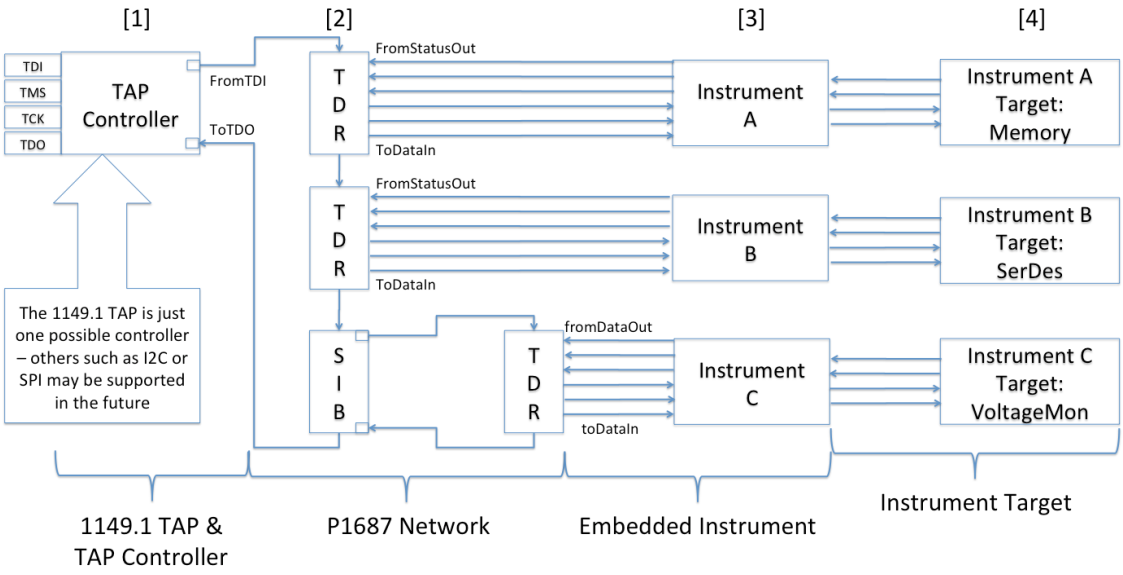


Figure 2: An example of a basic IJTAG architecture

IEEE P1687 IJTAG allows the JTAG/boundary-scan TAP and its TAP Controller to efficiently and effectively access instruments that are embedded on-chip. The IJTAG network of instruments is described by IEEE P1687's Instrument Connectivity Language (ICL) syntax and the operational procedures for the embedded instruments are described by IEEE P1687's Procedure Description Language (PDL) syntax. The software-driven IJTAG Segment Insertion Bit (SIB) is a control mechanism to dynamically configure access to the on-chip instrumentation network based on data passing through this network. SIBs can bypass or concatenate segments of the network in response to the requirements of the application. Instruments located on a bypassed segment of the network can continue operating independently of other ongoing processes.

The Proof-of-Concept

Conceptually, the IJTAG ecosystem is made up of three main parts: creation, integration and operation. This case study demonstrated that an embedded instrument and its access network could be created during the chip design phase with the help of Synopsys' DFTMAX tool. Next, test patterns could be generated by the Synopsys TetraMAX ATPG, and described in IEEE P1687 IJTAG's ICL and PDL syntax so that they could be re-used and operated in a validation,

test or debug environment by ASSET's ScanWorks platform for embedded instruments. In addition, using these tools for diagnostics or troubleshooting in the field was also demonstrated. Within the context of this proof-of-concept, the functional purpose of the embedded instrument was practically irrelevant. Of course, in a real world development setting, the functionality of every embedded instrument would be critical. The point of the case study was merely to illustrate the portability and re-use of embedded instruments and their operational test vectors within an IJTAG environment.

The figure below (Figure 3) outlines the flow between Synopsys tools and ASSET's ScanWorks platform. The target device, an Altera Cyclone III FPGA, is shown as the endpoint in the flow.

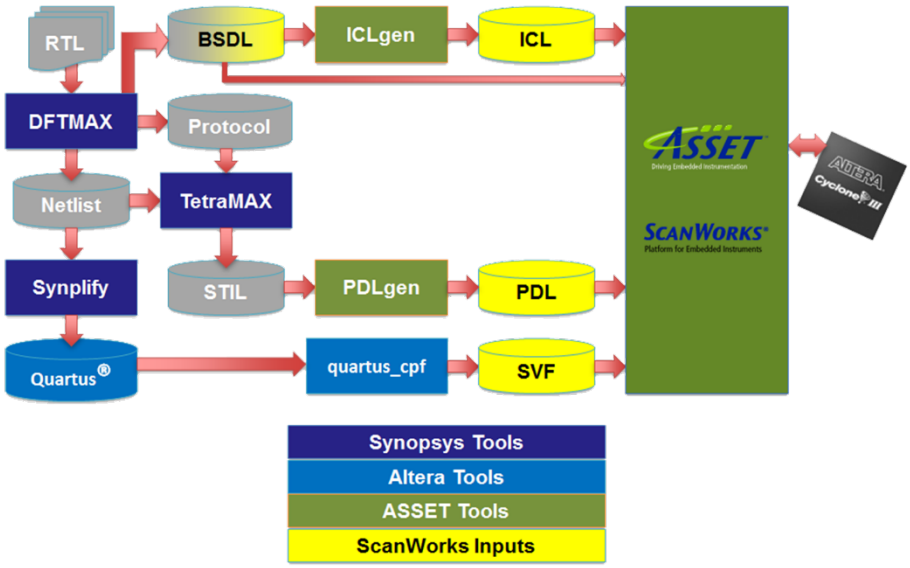


Figure 3: DFTMAX to ScanWorks Tool Flow

This tools flow had two distinct goals:

- To produce files that would configure an FPGA with certain circuitry.
- To generate test vectors represented in an IJTAG format so they could be re-used by a validation, test or debug tool. Typically, this would be an engineer validating a chip design or a test engineer testing a circuit board.

In this case study, ASSET's ScanWorks performed two different roles: [1] it processed a design bit-file to configure the FPGA, and [2] it processed the IJTAG files to operate the embedded

instruments within the FPGA. If the target chip had been an ASIC or system-on-a-chip (SoC) and not an FPGA, the overall tool flow would have remained largely the same.

The tool flow shown in Figure 3 began when a target circuit's Register-Transfer Level (RTL) files in Verilog were provided to the DFTMAX tool. DFTMAX, which represents the 'create/integrate' portion of the IJTAG ecosystem, inserted the instrument, the instrument's IJTAG access network and other required circuitry such as the JTAG TAP. These facilities would allow the instrument to be operated by ASSET's ScanWorks in various applications such as board- and system-level validation, test and debug. Next, DFTMAX generated several items, including a netlist of the device in Verilog, a protocol file for the TetraMAX ATPG tool and a Boundary-Scan Description Language (BSDL) file that described the circuitry's JTAG/boundary-scan data registers in the device's JTAG TAP.

The project team needed a Serial Vector Format (SVF) file so that ScanWorks could configure the FPGA. Synopsys' Synplify tool generated a Quartus project that was then executed to synthesize and implement the Verilog netlist into a configuration bitstream that was ultimately converted into an SVF file. Alternatively, a Standard Test and Programming Language (STAPL) file may be used by ScanWorks to configure the FPGA. TetraMAX generated the operational test patterns in the Standard Test Interface Language (STIL) format as defined by the IEEE 1450 standard. These STIL patterns were subsequently converted into a file containing IJTAG PDL syntax. The patterns described as procedure definitions in the PDL file operated the embedded instrument. ScanWorks configured the FPGA through the FPGA's integrated IEEE 1149.1 JTAG/boundary scan TAP.

As noted previously, the intent of this project was to demonstrate how the various IJTAG tools would interoperate to integrate embedded instruments into ASICs for system manufacturers. Following the case described here, an embedded instrument of the same type was inserted into an ASIC and operated. Figure 4 below illustrates this process.

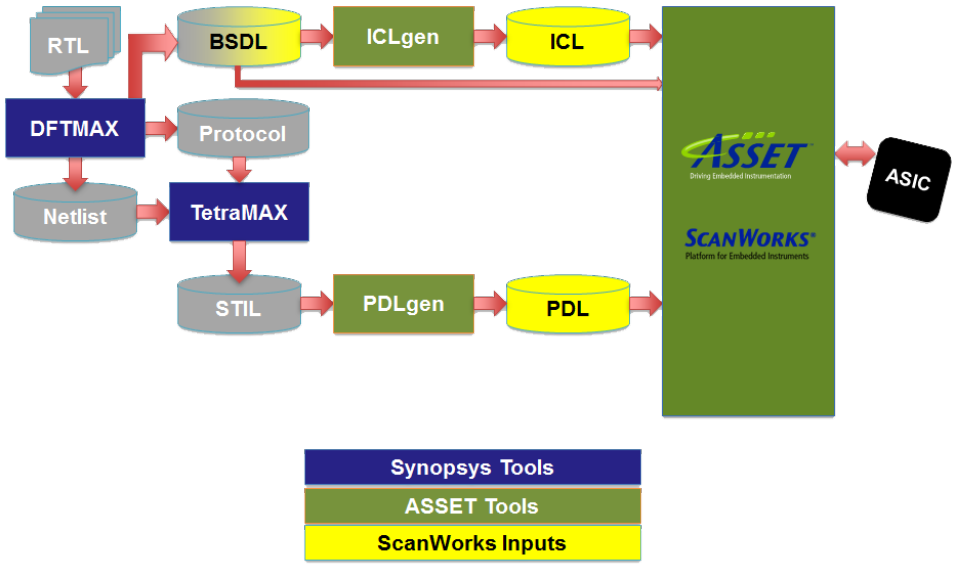


Figure 4: Inserting and operating an embedded instrument in an ASIC.

The Test Setup

The photograph below (Figure 5) shows the test setup for this proof-of-concept. An Altera Cyclone III FPGA Development Board with the target FPGA device is on the right. To emulate an ASIC environment, a secondary IEEE 1149.1 JTAG TAP to access the embedded instrument was created and inserted by DFTMAX and assigned certain pins on the device. This secondary TAP was accessed via one of the High Speed Mezzanine (HSM) headers on the development board. ASSET's ScanWorks could have connected directly to either the board's TAP or the FPGA's TAP to manage the embedded instrument. For convenience sake, ScanWorks was connected to the board's TAP via a USB JTAG hardware controller (lower right in the photo). ScanWorks is running on the laptop on the left in the photo. From the laptop, the ScanWorks platform could process IEEE P1687 IJTAG's ICL and PDL, as well as any IEEE 1149.1 JTAG processing that might be applied to test the target circuit board.

Figure 5: Hardware Setup for the FPGA portion of the case study

Validating Tool Effectiveness

An objective of this proof-of-concept experiment was to demonstrate that this tool flow could implement chip-level diagnostics in the field, such as troubleshooting a poorly performing SoC. Once the IJTAG flow was completed and demonstrated, a chip-level fault was inserted and activated, pattern response data was collected from test operations and this data was passed to the Synopsys TetraMAX tool for fault diagnosis.

ScanWorks was purposefully programmed using a mix of PDL and Tcl statements to indicate the embedded instrument had encountered a failure. Additionally, ScanWorks executed PDL and Tcl statements to create a TetraMAX-compatible failure file. The failure file was provided to TetraMAX to demonstrate its ability to locate and diagnose the embedded failure. (Figure 6)

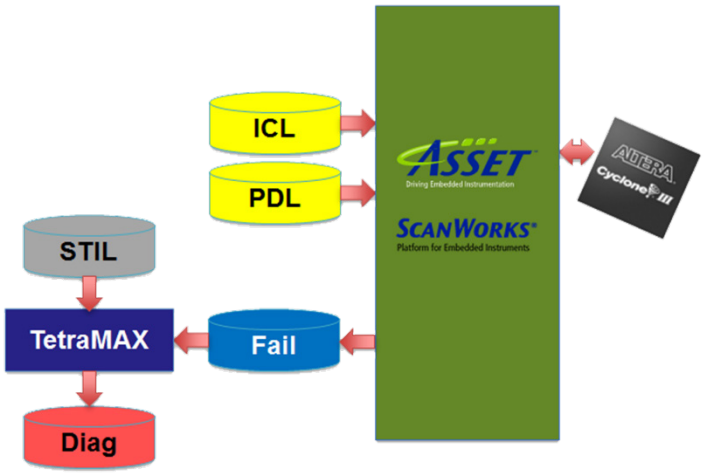


Figure 6: Diagnosing an embedded instrument failure

The simplest way to induce a failure signal to ScanWorks from the FPGA was to edit the data content that is loaded into the Boundary-Scan Register (BSR). The input and output contents of the BSR are typically held static. By editing the BSR contents, which had been initialized by the input pattern, an apparent stuck-at fault was introduced into the test circuit.

When TetraMAX analyzed the failure response, it was able to generate the likely candidates for the cause of the failure in the tool's diagnostic transcript. Subsequently, the location of the failure diagnosis was displayed in the tool's Graphical Schematic Viewer (Figure 7).

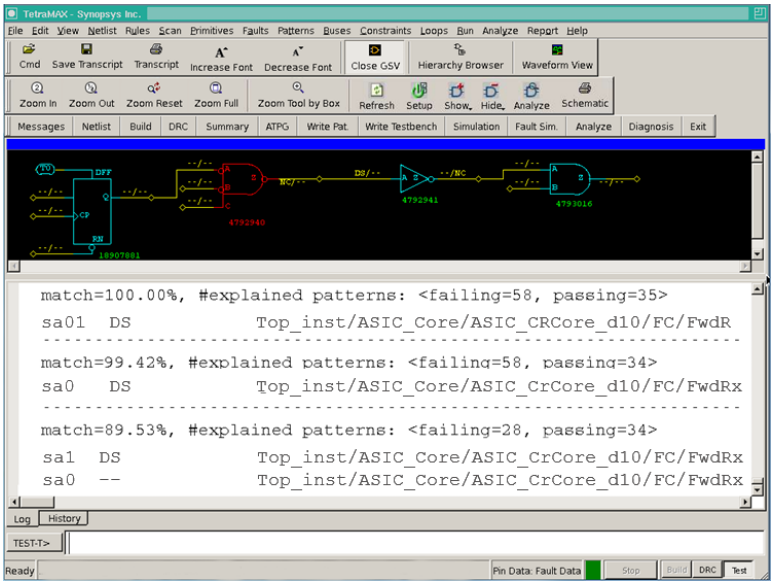


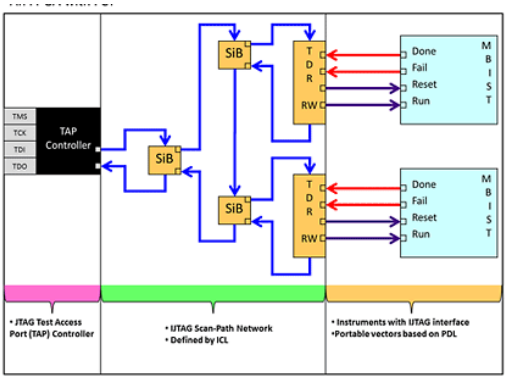
Figure 7: TetraMAX Graphical Schematic View

Conclusions

Interoperability among the tools that make up the IJTAG ecosystem and which are enabled by the new IEEE P1687 standard for embedded instrumentation (IJTAG) was demonstrated in this proof-of-concept case study involving chip-level design and test tools from Synopsys (DFTMAX and TetraMAX), and circuit board- and system-level validation, test and debug tools from ASSET InterTech (ScanWorks). This proof-of-concept was driven by certain engineering and test challenges faced by a system manufacturer, who worked with its ASIC provider as well as the tools suppliers to demonstrate the viability of the IJTAG ecosystem. Engineers at the system manufacturer were interested in determining how the IEEE P1687 IJTAG standard for embedded instruments could be deployed and scaled to meet the challenges of increasing ASIC complexities, lengthening test development cycles and escalating test costs. The results of this case study showed that embedded instruments and their operational test vectors could be re-used over and over again during each phase in a system's life cycle (chips, circuit boards and systems). Huge cost savings can be achieved because the cost of developing or modifying instruments and vectors for each phase in the life cycle can be avoided following the deployment of the IJTAG standard and its tool ecosystem.

Learn More

Learn more IJTAG. Register for our tutorial and lean how to use a standard protocol to access dissimilar instruments, shorten the design schedule, enable concurrent instruments and reduce effort and mistakes through automation.



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