# Doing More with Less – An IEEE 1149.7 Embedded Tutorial :
## *Standard for Reduced-pin and Enhanced-functionality Test Access Port and Boundary-Scan Architecture*

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**Abstract**

*IEEE Std 1149.7 offers a means to reduce chip pins dedicated to test (and debug) access while enhancing the functionality of the Test Access Port (TAP) as a complementary superset of the original IEEE Std 1149.1 (JTAG). Extended features such as hot-plug immunity, power management, optimization of scan throughput, access to instrumentation, and access to custom technologies provide welcome improvements for debug. Further, the boundary-scan architecture is bolstered to ensure full support for test. This important advancement in test and debug interfaces is well suited for access to multiple cores on SOC or multiple die in SIP or POP.*

## 1. Introduction

In the 1980s, the Joint Test Action Group (JTAG) was formed to address a growing concern about diminishing test access to chips on boards due to the adoption of surface-mount assembly methods and ongoing miniaturization of chip packages. In 1990, their efforts culminated in the ratification of IEEE Std 1149.1 – Standard Test Access Port and Boundary-Scan Architecture. While 1149.1 was firmly rooted in the need to solve the problems of board test, as exemplified by the provision for boundary scan, the proponents of the standard realized the need for a generalized means of low-level access to components on boards and in systems that would suit a wide range of uses. As a result, the 1149.1 test access port (TAP), as specified, has met this need.

In fact, even before the ink was dry, the 1149.1 TAP was being exploited for purposes beyond board test. In these early days, its utility was deployed to support access to chips for in-circuit emulation (debug), albeit often with additional pins for proprietary signals. Somewhat later, the ubiquity of the 1149.1 TAP was exploited in a normative sense for in-system configuration of programmable devices by way of IEEE Std 1532. Later still, use of the 1149.1 TAP as a debug interface was standardized by NEXUS 5001 (although still requiring additional signaling for many cases). Today, for the same reasons of utility and ubiquity, the 1149.1 TAP is considered the most likely means of access to chips that support embedded instruments per P1687 (informally known as Internal JTAG or IJTAG).

Notwithstanding the exceptional merits of the 1149.1 TAP, ongoing industry momentum toward greater miniaturization and still more integration led some to the conclusion that a makeover was needed [1]. In particular, they proposed to enhance its functionality and utility in applications debug, but also to reduce pins to be better suited to multi-core/ multi-die architectures. IEEE Std 1149.7 [2, 3, 4, 5] has been developed to meet these needs [6, 7, 8, 9, 10, 11, 12].

### 1.1 What is IEEE 1149.7

IEEE 1149.7 is a standard for a test access port and associated architecture that offers reduced pins and enhanced functionality. With regard to pin reduction, whereas the conventional 1149.1 TAP (TAP.1) requires at least four signals (with a fifth, for test reset, being optional), the reduced-pin 1149.7 TAP (TAP.7) requires only two signals (with the possibility for encoding the optional test reset function onto these). Further, with regard to functionality enhancement, it is expected that, in many cases, extended signaling needs for uses such as applications debug can be met on no more than two pins.

Even while delivering these benefits, 1149.7 has taken great pains to preserve the investment that the industry has made in 1149.1 for chips and on boards. Particularly, 1149.7 adopts the entirety of the 1149.1 boundary-scan architecture to fully support board test and in-system configuration. Further, 1149.7 does not replace 1149.1, but rather adapts it and extends it, building upon its foundation and legacy. For example, as illustrated in Figure 1, an 1149.1 chip can be adapted easily to provide a TAP.7. As well, TAP.7s can coexist with TAP.1s on boards and, in some cases, even on the same board-level TAP connections.

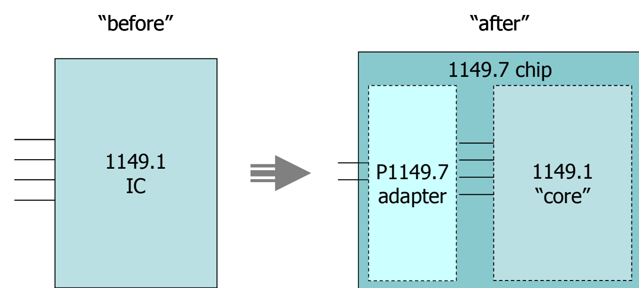


**Figure 1—Adaptation of 1149.1 to 1149.7**


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## 1.2 IEEE 1149.7 Key Objectives

The key objectives for 1149.7 fall broadly into three categories – system architecture, applications debug, and legacy infrastructure (to include test).

Benefits for system architecture derive from the appropriate accommodation of multiple on-chip embedded TAP Controllers (EMTAPC), the reduction of pins, the adoption of glue-less star topology, independence from CPU/debug technology, and provisions for power management. Where intellectual property (IP) blocks may each contain EMTAPCs, multiples of these may be accommodated on a complex system-on-chip (SOC).

While reduced pin count has inherent value with respect to miniaturization, consider as well that, in combination with the star topology, fewer pins better support the new 3D packaging methodologies such as system-in-package (SIP). These typically involve the stacking of die as shown in Figure 2; conversely, a daisy-chaining implementation is not only more difficult but also is not 1149.1 compliant. Of course, the same can be said for package-on-package (POP). Further, independence from particular CPU/debug technologies supports similar integrations even where chips may incorporate CPU IP from multiple sources. Facilities that permit the test logic to enter power-down modes support increasingly aggressive power management requirements.

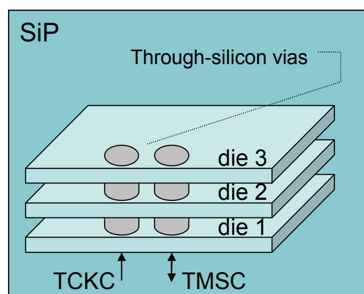


**Figure 2—Star topology for a 3-die SIP**

For applications debug, the TAP.7 provides advanced capability that reduces or eliminates the need for signaling beyond the two wires. Extensions provided include robust hot connect, increased throughput by way of scan optimization, higher operating frequency, and transport of background instrumentation data and/ or custom protocols. Of course, independence from CPU/debug technology also accrues here because uniform tool sets can support chips with heterogeneous CPUs.

Finally, as concerns the legacy infrastructure, the objectives are two-fold – first, honor 1149.1 by preserving the test infrastructure that has been built up around it and on which the industry depends; and second, maintain a level of compliance such that existing intellectual property in chips, on boards, and in debug and test systems (DTS) can be adapted at low cost.

# 2. Overview/ How it Works

At the highest level of abstraction, 1149.7 provides for a chip-level TAP.7 Controller that bridges the conventional 1149.1-accessible System Test Logic (STL) to the four (five) or two (three) wires of the chip-level TAP.7 (the test reset signal is optional in either case). The STL has its own 1149.1 chip-level TAP Controller (CLTAPC) and all of the associated test logic architecture, including a chip-level boundary-scan register and related EXTEST, PRELOAD, and SAMPLE instructions.

Seeking to extend 1149.1 in a compatible fashion, 1149.7 starts with the observation that the TAP Controller (TAPC) at the core of 1149.1 is a two-wire control means, even in the conventional series topology, as shown in Figure 3.

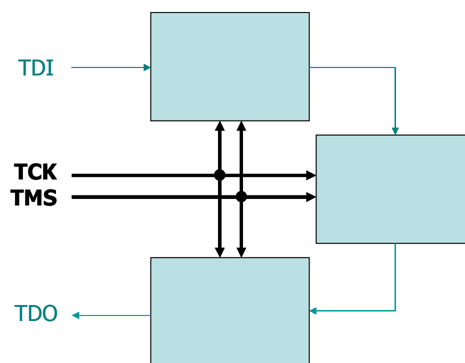


**Figure 3—Conventional series topology, highlighting the star wiring for TCK/TMS**

Per 1149.1 convention, the starred TCK/TMS can only advance the TAPC state, which in turn invokes TDI/TDO for scan operations, but, absent instruction register scans, does not change the mode of the test logic. Thus, the key concept of 1149.7 continues with the observation that control extensions might be overlaid on *sequences* of TAPC states (more details on this later).

Thus, 1149.7 adds its own commands and registers on which the other layers of extended functionality are based. These additional layers add scan formats, direct addressability, packetization of scan data (TMS, TDI, and/ or TDO information) onto the TMS wire (hence, re-designated TMSC), and finally packetization of non-scan information onto TMSC to provide for transport of background and/ or custom data.

As such, 1149.7 supports a number of capability classes (six in number, designated as T0 - T5). So the TAP.7 Controller is configurable to support the required capability for a given implementation. The primary functional units are illustrated in Figure 4 and are designated as follows: Advanced Protocol Unit (APU), Extended Protocol Unit (EPU), Pin-Sharing Logic (PSL), and Reset and Selection Unit (RSU). The manner in which these items are invoked (or not) for given capability classes will be described in subsequent sections.


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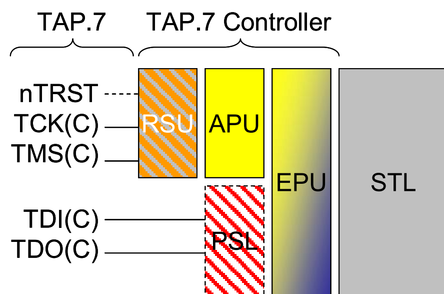


Figure 4—Notional view of the 1149.7 architecture

## 2.1 Capability classes

Regardless of which capability class is implemented, a given TAP.7 must implement all of the mandatory features of its own class as well as those of all lower-numbered classes (T0 < T5). The classes are generally considered in two primary groupings: those which extend 4-wire operation (T0 – T3) and those which provide the reduced-pin, 2-wire operation (T4 – T5).

### T0–foundation

As the foundation of all TAP.7 capabilities, T0 begins with 1149.1-Specified behavior, such that the T0 STL is 100 percent compliant to 1149.1 including provisions for the mandatory chip-level boundary-scan architecture. With 1149.7 T0, the chip-level device identification register becomes mandatory.

Of the TAP.7 Controller elements shown in Figure 4, only the RSU is permitted as an option; the other items are reserved for higher classes.

Where the RSU is implemented, this would be done, as for any other class, to permit Escape Sequences and/ or Selection/Deselection Alerts to be available to manage the sharing of TAP.7 signaling across technologies and topologies. When the TAP.7 Adapter TAPC (ADTAPC) is deselected, the CLTAPC will be parked. These topics will be addressed in greater detail with T3 where the RSU becomes mandatory.

Of particular note, even where the chip has multiple EMTAPCs, as might be the case for a complex SOC that implements a mix of several core IP blocks, the T0 STL shall provide 1149.1-Specified behavior from the Test-Logic-Reset TAPC state. 1149.7 identifies several means by which EMTAPCs can be selected under the control of the CLTAPC. A further method is defined for managing multiple die-level TAPCs in a similar manner for SIP.

### T1–commands and registers

With T1, the 1149.7 mechanism providing extended control by way of TCK/TMS is invoked to access 1149.7 commands and registers. These functions pertain to the EPU as illustrated in Figure 4. So, the EPU block of the TAP.7 Controller is present for T1. Otherwise, excepting the RSU, as for T0, all other blocks are reserved for higher classes.

As described earlier, the extended control mechanism operates without disruption to the conventional 1149.1 TAPC state machine. Rather, it uses a particular state sequence, which is benign to normal 1149.1 operations, to initiate 1149.7-defined action.

The state sequence of interest is known as a zero-bit DR scan (ZBS) and these are to be operated only while all of the CLTAPCs in the selected topology operate BYPASS or IDCODE so as to ensure that they do not disrupt normal system operation. In fact, ZBS detection is validated only when no IR scans have intervened since the last occurrence of the Test-Logic-Reset TAPC state.

The progression of states that is recognized as a ZBS is illustrated in Figure 5.

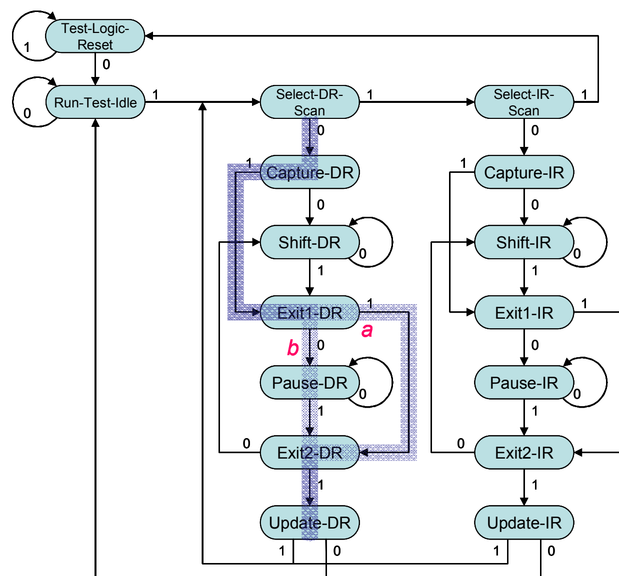


Figure 5—Zero-bit scan (ZBS)

There are actually two different paths, labeled as "a" and "b" in Figure 5, that can implement a ZBS. In either case, the state sequence of interest is defined as follows: from the Select-DR-Scan TAPC state, proceed to the Update-DR TAPC state without passing the Shift-DR TAPC state.

From the Test-Logic-Reset TAPC state, wherein the ZBS count is set to zero, the extended control mechanism is initiated when at least two ZBSs are detected before a subsequent non-zero-bit DR scan, which locks the ZBS count. A locked ZBS count of two provides access to the 1149.7 commands and registers. Locked ZBS counts greater than two access higher control levels that will not be detailed here.

Once the ZBS count is locked, and a control level set, it is only unlocked when the control level is exited by entry to either the Select-IR-Scan or Test-Logic-Reset TAPC states or by certain 1149.7 commands and events that are used to synchronize T4 and T5 operations.

At control level 2, commands are recognized, without the use of TDI/TDO pins, by counting the number of TCK(C)


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ticks in the Shift-DR TAPC state for two scans that immediately follow the completion of the non-zero-bit DR scan that locked the ZBS count. Each of these two primary command words is coded in 5 bits, ensuring that these counts need not exceed 31. All commands include two such parts for a total code length of 10 bits. In most cases, the command and register operations are concluded in these two parts but in some (only three) special cases a third part (a DR scan of a length determined by the control register addressed by the command) is required.

T1 mandates a given minimum set of such commands and the registers that they address. Additionally, some commands, registers, and associated functions are optional, notably those that invoke directed test reset generation and request for functional reset.

Additionally, T1 provides for power management through four modes of power control for the test logic. These four modes are: allow power down if TCK stops at logic one for more than 1 ms, allow power down if TCK stops at logic one for more than 1 ms in the Test-Logic-Reset TAPC state, allow power down if the device is in the Test-Logic-Reset TAPC state, and do not allow power down (the test logic is always powered).

Given that a power-down mode is supported, the test logic is directed to resume powered operation when the Run-Test/Idle TAPC state is forced for at least 100 ms and at least 3 TCK(C) ticks.

**T2–scan formats**

The 1149.7 scan formats are introduced in T2. A T2 TAP.7 supports JScan0 – JScan2; other scan formats are reserved for higher classes.

Of the TAP.7 Controller elements shown in Figure 4, for T2, as for T1, only the EPU is mandatory with the RSU permitted as an option; the other items are reserved for higher classes. For T2 versus T1, the EPU adds the commands and registers associated with the scan formats.

As regards the function of these scan formats, JScan0 provides 1149.1-Specified behavior while JScan1 provides for the deselection of the CLTAPC in favor of a 1-bit scan path (so-called Super Bypass) that is active for IR scans as well as DR scans and JScan2 provides for activation/deactivation of the Super Bypass according to the value of an 1149.7 register.

A T2 TAP.7 can opt either for JScan0 or JScan1 as its startup behavior. The latter case is described as providing hot-plug immunity since it should permit live connection (or disconnection) of the TAP.7 signals to be non-disruptive to the test logic.

**T3–direct addressability**

Finally, with T3, the star topology (4 wire), as in Figure 6, is supported. This comes by adding the means for direct addressability and the JScan3 scan format that provides for scans to star-4 topologies.

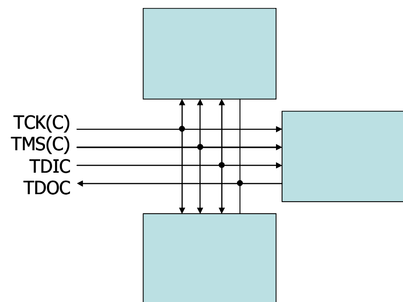


**Figure 6—Star-4 topology**

Of the TAP.7 Controller elements shown in Figure 4, T3 adds the RSU as a mandatory element in addition to the EPU. For T3 versus T2, the EPU adds the commands and registers associated with direct addressability. Note that for T3, the TDI and TDO signals are re-designated as TDIC and TDOC, respectively.

Concerning the RSU for T3, it is required to implement Escape Sequences for reset and for selection/ deselection and may optionally implement Selection and Deselection Alerts. Escape Sequences involve the detection and counting of a number of edges on TMS(C) driven while TCK(C) is held at logic 1. The count of such edges determines the action to be taken in response to the Escape Sequence. Alerts are specific predefined sequences of 128 bits as driven on TMS(C).

The resource invoked for support of direct addressability is the TAP.7 Controller Address (TCA), as shown in Figure 7. The values corresponding to DEVICE_ID are inherited from the 1149.1 device identification register capture value for the CLTAPC. The assignment of the NODE_ID is made by some implementation-specific means that is not defined by 1149.7. The NODE_ID serves to distinguish multiple TAP.7s on a given topology branch where they are of the same device type.

| MSB | | LSB |
|---|---|---|
| 34 27 | 26 11 | 10 00 |
| NODE_ID[7:0] | DEVICE_ID[27:12]<br>Part Number | DEVICE_ID[11:0]<br>Manufacturer |

**Figure 7—TAP.7 Controller Address (TCA)**

A key provision required to facilitate scans to the star-4 topology is the prevention of drive conflict on TDOC. The JScan3 format is managed so that when multiple TAP.7 Controllers are requested to participate, then drive on TDOC will be inhibited.

As discussed in more detail in 4.1, test applications require the ability to coordinate the simultaneous entry of all devices of interest into and/ or through the Capture-xR, Update-xR, and Run-Test/Idle TAPC states. At first glance, the star topology would seem not to support this requirement. But in addition to the JScan3 scan format, T3 adds the Scan Selection Directives (SSD) to deal with this matter. The SSDs make use of Pause-xR TAPC states as parking states to which simultaneous scan captures are


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directed and from which simultaneous scan updates are directed. Scan shift operations, as necessitated by the star topology are done on a device-by-device basis and are both directed from and to the Pause-xR TAPC states.

**T4–packetization of scan data (2-pin scan formats)**

With T4, a number of additional scan formats are added to support the advanced protocol, which is operated on two pins. The TCK/TMS pins are re-designated as TCKC/TMSC, respectively. The corresponding star-2 topology is illustrated in Figure 8. Note that TMSC is bidirectional.

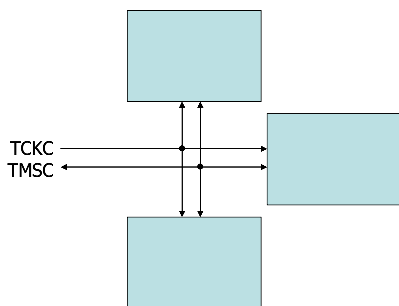


**Figure 8—Star-2 topology**

Of course, these additions require the provision of the APU of Figure 4. As well, since the TDIC/TDOC pins are optional since they are not used for 2-pin operation, where they are provided the PSL also becomes an option.

Where a T4 TAP.7 does not provide the TDIC/TDOC pins in any configuration, it is described as narrow and designated as T4N. Where a T4 TAP.7 does have a configuration that provides the TDIC/TDOC pins, it is described as wide and designated as T4W.

One of the more basic scan formats that supports the advanced protocol is OScan1. The serialization of the scan packet for OScan1 is illustrated in Figure 9. As shown, the TDI bit information is inverted. Also, for each cycle in which the TDO bit appears it is driven from the selected device in the target system back to the DTS.

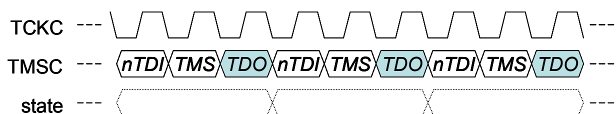


**Figure 9—Scan packet serialization – OScan1**

Other scan formats in the OScan series provide for optimizations in which the scan packets omit bits that can be known to carry no significant information. An example worth noting is the OScan7 format which is optimized for downloads from the DTS to the target system. For OScan7, as illustrated in Figure 10, only the TDI bit information is included in the packets sent during Shift-xR TAPC states.

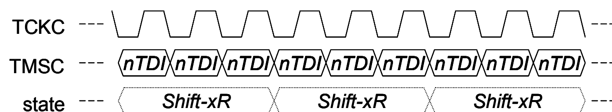


**Figure 10—Scan packet serialization – OScan7**

Further performance optimization that can be obtained for T4 is by invoking falling-edge sampling for TMSC which, presuming hold times still can be met, delivers a degree of improvement in setup times that would allow the TCKC frequency to be increased (perhaps doubled).

**T5–transport of non-scan data (2-pin mode)**

At the top of the classes, T5 offers the capability to interleave transfers of non-scan data among the scan transfers. This is referred to as transport and has two variants – background data transport (BDX) and custom data transport (CDX).

Both types of transport can use any combination of Run-Test/Idle, Pause-xR, and Update-xR TAPC states after which to insert transport packets. The distinction is that, whereas BDX has fixed allocation of I/O bandwidth available to the chip-level data channel, CDX has a custom allocation of I/O bandwidth as determined/ defined by the chip-level unit.

## 2.2 Selection hierarchy

While some aspects of the selection hierarchy have been described above, some additional detail is warranted as it is a key aspect of the 1149.7 system architecture.

In general, where selection is enabled within the hierarchy, those items not selected are effectively offline/ parked and respond only to particular selection requests on the TAP.7 signaling. Those that are selected are online and respond to the TAP.7 signaling according to the protocols for which they are configured.

Five levels in the selection hierarchy are elaborated below. For each level of the hierarchy, one or more selection mechanisms may pertain.

- Technology

  Where the 1149.7 technology can be placed offline, the TAP.7 signaling can be shared with other technologies

- Topology

  Where the constituent 1149.7 devices can be placed offline (a function required for T3 and above), the TAP.7 signaling can be shared among any topology branches, whether series, star-2, or star-4

- Adapter (i.e., ADTAPC)

  1149.7 devices comprising a selected topology branch will share TAP.7 signaling and, where the topology branch is star-2 or star-4, a given device may be selected for a given operation


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- Chip (i.e., CLTAPC)

  For a selected ADTAPC, the CLTAPC may be offline and will require selection when it must be operated

- Core (i.e., EMTAPC)

  For a selected CLTAPC, given EMTAPC(s) of interest may be offline and will require selection when it (they) must be operated

## 3. Implications for Debug

In many respects, 1149.7 was defined by and for the debug community. Thus, many of the implications, considerations, and supporting features have already been addressed in the elaboration of the basic 1149.7 functions as described above. Still some of these bear specific mention in this context.

### 3.1 Debug considerations

Chief among the considerations for debug are ease and efficiency. Of course, these unfold across multiple dimensions and are often intertwined.

**Ease**

The highest degree of visibility and control is required to drive the analysis tools that can get to the bottom of thorny problems that arise in today's multi-threaded, multi-core, real-time embedded systems. 1149.7 promises to bring value to this equation by consolidating debug access for multiple cores onto a smaller number of chip pins.

Other features tending toward ease of debug are the hot-plug immunity and system interrogation.

**Efficiency**

Certainly 1149.7 enjoys a performance boost relative to 1149.1 with its various optimizations for scan throughput and its ability to improve link utilization by using otherwise idle non-scan states to transport background instrumentation data.

### 3.2 Debug features

As one would expect, 1149.7 brings a wealth of features to address debug ease and efficiency.

**Access consolidation**

Several aspects of the 1149.7 system architecture provide for access consolidation: management of EMTAPCs (T0), star topology (T3), pin reduction (T4N/T5N), and capability for the TAP.7 to transport background data and custom protocols (T5). All of these result in making debug instrumentation more accessible and, hence, easier to use.

**Hot-plug immunity**

Live connection without system disruption is vital and is enabled by the offline at startup (T3 or any with RSU) and Super Bypass at startup (T2) features.

**System interrogation**

A method for topology interrogation (T3) is provided and enumeration of controllers can be made by undirected allocation of Controller IDs (CID) (T3), as in Figure 11. These features allow the system architecture to be discovered by the debug tool at connect time.

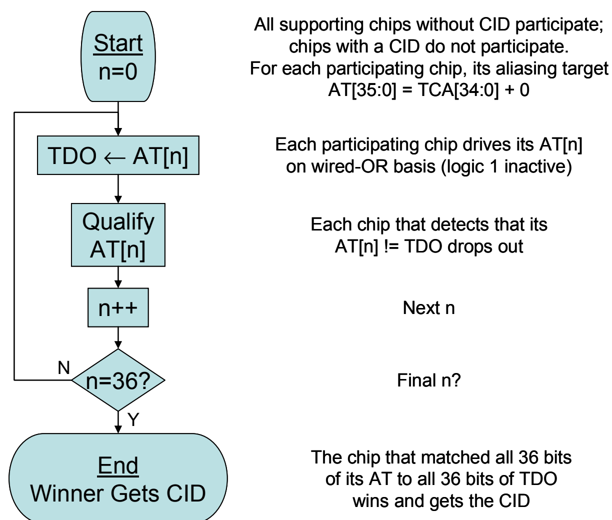


**Figure 11—CID Allocation, Undirected**

**Optimization of scan throughput**

Perhaps above all, 1149.7 offers a great number of opportunities to optimize scan throughput. Super Bypass (T2) results in shorter scan chains for series topology. Star topology (T3) offers direct addressability and, hence, scan operation in only the target of interest.

Advanced protocol (T4) offers still further improvements based on scan packet optimization on one hand and falling-edge timing (and thereby clock doubling) on the other.

**Improved link utilization**

BDX and CDX (T5) allow the link to be used for transport of instrumentation data even during non-scan states, which would otherwise be idle.

## 4. Implications for Test

While 1149.7 primarily has been developed for the benefit of applications debug, it also has gone to considerable lengths to ensure that the test legacy of the original 1149.1 is honored. Among the several test-related provisions are the scan selection directives that ensure update/ capture/ run-test synchronization and the definition of suitable test languages.

### 4.1 Test considerations

While 1149.7 does not change radically how 1149.1 boundary scan/ test is being used today, there are some new considerations for test that arise with the 1149.7 architecture. Primary among these are the divergence in


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scan-state sequencing and series/star interoperability. Other considerations worth mention are hierarchical navigation, power control, and large-system applications.

**Scan-state sequencing**

The typical test application has requirements for scan-state sequencing that necessitate coordination of application of stimuli across multiple distinct components (with their own boundary-scan registers) on a given unit under test (UUT). Consider the case where several components have distinct 3-state outputs on a shared wire junction. If the distinct output control cells in each of these components were not updated in a coordinated fashion, a contention could be present on the shared wire. The simplest means of such coordination is to ensure that all components pass simultaneously through the Update-DR TAPC state.

As well, while it might not be necessary in some cases, the coordination of the acquisition of response generally also is required (or at least preferred). At the least, where specific response to given stimuli is required, the distinct responses for each component involved must all be acquired before the applied stimulus is changed. Here again, the simplest means for such is to ensure that all components pass simultaneously through the Capture-DR TAPC state (in fact, simultaneity may be strictly required in some special cases).

Some test applications, such as the testing of advanced digital networks per IEEE Std 1149.6, have an additional requirement that all components participating in such testing must pass simultaneously through the Run-Test/Idle TAPC state.

Conventional scan sequencing for test applications presuming series topology is illustrated in Figure 12.

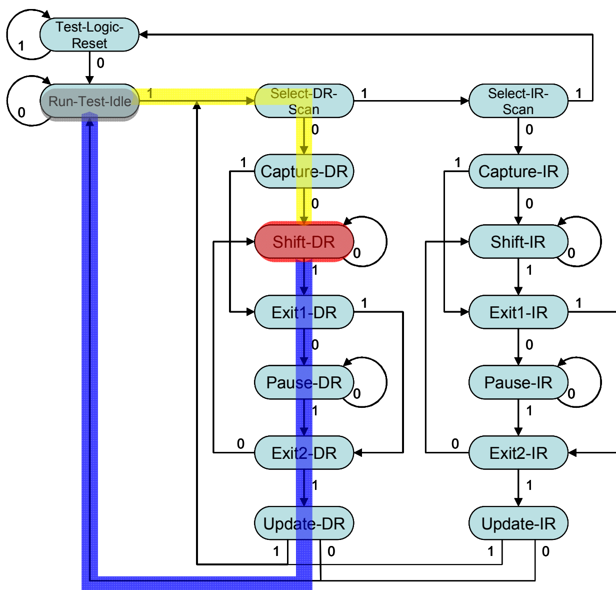


**Figure 12—Scan-state sequence (conventional) for test applications, series topology**

This conventional scan-state sequence can be broken down as follows:

- (in yellow) all components on the UUT (series topology) pass through the Capture-DR TAPC state wherein responses (to a previously applied stimulus) are acquired in concert
- (in red) all components on the UUT (series topology) enter and remain in the Shift-DR TAPC state until all responses have been exported and all new stimuli have been imported
- (in blue) all components on the UUT (series topology) pass through the Update-DR TAPC state wherein new stimuli are applied in concert
- (in grey) all components on the UUT (series topology) dwell in/ pass through the Run-Test/Idle TAPC state wherein transient stimuli may be generated in concert

The divergence introduced by the 1149.7 star topology is that, due to shared wiring of TDIC and TDOC for star-4 or TMSC for star-2, only one component may be operated in the Shift-DR TAPC state at a time.

Fortunately, we can take from the above discussion that the Shift-DR TAPC state is actually neutral to the requirements of the test application. Thus, the needs of the test application can be served, even for a star topology if each of the TAPC states Capture-DR, Update-DR, and Run-Test/Idle can be operated in concert across all of the UUT components of interest.

It is for just this purpose that the scan selection directives (SSD) were devised. Figure 13 illustrates the scan-state sequence made possible by the SSDs (star topology).

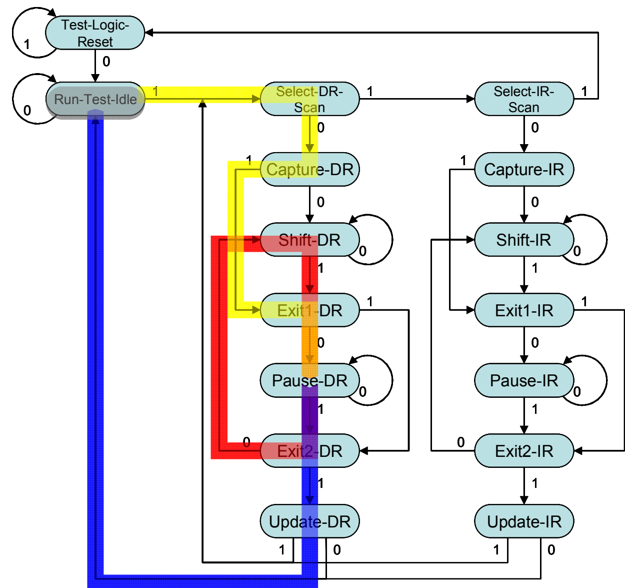


**Figure 13—Scan-state sequence for test applications, modified for star topology**


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This modified scan-state sequence can be broken down as follows:

- (in yellow) all components on the UUT (star topology) pass through the Capture-DR TAPC state, wherein responses (to a previously applied stimulus) are acquired in concert, and then on to Pause-DR
- (in red) each component on the UUT (star topology) is brought, one at a time, from Pause-DR to enter and remain in the Shift-DR TAPC state until its responses have been exported and its new stimuli have been imported, and then back to Pause-DR; this step is repeated once for each component of interest to the test application
- (in blue) all components on the UUT (star topology) pass through the Update-DR TAPC state, wherein new stimuli are applied in concert, and then on to Run-Test/Idle TAPC state
- (in grey) all components on the UUT (star topology) dwell in/ pass through the Run-Test/Idle TAPC state, wherein transient stimuli may be generated in concert

The use of this same sequence can be extended beyond just one star topology to include several distinct star topologies (such as with separate TCK) and even further to accommodate a mix of series topologies with star topologies on the same UUT.

**Hierarchical navigation**

Another consideration for test involves the divergence that results from the introduction of selection hierarchy throughout 1149.7-based systems. These layers are technology, topology, adapter, chip, and core, as detailed in 2.2. A test application must navigate these layers using their respective selection mechanisms to access the desired TAPCs wherever they may reside in the hierarchy.

**Power control**

A further consideration for test arises concerning control of the power-down modes to avoid inadvertent loss of power to components required to support the test application. When one or more of the components of interest implement a power-down mode, this DTS must issue a directed power-up request to bring it (them) out of Test-Logic-Reset TAPC state. This involves forcing TMS(C) to 0 for at least 100 ms followed by at least 3 TCK(C) ticks in the Run-Test/Idle TAPC state.

**Considerations for large-system applications**

Whereas debug typically involves a small-system view (even where the system of interest may be part of a much larger system), test applications often involve large systems. These may comprise large printed circuit boards (PCB) and/or collections of many such PCBs.

Some aspects where large-system applications (such as for test) contrast versus small-system applications (such as for debug) include: the numbers of components (great versus few), the dispersion of components (spread across many substrates, e.g. PCBs, versus on a single substrate), the available real estate for access to TAP signals (plenty versus limited), and the logical and electrical constraints on connectivity (many devices/ loads versus few).

As a result, for some large-system applications, the star-2 topology may not provide adequate connectivity. Furthermore, an abundance of real estate may render the reduced-pin TAP.7 unnecessary. Where such factors can be known in advance, system architects may wish to consider them in regards to the specification of supported topologies.

## 4.2 Test languages

Recognizing that a set of description files is required to support test applications, 1149.1 introduced the Boundary-Scan Description Language (BSDL), hereafter referred to as BSDL.1. Likewise, 1149.7 recognizes the need for additional description elements and so has offered its own BSDL derivatives.

Consider the example 1149.7 component illustrated in Figure 14. The items identified as “Chip A” and “Chip B” are further identified as test endpoints, signifying that they each contain a single CLTAPC that exposes a single boundary-scan register for external test. The embracing item is identified as a test module because it must necessarily contain more than one CLTAPC and must expose more than one boundary-scan register for external test.

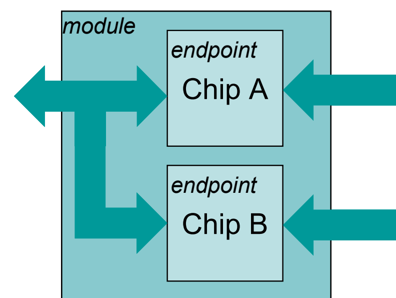


**Figure 14—Example 1149.7 component comprising a test module with two test endpoints**

Note that according to the above classification criteria, a test endpoint could be one that provides 1149.1-Specified behavior just as well as one that provides 1149.7-Specified behavior. Thus, as a corollary to the BSDL.1, 1149.7 has specified a BSDL variant (BSDL.7) for test endpoints.

In contrast to 1149.1, 1149.7 has expressly considered hierarchy within its bounds. Consider that an item classified as a test module per the above criteria can be one that provides 1149.7-Specified behavior. In fact, in the general case, a test module is defined as a collection of test endpoints and other test modules where TAPs are connected to define a scan topology.

Since test modules can contain other test modules as subcomponents, a hierarchy is formed. While the simplest


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test module contains one or more devices connected into a single scan topology, more complicated test modules can represent multi-chip modules, etc. Thus, the need for a new, hierarchical description has been recognized and the 1149.7 Hierarchical Scan Description Language (HSDL.7), based on BSDL.7, has been defined.

With the combination of BSDL.7 and HSDL.7 descriptions as identified above, and a top-level netlist for the given UUT, test software can extract scan chain topology and other connection information needed for test generation. The inclusion of component-to-component functional connections in the HSDL.7 provides for the testing of intra-module connections where possible.

**Describing 1149.7 test endpoints–BSDL.7**

As for BSDL.1, the BSDL.7 model of a component (test endpoint) is effectively an electronic data sheet for parameters of the test logic that may vary from one component to another. As 1149.7 has added some new parameters that may vary from chip to chip, these need to be accommodated in the BSDL.7. Otherwise BSDL.7 derives entirely from the BSDL.1.

Figure 15 presents the attributes that are new for BSDL.7 (versus BSDL.1).

```
attribute COMPONENT_CONFORMANCE_ADAPTER
attribute COMPONENT_CONFORMANCE_STL
attribute TAP_CLASS
attribute TAP_SCAN_CLOCK_COMPACT
attribute TAP_SCAN_MODE_COMPACT
attribute TAP_SCAN_IN_COMPACT
attribute TAP_SCAN_OUT_COMPACT
attribute TAP_SCAN_RESET_PD
attribute CNFG0_REGISTER
attribute CNFG1_REGISTER
attribute CNFG2_REGISTER
attribute CNFG3_REGISTER
```

**Figure 15—Attributes added for BSDL.7**

Taken together, the BSDL.7 attributes COMPONENT_CONFORMANCE_ADAPTER and COMPONENT_CONFORMANCE_STL replace the BSDL.1 attribute COMPONENT_CONFORMANCE and, respectively, indicate the conformance level of the TAP.7 (which is governed by 1149.7) and of the system test logic (which is governed by 1149.1).

As a group, BSDL.7's new TAP_CLASS and TAP_SCAN attributes augment the existing BSDL.1 TAP_SCAN attribute. As appropriate for the supported class, these complete the description of the TAP.7 (scan port) to comprehend its possible extensions relative to the TAP.1, whether narrow or wide, falling edge timing, etc.

The BSDL.7 attributes that begin with CNFG are completely new. These allow the content of the 1149.7 configuration register to be expressed. The bit values contained within the BSDL.7 can be mapped out to determine all of the chip-specific capability options.

**Describing 1149.7 test modules–HSDL.7**

An HSDL.7 model of a component (test module) likewise is effectively an electronic data sheet for the parameters of the test logic that may vary from one component to another. Of course, the parameters that are of interest to HSDL.7 are those that pertain to test modules, versus those that pertain to test endpoints for BSDL.7 (which are omitted as appropriate).

Figure 16 presents the attributes that are new for HSDL.7 (versus BSDL.7).

```
attribute COMPONENT_CONFORMANCE_MODULE
attribute MEMBERS
attribute MEMBERS_PORTMAP
attribute MEMBERS_NODEIDS
```

**Figure 16—Attributes added for HSDL.7**

Attribute COMPONENT_CONFORMANCE_MODULE of HSDL.7 replaces those for BSDL.7 with prefix COMPONENT_CONFORMANCE_ and correspondingly indicates the conformance level of the test module (as opposed to the TAP.7(s) and/ or STL(s) of its constituent subcomponents).

As a group, the HSDL.7 attributes that begin with MEMBERS are completely new. These list the subcomponents of the test module, describe how these subcomponents are interconnected, and assign NODE_IDs to the subcomponents, as needed. When combined with the DEVICE_ID information from the associated BSDL.7 file(s), the full TCA(s) of the test endpoints can be determined.

## 5. Conclusion

IEEE 1149.7 ratifies a test and debug interface that is a complementary superset of the venerable IEEE 1149.1 (JTAG) TAP. By way of options for reduced pins and for enhanced functionality, 1149.7 offers an access mechanism that is well suited to interfacing multiple cores on SOC or to interfacing multiple die in SIP or multiple packages for POP.

While the enhanced functionality is necessary to support the reduced-pin access capability of 1149.7, it also provides a number of features that improve the debug process. Such features include hot-plug immunity, power management, optimization of scan throughput, access to debug instrumentation, and access to custom debug technologies.

Still, the enhanced functionality and the reduced pin capability are deployed in such a way as to maintain compatibility for test. It will be possible for chips that have IEEE 1149.7 TAPs to reside on modules and boards with chips that have IEEE 1149.1 TAPs and, further, for


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the test logic in these chips to interoperate to perform a test application (e.g., boundary scan) that spans these chips.

Finally, it is expected that, even though 1149.7 is, indeed, a new standard, it will have a leg up with regards to adoption by industry due to its having been laid solidly on the foundation of 1149.1. In effect, 1149.7 already has a presence in the marketplace thanks to its ancestor, 1149.1. In fact, the significant infrastructure already in place for 1149.1 will be leveraged to bring 1149.7 solutions to market in short order.

## 6. Acknowledgements

The author acknowledges all those involved in the P1149.7 working group, without whose effort a standard would not have been realized. A further recognition goes to Stephen Lau of Texas Instruments, upon whose training and education materials this embedded tutorial/ paper has drawn. Finally, and most especially, the author thanks Gary Swoboda of Texas Instruments, who shall be recognized as the technical architect and principal author of 1149.7.

## 7. Disclaimer

Where discrepancies between the descriptions presented herein may arise with respect to the ratified IEEE Std 1149.7, the latter shall be considered authoritative. If any such errors are present, they should be considered the sole responsibility of this author.

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