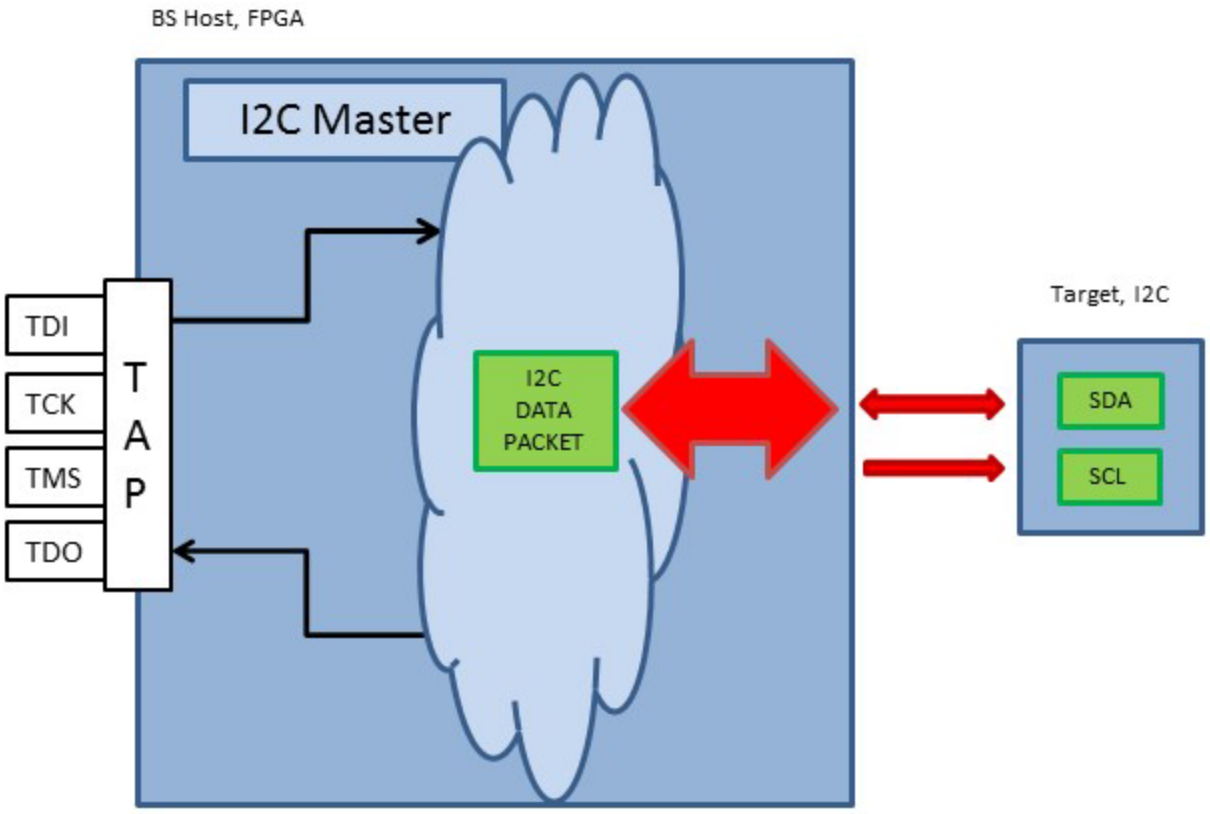
I2C Interface Test with FPGA IP and JTAG



eBook

BY KENT ZETTERBERG

ASSET

ScanWorks®
Platform for Embedded Instruments

By Kent Zetterberg – Product Manager

Kent Zetterberg started his career in the automation industry, working with systems from ABB, Siemens and others. Following graduation from the University of Gävle with a Bachelor's of Science Degree in Computer Engineering, he worked 15 years in the telecom industry where he held various positions involving hardware test and debug. He joined Ericsson AB in Sweden in 1997 where he developed functional test programs for processor boards, and designed interface boards and test fixtures. At Ericsson he became an expert in boundary scan and eventually led the boundary scan team. With ASSET Kent has held several positions in support, serving as a customer trainer and European support team leader. Currently he is the technical product manager for ScanWorks boundary-scan test products.

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Executive Summary

A circuit board doesn't have to be operational for functional tests to be applied to its I2C (Inter-Integrated Circuit) interfaces. In fact, the board doesn't have to boot and its functional firmware/software can be a long way from complete. The ability to perform at-speed functional I2C tests on non-functional prototype circuit boards can save the design and manufacturing test teams' significant time and reduce costs accordingly. Specifically, engineers no longer need to spend a tremendous amount of time and effort developing traditional functional tests – a time consuming process in itself. They can employ boundary-scan test structures as well as re-useable intellectual property (IP) inserted into a field programmable gate array (FPGA) to quickly determine whether the design's I2C interfaces are functional. If they are not, engineers will have much better fault diagnostic information than they would have had from the severely limited traditional functional tests of the past.

This eBook explains boundary-scan-based (IEEE 1149.1 / JTAG) methods for the testing of I2C interfaces without functional software or traditional functional tests. The overall methodology begins at the structural level with boundary-scan tests that verify the integrity of the board's I2C interconnects by detecting any shorts and opens. This would be followed by at-speed verification and testing with embedded instrumentation IP inserted into an on-board FPGA.

With this methodology products are delivered to market faster because of the benefits of concurrent engineering. In addition, hardware and software development costs are reduced through re-use and programming time decreases since traditional functional tests need not be developed. Serial ports like I2C, SPI and UART can be tested with the same boundary-scan controller hardware that's likely already present in the test fixtures. And, the serial interfaces can be functionally tested even though the software development department may still be developing the product's functional firmware. This methodology lets system manufacturers decouple the functional testing of serial interfaces from functional firmware development. Instead of functional test following firmware development in time, both processes can take place concurrently. Plus there's the added benefit that the test IP temporarily inserted into an on-board FPGA can be replicated and re-used again and again on successive designs.

Introduction

During the prototype phase of a new printed circuit board (PCB), design engineers often face the challenge of having to verifying serial communications interfaces such as I2C, UART (Universal Asynchronous Receiver/Transmitter), SPI (Serial Peripheral Interface) and others as soon as possible. Promptly verifying the functionality of prototypes PCBs and finding design faults is critical for moving the product into manufacturing. And the sooner a new product is brought to market, the sooner it generates revenues.

Unfortunately, the time relationship between firmware development and test has been serial rather than in parallel. That is to say that functional firmware is usually needed to boot prototype PCBs so that functional tests can be applied. But the development of firmware is often not complete when the first prototypes of a PCB hardware design are available for testing and verification. Without firmware, the application of traditional functional tests had to wait for the programmers to finish their task. In addition, developing functional test programs could lengthen the prototype test and verification phase even more. Ideally, the product's functional firmware and all test programs, including functional tests, would be fully developed and available when first prototypes of hardware arrive. This is rarely – if ever – the case.

Now though, new solutions are available to allow functional testing of serial interfaces like I2C at their operational speeds without booting the system or installing functional firmware. By temporarily configuring an on-board FPGA with test-specific IP these interfaces can now be tested independently of other functional firmware or software. These methods allow prototypes to be verified sooner and the amount of test-specific software test engineers have traditionally developed for each and every design could also be reduced. In general, boundary-scan-based test methods are usually repeatable from one generation of a design to the next. Also, the embedded instrumentation IP, which drives the at-speed functional tests, is portable and can typically be re-used in the same FPGA device on other designs, considerably shortening the time-to-market for multiple designs.

On-Board Structural Test

Many, if not most, digital chips, including processors, FPGAs, application-specific integrated circuits (ASIC), digital signal processors (DSP), memory controllers and other interface controllers conform to the boundary-scan/JTAG standard (IEEE 1149.1). As a result, these devices include a boundary-scan Test Access Port (TAP). Frequently, these JTAG-compatible devices are connected to less advanced system monitors and system controllers on board designs via the I2C bus interface and communications protocol. The I2C device may perform a variety of tasks, such as monitoring temperature, reading configuration data from EEPROM and DDR memories, accessing digital-to-analog converters (DAC) and analog-to-digital converters (ADC), reading real time clocks, controlling audio volume and LEDs, and more. The boundary-scan TAP on these I2C controllers gives engineers easy and fast access to these devices. And, with the information they provide, the engineering team can decide whether the system performs to specification before any functional software is executing.

Some model-based boundary-scan tools are able to re-use information about a certain I2C device so that tests for the next generation of a design with the same I2C chip can be as simple as dropping in the model and compiling the tests. At the basic structural level, these boundary-scan tests will identify shorts and opens, and verify the fundamental electrical connectivity of the interface as well as the basic functionality of the I2C protocol.

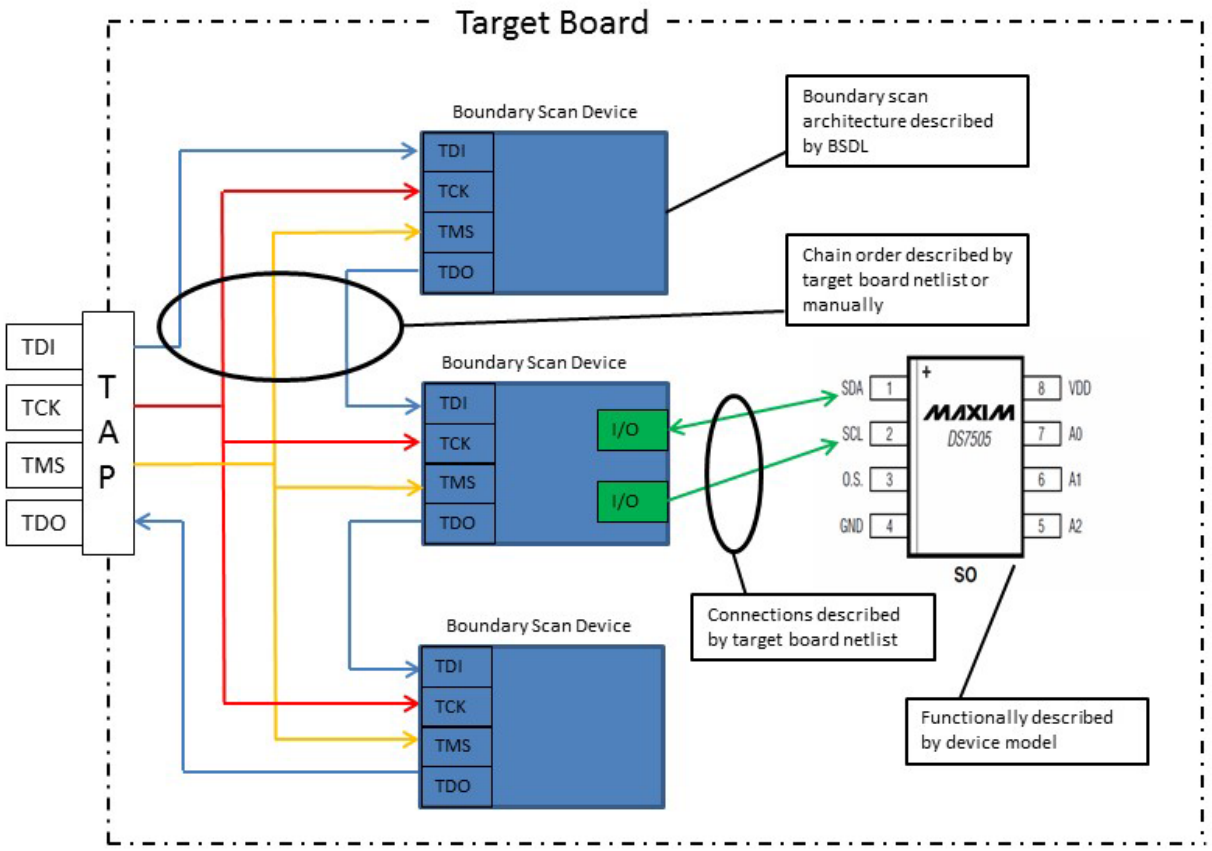


Figure 1: Testing an I2C interface with boundary-scan (JTAG)

At-Speed Functional Test

Following structural verification, I2C interfaces can also be functionally tested at-speed from embedded instrument IP inserted into an on-board FPGA (Figure 2). This embedded instrument will consist of an I2C Master synchronized to the FPGA's system clock and it will be able to exercise the I2C interface at its functional speed.

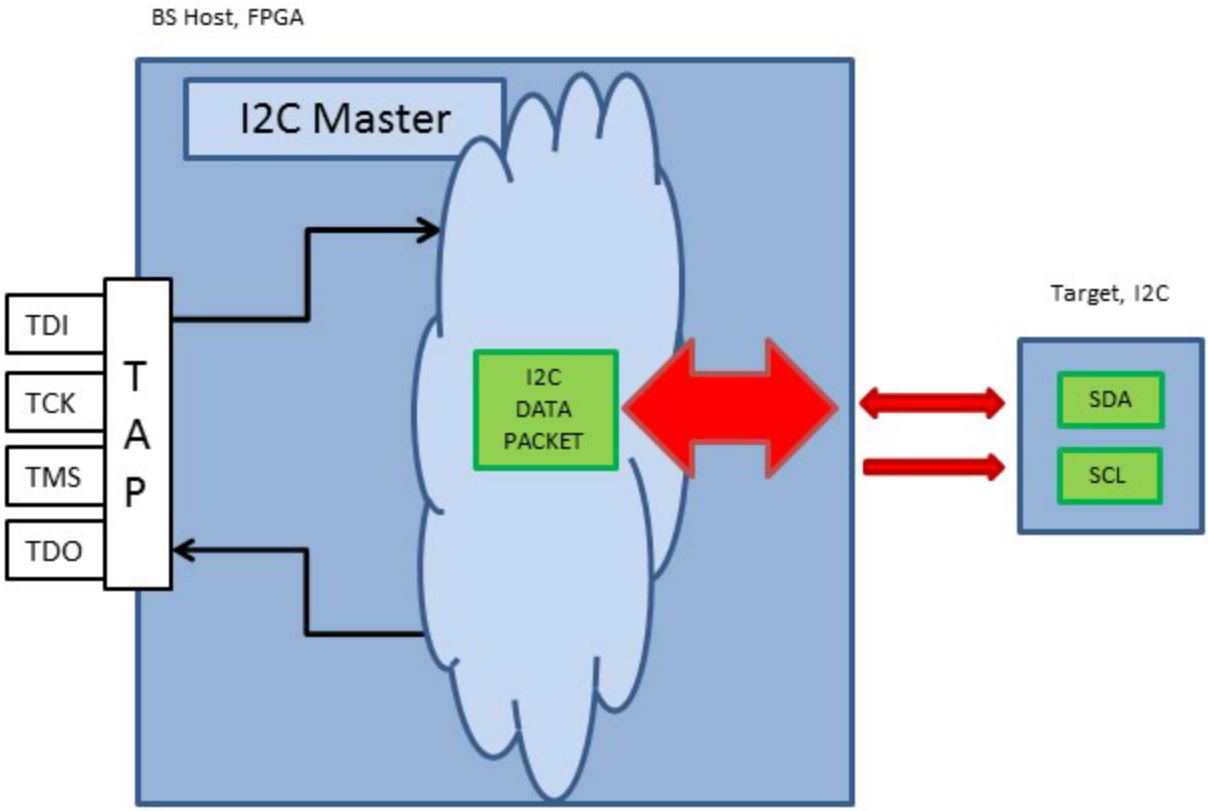


Figure 2: At-speed testing of an I2C interface from an embedded instrument in an FPGA

Before testing can begin, the FPGA must be configured with an I2C Master embedded instrument that can communicate through the boundary-scan/JTAG TAP interface on the FPGA. The I2C Master is typically inserted into an on-chip IEEE P1687 Internal JTAG (IJTAG) network of embedded instruments. This IJTAG network would support multiple instruments in the same FPGA configuration, so that many different test and measurement functions could be performed, including the functional testing of other serial interfaces like SPI and UART.

In this case, the I2C functional tests begin when a test tool or test executive communicates test data over the JTAG/IJTAG interface to the I2C Master embedded instrument in the FPGA. The I2C Master then translates this data into a serial bit stream and bit-bangs it onto the I2C interface. Typical test applications might involve moving various kinds of data through the I2C interface, such as system temperature, voltage, time of day, read configuration data from a memory device, or a DAC might be initiated and instructed to communicate analog data off the board to an

analog instrument. Below is another example of how functional data gathering through an I2C device can become a test of the I2C port.

Application Example: An I2C I/O Expander

A common example of an I2C-based functional device is an I/O expander. These types of devices are often integrated into processor or microcontroller designs to expand the available I/O without requiring more complex and expensive processors or to add other types of more expensive I/O devices to the board design. When an expander device is attached to a boundary-scan device, communications between the two devices can be easily established over I2C to read and write to the I/O ports. When the boundary-scan device is an FPGA, the communication with the I/O device can be at-speed.

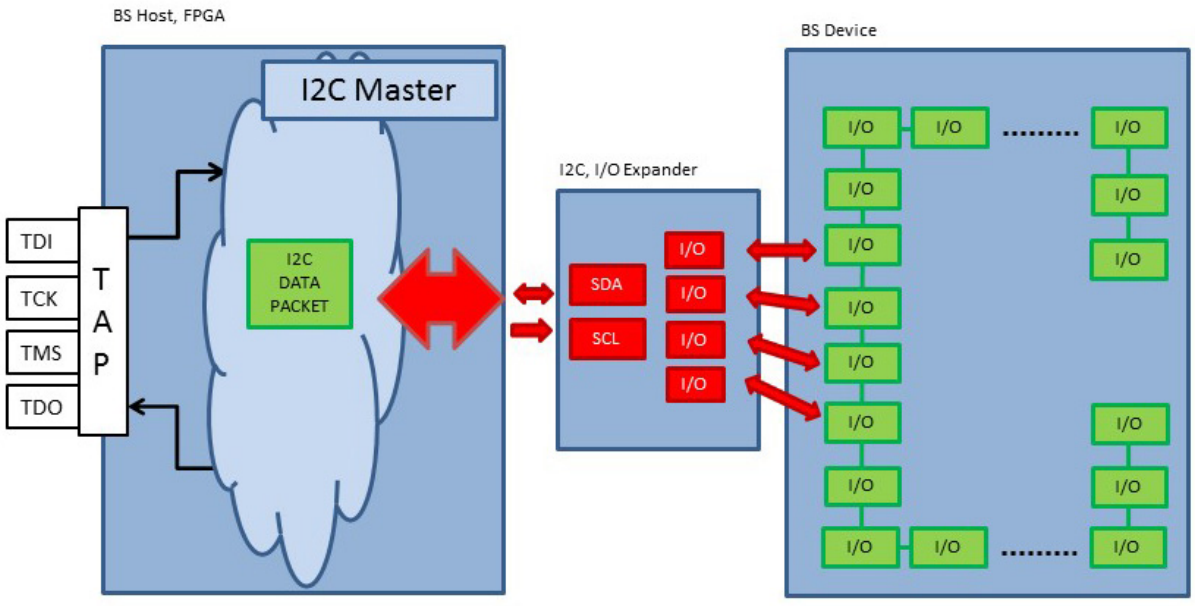


Figure 3: Configuration of an I2C-based I/O expander

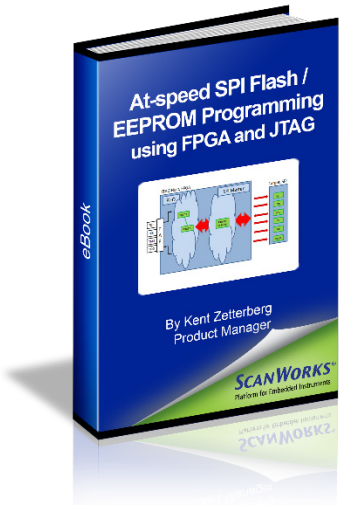
Conclusions and Learn More

Design and test engineers, as well as engineering managers, must constantly be on the lookout for new test methods that will shorten a product's overall time-to-market. One such method is concurrent engineering, which consists of multiple engineering tasks being performed in parallel rather than sequentially. The ability to perform at-speed functional tests while the functional firmware is being developed is one example of concurrent engineering. Previously, performing functional tests on prototype PCBs required functional firmware already running on the hardware. Now, several boundary-scan/JTAG-based test methods can be deployed to test and verify the structural integrity and at-speed functionality of selected interfaces without functional firmware operating on the hardware, greatly shortening the product's time-to-market.

Embedding instrumentation IP into a functional on-board FPGA enables a wide range of critical and time-sensitive tasks during development and production. For example, an embedded instrument might perform high-speed programming of SPI flash or EEPROM memory connected to an FPGA.

Learn More

Lean how to program SPI flash or EEPROM memories at high speeds. Click here.



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