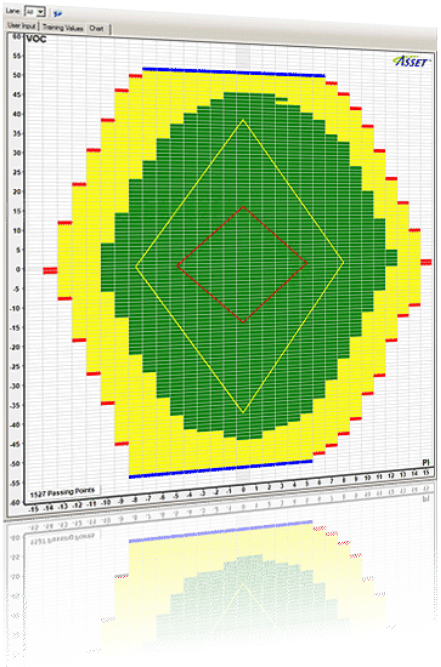
How to avoid poor SERDES performance caused by circuit board manufacturing variances



e-Book

by Arden Bjerkeli and Eric Johnson

ScanWorks®
Platform for Embedded Instruments

By Arden Bjerkeli and Eric Johnson

As Director of Customer Experience and Information Infrastructure, Arden provides the staffing, processes, tools and infrastructure that connect customers to expert support, services, and training they may need to maximize success using ScanWorks products. Arden's entire career has been dedicated to the test engineering profession. Prior to joining ASSET, Arden held director, manager, and engineering positions in the computer manufacturing industry, including Compaq, Zaisan and Telxon. Arden holds a BSEET in Computer Architecture from the University of Houston, and studied business at the University of Texas.

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Executive Summary

Validating the design of high-speed serializer/deserializer (serdes) interconnects on prototypes of a printed circuit board (PCB) does not assure that the serdes will maintain the validated level of performance once high-volume production begins. Variances in manufacturing processes can degrade performance and are all too common. The confidence that design engineers may have built up in a circuit board design by validating a limited number of prototypes can often evaporate once the board moves into production, where it is subject to manufacturing process variations. In this white paper, many of the causes of manufacturing variances are discussed, as well as potential solutions that could make validation possible during volume manufacturing and throughout a circuit board design's entire life cycle. A case study example of a typical serdes trace on a PCB and the effects of manufacturing process variations are also described.

Eroding Confidence

Confidence in the design of a serdes channel on a printed circuit board (PCB) is often based on running margining, bit error rate (BER) and other validation tests on one of the first batches of assembled prototype boards. Typically, this limited number of boards will be cycled through a range of temperatures and supply voltages to build confidence in the board. The design team must be assured that BER will remain below a certain predefined level despite variations in the manufacturing process of the chips on the board and the board itself.

Unfortunately, these confidence levels are not always well founded since they are sometimes based on a small number of manufactured PCBs from only one supplier. These boards may or may not represent the mean manufactured board over the foreseeable future during volume production. In fact, since the validated boards are usually among the first assembled, the supplier might have paid unusually close attention to higher quality, which would have made the margin of performance on the serdes appear wider than that present on boards that are produced during volume production. In addition, cost reductions over a system's life cycle can affect operating margins on circuit boards. Often, these cost reductions may save pennies per board during manufacturing, only to generate significant returns and repair costs later.

A number of variations can be expected during volume production of a PCB and many of these will affect the eye diagram of a serdes transmission line (Figure 1). This raises the question whether performing margin and BER testing only once during design validation is adequate.

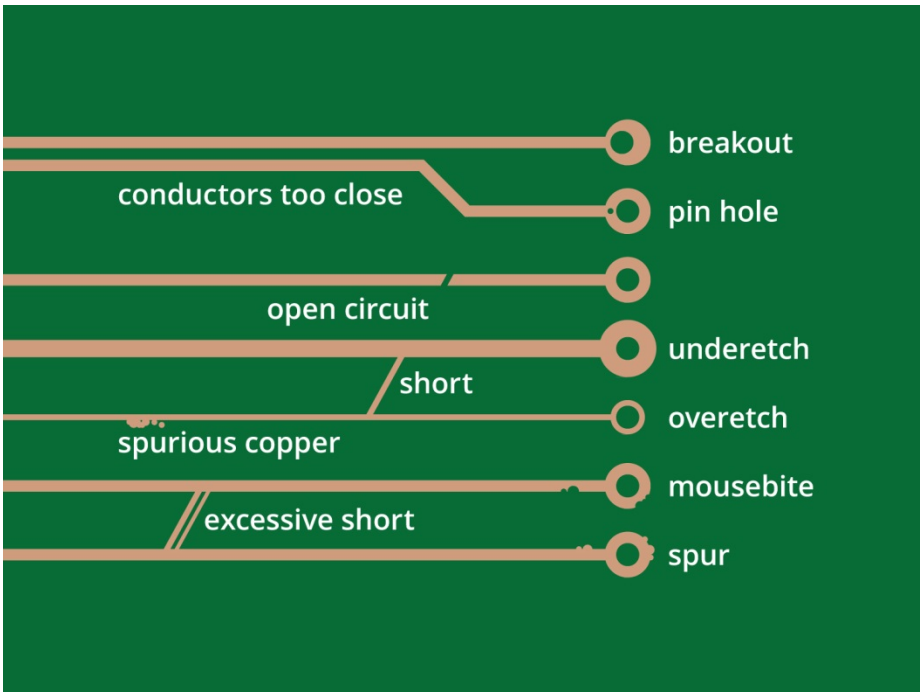


Figure 1: Manufacturing process variances can cause a number of defects.

Design Intent vs. Manufacturing Reality

Despite following all of the design rules and recommended practices in selecting the parameters for transmission line layout, variances and flaws during the production of a PCB can modify the performance of transmission circuits over an extended production run. Any one variance may not cause the PCB to fall outside the acceptable tolerance range, but the cumulative effects of several variations may downgrade the performance of a serdes line to an unacceptable level.

Most circuit boards today are designed with operating margins that allow for some variation in manufacturing processes. That is, the board will still achieve its intended performance specifications, despite variances in the manufacturing process. But, on the down side, these same techniques can make it difficult to catch marginal faults during a quick factory functional test. And traditional structural tests are not designed to catch at-speed marginal faults. As a result, structural and functional tests during volume manufacturing often do not detect faults and failures in circuit boards that result from process variances.

During design validation on prototype boards, the performance margins on a transmission line are typically measured by creating eye diagrams using oscilloscopes or embedded instruments.

Eye measurements should be run over a large sample of prototype boards from different suppliers in order to maximize confidence in the design. However, it is usually not practical to test for all possible PCB variances during design validation because other types of variances will only be manifested later, during volume manufacturing. It may be more practical to repeat validation processes throughout the life of a product to ensure that actual PCB variances have not compromised margins. Repeating eye measurements with an oscilloscope is tedious, but the emergence of embedded instruments has made this process more practical. If eye measurements cannot be repeated on all assemblies during volume manufacturing, then it should at least be done on sample lots, especially if there have been changes in prototype manufacturers, processes or materials. Some simulators attempt to model the effects of PCB variances during design validation to help visualize their effects on margins. While simulation improves confidence in a design, it is not a substitute for actual empirical testing.

Margining and BER tests can expose the effects of these variances on serdes performance, but they require more time to execute during volume manufacturing than the typical structural and functional tests that are performed in the factory. Therefore, it may only be practical to perform these tests on production printed circuit assemblies (PCA) when performance is highly critical to the user. As an alternative to performing these tests on every PCA during volume manufacturing, it may be wise to run margin and BER tests on sample lots consisting of multiple production boards throughout the life cycle of the product, especially when vendors have changed, the design was re-spun or alterations were made in the assembly process. But while some PCB process variants can be caught by sampling at the batch level, other flaws and process variants may be missed entirely because they only affect a single board's performance or the performance of random boards as they pass through the manufacturing process.

Process Variances in PCB Manufacturing

An example transmission line with specific characteristics will be examined to illustrate the effects of PCB variance on the performance of a serdes circuit. The line in this example will be a Stripline with a .005-in. trace width on half-ounce copper and .005-in. spacing between traces. The trace will be embedded in FR-4 with a dielectric constant of 4.3. The line's surfaces are 5 mils from an upper ground plane and 8 mils from a lower ground plane. The transmission line

must support a 5 gigabits per second (Gbps) bus speed. The example trace pair is eight inches long. The intended impedance of the transmission line is 50 ohms.

Stripline Dimensions

The ratio of the conductor width to the distance from the power planes plays an important role in controlling impedance. The dielectric constant of the material that separates the trace from the power planes is also an important factor. These dimensions all work together to affect the inductance and capacitance of the trace and, consequently, its overall impedance.

Variation in etching time and the amount of etching material applied will affect the width of the trace. The typical tolerance on trace width is +/-10 per cent. For this example, the width (W) can range from .0045-in. to .0055-in.

The processes used for creating the core FR-4 and for pressing the pre-impregnated (pre-preg) layers of FR-4 are also inexact. For the purposes of this example, it is assumed that the core thickness is .005-in. (+/-.001-in.) and that the finished pre-preg thickness is .008-in. (+/- .002-in.).

The thickness of a trace is determined by the weight specification. Half-ounce copper foil is .000675-in. thick (T) and it is rarely specified with a tolerance. The thickness is relatively easy to control. For this example, thickness is considered constant. The dielectric constant is 4.3 with a tolerance of +/- .1, or a range of 4.2 to 4.4.

Impedance is derived from a formula. (See Appendix A, *Determining the Resistance and Impedance on a Transmission Line,* for two spreadsheets containing calculations for resistance and impedance.)

Using the example trace described above and assuming all specifications are exact, the impedance would be 47.77 ohms or close to the ideal, but the cumulative effects of worst case extremes can result in an impedance range of 63.39 ohms (thick dielectrics, narrow trace and low dielectric constant) to 36.28 ohms (thin dielectrics, wide trace and high dielectric constant).

Of course, the distribution of this impedance range between 36.28 ohms and 63.39 ohms is Gaussian (that is, it follows a bell curve), but an impedance range this wide is enough to cause significant variation in signal reflections which result in losses and distortion at the input of the receiving device. The reflection coefficient for the example Stripline, assuming source and load impedances of 50 ohms and considering no variance from the PCB specifications, is .002281, while the reflection coefficients for the two worst case extremes are -.09413 and .15889.

In other words, based on PCB variances that are within commonly accepted tolerances, as much as 15 percent of the energy in the signal may never enter the receiver. This is enough to have very noticeable effects on signaling margin on this trace.

Trace Surface Finish

This example assumes that the cross section of a Stripline trace is rectangular. In practice, it is not. Process differences between suppliers, or even between different batches of PCBs from one supplier, can cause significant variations in the shape and smoothness of a trace's cross sectional perimeter. (Figure 2)

Figure 2: This illustration of a trace on an inner layer of a PCB shows the roughness of the copper on the upper and lower surfaces of the trace.

Some of the process variations that can affect the shape of a trace are over-etch/under-etch (See Figure 1), substrate effects, imaging quality, oxide treatments and micro-etch oxide alternatives, and foil treatments. Assuming that the PCB manufacturer has assured that the nominal trace width is within tolerance, some of these effects can be minor. However, trace surface roughness is proving to be a significant factor in high-speed transmission lines and this variance may not be detected by common PCB tests.

Surface roughness has both good and bad effects. The metal foil's surface is intentionally made rough so that the metal will have a stronger bond to the dielectric materials during core layer production and during the pressing of core and pre-preg layers. Better bonds ensure against delamination of the layers, which can cause fatal (and possibly latent) failures on transmission lines. But increasing surface roughness also increases insertion loss.

The skin effect causes current density at higher frequencies to concentrate near the outer edge of a conductor. As frequency increases, the skin depth decreases. At 5GHz, the frequency used in this example, the skin depth is only .92 microns and even less for the harmonics. Surface roughness is measured in microns. Roughness typically measures from 1 micron rms (root-mean-square) to 8 microns rms. When surface roughness exceeds the skin depth, the effects of roughness on characteristic impedance and resistance (per unit length) is more pronounced. As current travels down the length of the trace on the outer shell of the metal, the rough outer surface affects the distance the current travels, which increases the resistance. The rough path of the current also forces many changes in the direction of current flow, which increases the inductance of the trace. This is analogous to driving a car over a mountain range vs. driving it on a flat and straight road. This phenomenon is accentuated at the higher harmonics of the signal. As a result, the shape of the signal will be affected.

If a PCB manufacturer changes the foil type or changes suppliers, or if the processes for ensuring good adhesion to pre-preg layers is altered, surface roughness can change from batch to batch. Due to the non-uniform nature of surface roughness, the effects are difficult to simulate and measure. Performing margining and BER on sample batches of multiple PCAs from different manufactured lots of PCAs is a good way to measure the effects of such changes.

Random Variance (Defects)

Some of the defects that can occur during the process of manufacturing a printed circuit board include the following:

- Incompletely plated vias
- Annular ring breakout
- Flaws introduced during the imaging process (pin holes, nicks, cuts)
- Plating thickness variances
- Delamination

These kinds of defects may or may not be detected by electrical tests or visual inspection, but they can affect the performance of transmission lines. In fact, some defects may go undetected by structural and functional tests after the PCA is assembled.

Another characteristic of random defects is that they may not be detected by testing a sample batch of PCBs. A margining and BER test of individual assemblies may be required to ensure proper performance.

Validation with Embedded Instruments

As explained above, BER and margin testing are frequently employed during design validation, but due to the complex instrumentation, setup and time required to run these tests, these techniques are often not repeated after a product is launched into volume production. It is not reasonable to introduce certain types of test equipment like oscilloscopes and vector network analyzers (VNAs) into the main production flow. These types of external hardware-based testers are high-cost items that require expert users and it would take far too long to test every high-speed net on a board during production. In addition, probing signals in the multi-Gb/s range is an art form in itself, often requiring a dedicated probing station and simulation to isolate the effects that fixtures and probes have on measurements.

Fortunately, the increased deployment of instrumentation embedded inside of chips (embedded instrumentation), as well as the emergence of protocol standards and tools for communicating

with these instruments are enabling margin and BER tests throughout a product's life cycle, including during volume manufacturing. The emergence of embedded instruments in chips provides a new approach for solving these problems.

The Emergence of Embedded Instrumentation

Many of today's chips already have instruments embedded in them by the device manufacturer. These embedded instruments can usually be accessed through a software solution to allow on-board testing without the need for external hardware testers. With a tool platform like ScanWorks® driving the embedded instruments inside chips, the only external hardware required is a small, low-cost interface pod. Rather than relying on external hardware-based measurements, simulation and user interpretation of specifications and results, embedded instruments can provide true, uncorrupted results observed at the receiver itself. Tests executed by embedded instrumentation use the same receiver that is employed in normal functional modes. There is no interpretation of results by the tester since the actual functional receiver is the test point.

An example of this is the instrumentation that Intel® is embedding into its processors and chipsets, including Core®, Atom® and Xeon® devices. Not only can this embedded instrumentation technology detect structural board faults on chip-to-chip interconnects, but it can also provide information about the performance and quality of the links.

For example, the overall test strategy for Intel® Xeon® designs focuses particularly on high-speed buses such as QuickPath Interconnect (QPI) and PCI Express (PCIe). With Intel's embedded instrumentation and a toolkit such as ScanWorks®, functional tests can be performed on these buses using pseudo-random bit sequence (PRBS) patterns as a foundation for pattern generation and checking (PG&C), BER testing and margining.

Basic PG&C tests can detect many structural faults, but high-speed serial nets like QPI and PCIe are designed to reject common mode noise and DC offsets. Some structural faults, such as shorts to ground or power, simply inject a DC offset which the receiver attempts to reject. In these cases many types of test technologies may show that the links are operating normally and they could even work functionally, but the performance and margin available on the link will be

degraded. The more advanced capabilities of Intel's embedded instrumentation technology are required to detect performance degradation due to structural faults or variances in device, materials or process changes.

Rather than attempting to measure low-level parameters such as insertion loss and impedance variations to determine the performance of the link, embedded instruments can determine BER and margin data such as eye height and width at the receiver inside the chip itself. (Figure 3) This provides data directly from the functional receiver without requiring modeling and simulation to de-embed probe and fixture effects. With this direct measurement, no human interpretation of passing vs. failing bits is needed.

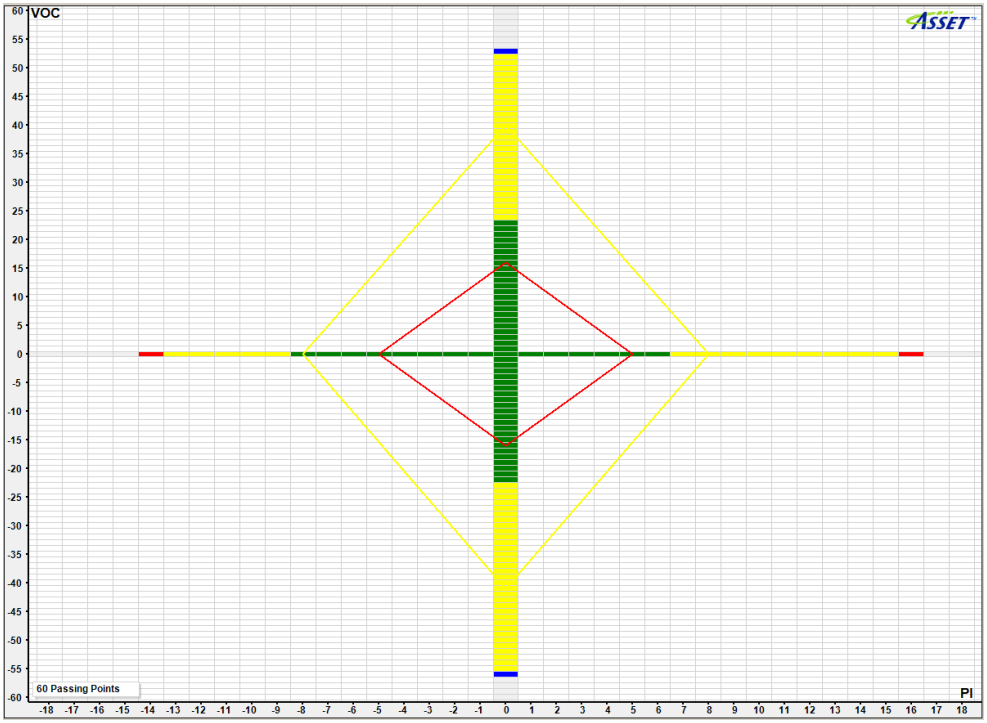


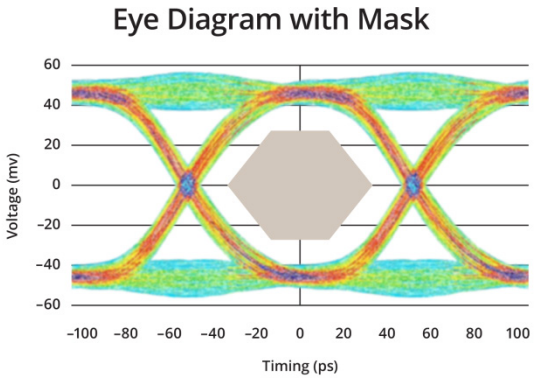
Figure 3: This composite view of a cross margin test shows where all lanes are passing (green), some lanes are failing (yellow) and all lanes have failed (red). Blue indicates some lanes were still passing at the maximum allowed range.

Overcoming Variances

Process variances encountered over the course of volume manufacturing can cause circuit boards to drift outside of their operating range. Also, systems deployed in the field can suffer from degraded performance or fail over time due to environmental factors or the effects of silicon aging. A proactive approach to signal integrity validation enabled by embedded instrumentation in the factory during volume production – as well as the entire life cycle of a PCB – is the new standard for the next generation of high-speed buses.

Learn More

If this information was helpful, you might find other white papers and e-books on our web site. Learn more about signal integrity. Register for our e-book, *Bandwidth tests reveal shrinking eye diagrams and signal integrity problems*, and learn why performance validation is so critical for today's complex and ultra-fast circuits.



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Appendix A

The following spreadsheets calculate the resistance and impedance on the example transmission line cited in this white paper. An online tool for determining transmission line impedance can be found at: http://www2.asset-intertech.com/l/7432/2013-02-01/j8ymw

DC and AC Resistance of the Example Transmission Line

Thickness (T)	0.000675	inches	17.145	um
		Smallest W	Mean	Largest W
Width (W)		0.0045	0.005	0.0055
Area	W * T	0.000003038	0.000003375	0.000003713
Perimeter	2T + 2W	0.01035	0.01135	0.01235
Trace Length		8	8	8
Trace Length		10	10	10
Rdc/inch =	6.5866E-07	/ Area		
Rac/inch = (	0.000000216	* SQRT(f)) / Perimeter		
Total R/in. =	$((R_{DC})^2 + (R_{AC}(f)^2))^{1/2}$			

		Smallest W	Mean	Largest W
	Rdc	0.21684	0.19516	0.17742
Harmonic				
5000000000	Rac (fund)	1.47570	1.34568	1.23672
15000000000	Rac (3rd)	2.55599	2.33079	2.14206
25000000000	Rac (5th)	3.29977	3.00904	2.76539

Harmonic		Skin depth inches	Skin depth microns	5 x SD inches	5 x SD microns
5000000000	Rac (fund)	0.00003625	0.92	0.00018125	4.60
15000000000	Rac (3rd)	0.00002093	0.53	0.00010465	2.65
25000000000	Rac (5th)	0.00001621	0.41	0.00008105	2.05

	Total R/inch			
5000000000	Rac (fund)	1.49155	1.35976	1.24938
15000000000	Rac (3rd)	2.56517	2.33895	2.14940
25000000000	Rac (5th)	3.30689	3.01536	2.77108

Attenuation at 8 inches = EXP(-((R*X)/(2*SQRT(L/C))))

	Smallest W	Mean	Largest W
Attenuation of fundamental	0.88895	0.89238	0.89510
Attenuation of 3rd harmonic	0.81672	0.82214	0.82643
Attenuation of 5th harmonic	0.77029	0.77686	0.78209

Attenuation at 10 inches = EXP(-((R*X)/(2*SQRT(L/C))))

	Smallest W	Mean	Largest W
Attenuation of fundamental	0.86317	0.86734	0.87065
Attenuation of 3rd harmonic	0.77642	0.78285	0.78796
Attenuation of 5th harmonic	0.72163	0.72934	0.73548

Impedance of the Example Transmission Line

per Asymmetric Stripline Impedance Calculator

Zo = 80/(√Er)*ln((1.9*(2H+T))/(0.8W+T))*(1-(H/(4*H1)))

Co = ((1.06*G55)/LN((1.9*(2*H+T))/(0.8*W+T)*(1-(H/(4*H1))))/1000000000000

Lo = (Co*POWER(Zo,2))

Where		
	Zo is	impedance
	Er is	dielectric constant
	H is	space between trace and upper plane
	H1 is	space between trace and lower plane
	W is	width of trace
	T is	thickness of trace

	Specification for the example		minimum	maximum
Zo	50	ohms		
Er	4.3	(no unit)	4.2	4.4
H	0.005	inches	0.003	0.007
H1	0.008	inches	0.006	0.01
W	0.005	inches	0.0045	0.0055
T	0.000675	inches	0.000675	0.000675

Varying only the trace width,	Smallest W	Mean	Largest W
Zo	50.68168	47.77012	45.09774
Co	3.46960E-12	3.68107E-12	3.89920E-12
Lo	8.91212E-09	8.40014E-09	7.93021E-09

Considering all tolerances for Er, H, H1, W			
Zo	60.39075	47.77012	36.28913
Co	2.87773E-12	3.68107E-12	5.81975E-12
Lo	1.04952E-08	8.40014E-09	7.66403E-09

reflection coefficent (r) = (Zl - Zs)/(Zl +Zs) where Z(load) is 50 ohms and Z(source) is Zo			
	-0.09413	0.02281	**0.15889**