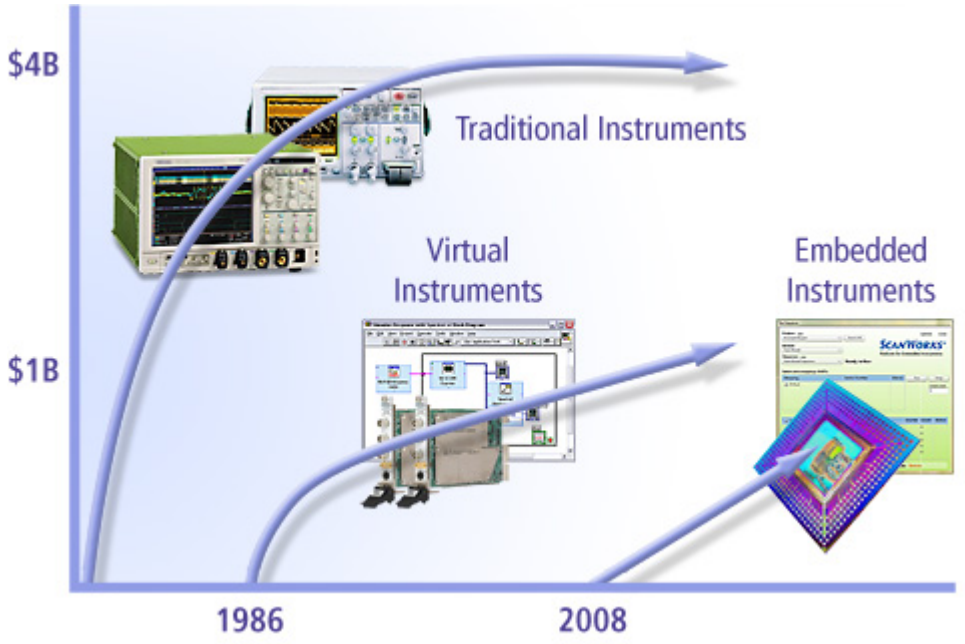
HIGH-SPEED BOARD SCAN TEST | PCI, QPI, …



ECONOMICS OF NON-INTRUSIVE BOARD TEST

BY ALAN SGUIGNA

High-Speed Board Scan Test | PCI, QPI, …

Economics of Non-intrusive Board Test

By Alan Sguigna – Vice President of Sales

Alan Sguigna has more than 20 years of experience in senior-level general management, marketing, engineering, sales, manufacturing, finance and customer service positions. Before joining ASSET, he worked in the telecom industry. He has had profit and loss responsibility for a $150 million division of Spirent Communications, a supplier of test products and services. Prior to his tenure with Spirent, Mr. Sguigna also served in business development positions with Nortel Networks, overseeing the growth of its voice over Internet protocol (VoIP) products.

High-Speed Board Scan Test | PCI, QPI, …

Economics of Non-intrusive Board Test

Table of Contents

Executive Summary

For the last 30 years or more, the electronics industry has mostly relied upon a hands-on approach to test and measurement. That is, older test technologies like in-circuit test (ICT), oscilloscopes, manufacturing defect analyzers (MDA), flying probe testers, logic analyzers and others have depended on physical contact to test printed circuit boards. Beginning more than 10 years ago and taking on even greater importance over the last two to three years, a hands-off approach to test – non-intrusive board test (NBT) – has become an increasingly critical facet of contemporary board test strategies. Recent developments in basic electronic technology as well as the evolving economics of electronic test have combined to make NBT and the test technologies that comprise it, such as boundary-scan test, processor-controlled test (PCT) and built-in self test (BIST), a necessity.

The trajectory of the electronics industry has always been toward faster, more sophisticated and more complex chips. In recent years, circuit board design practices have also become more complex. For example, chip-to-chip interconnects have shifted away from broad parallel buses to high-speed serial interconnects. Many circuit boards are now composed of multiple layers of fiberglass; burying many the boards interconnect traces deep within the substrate. These and other factors have contributed to the disappearance of the physical access that intrusive test technologies like ICT and oscilloscopes have relied upon.

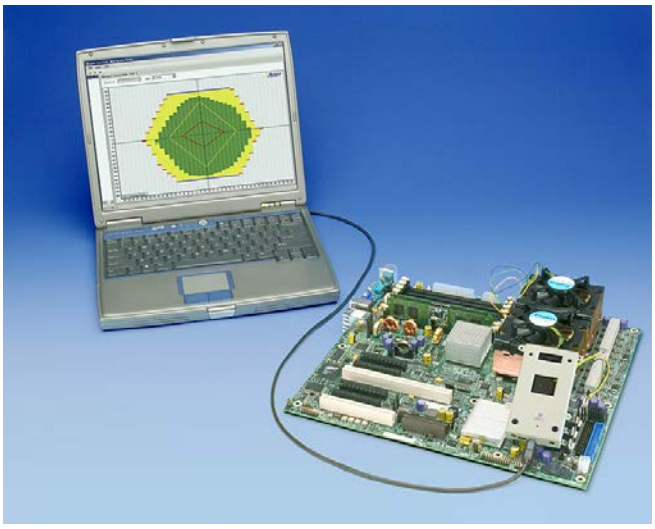
In recent years, the pendulum has swung toward NBT. Test strategies incorporating NBT techniques can achieve coverage as extensive as – or better than – the coverage that the older intrusive methods were once able to achieve. As a result, manufacturers of computers, communication systems, embedded systems, aerospace and defense products, medical systems and many other leading-edge applications are turning to NBT as they implement next-generation chips, circuit board architectures and systems.

At the same time, performing test with the old, intrusive test technologies has become prohibitively expensive. It becomes increasingly more difficult to justify old-generation test equipment like ICT systems when their ability to identify faults is diminishing and they come with a very high price tag and exorbitant operating expenses.

NBT is proving its worth to the industry. It can more effectively test today's most advanced circuit boards and, being largely software-based, it is significantly more cost-effective than previous generations of test technologies.

What is Non-intrusive Board Test?

Unlike the older generations of electronic test technologies, non-intrusive board test (NBT) does not involve placing a metal probe on a circuit board, test pad or chip pin to test the electrical continuity of the connection between the chip and the trace on the circuit board. Specifically, NBT is a software-driven technology, rather than hardware-intense, as the older intrusive test technologies have been. For NBT, a simple connector on the printed circuit board links the board to an NBT test station, which is typically a personal computer (PC) running test system software and other tools. In many cases, NBT test technologies make use of the JTAG port (that is, the IEEE 1149.1 Boundary Scan Standard's Test Access Port) to access the circuit board, but other interface technologies can serve in the same role. In addition, NBT involves embedded test intellectual property (IP) in chips and on circuit boards. With boundary scan, for example, chips that are compliant with the standard include a few test registers, and circuit boards are architected to enable boundary scan access and test.



Essentially, NBT technologies apply electrical test patterns that are internal to the circuit board. These tests exercise the board, the results are observed and any failures in the structural integrity of the board are noted. Extensive diagnostic capabilities pinpoint the locations of failures to facilitate rapid repair.

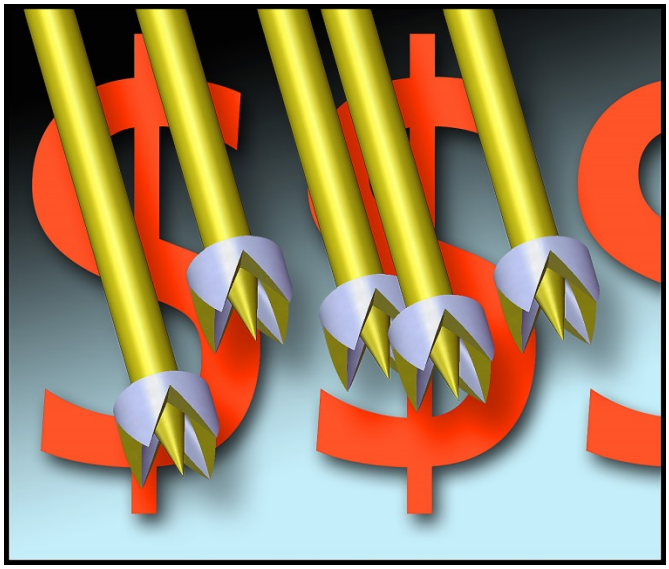
NBT has emerged as a matter of necessity. Many of the electronics industry's building blocks – the chips, how they are connected on circuit boards, the advanced design techniques that are

being applied to circuit boards and other facets of the industry – have moved beyond a reliance on physical contact to test the electrical continuity or structural integrity of circuit boards. This trend is being driven by developments on several fronts.

For example, not too long ago it was a standard design practice to insert test pads, small contact points on a circuit board's interconnect buses, on the surface of a board. These were used for physical access to the underlying buses for test purposes. In recent years, high-speed serial interconnects like PCI Express 2.0 or 3.0, Fibre Channel, 10-Gbps Ethernet, InfiniBand, Intel®'s QuickPath Interconnect (QPI) and others have become more and more commonplace. Quite simply, placing a metal probe on a test pad on these high-speed serial interconnects can introduce signal integrity anomalies and does not yield reliable test results. Test pads and probes introduce capacitance on the bus which renders any intrusive test measurement unreliable.

Probing the pins on semiconductor devices has also been problematic for quite some time. Device pins are either disappearing in favor of metal balls that are inaccessible because they are placed underneath the silicon die in ball grid array (BGA) packages or the pins have become so small that they cannot be accurately probed one at a time. In addition, a host of other technological advancements are moving test strategies away from the older intrusive test technologies. These include several industry standards of the IEEE. For example, IEEE 1149.7 defines a compact two-wire boundary scan interface and enhances the original standard with capabilities for testing multi-die chips, like system-in-package (SIP), system-on-a-chip (SOC) and others. Other boundary-scan-based standard, like IEEE P1687 for managing instruments that have been embedded into chips and IEEE 1149.6 for testing AC–coupled nets, are also gaining adoption in the industry. A related standard, IEEE 1500, defines a processor core wrapper test process. It is to chip test what boundary scan is to circuit board test.

Economic Benefits Drive Industry to NBT



Another causative factor in the move toward NBT is economics. The older intrusive test technologies like in-circuit test (ICT) typically involve large, expensive test systems, which require complex and expensive test fixture. The life-cycle cost of one ICT system on a manufacturing line can be more than a million dollars. And the ongoing cost of developing and fabricating bed-of-nail test fixtures is often prohibitive.

NBT can counteract the ever-escalating cost of intrusive test technologies. Because it is software driven, NBT is extremely flexible and very adaptable. In particular, NBT can be quite efficient when new product designs are transitioning from development to high-volume manufacturing. During this phase of a product's lifecycle, circuit board designs are still being qualified and numerous design changes are being made. For example, if ICT were the board test technology used on beta versions of a new board design, an ICT test fixture costing tens of thousands of dollars would be needed for each batch of prototype boards produced. Moreover, another version of the ICT test fixture would be needed whenever the qualification process discovered a flaw that triggered a design change. The cost of ICT test fixtures can escalate quickly. In contrast, NBT is not limited by test fixtures. A design change might trigger a software change or the recompilation of a circuit board's NBT tests, but expensive hardware re-spins of test fixtures are avoided entirely.

When compared to the older intrusive test methodologies, NBT technologies like boundary scan, PCT and BIST are more agile, software-driven and much more cost-effective. Whereas basic ICT systems often come with a starting price tag in excess of $250,000, a personal computer-based NBT station can be deployed in a manufacturing line for less than $25,000, a tenth of the cost of an ICT system. In addition, NBT does not require test fixtures which are expensive to

produce and maintain, especially when every design change triggers the production of a new fixture.

Non-intrusive Board Test Technologies

Several currently deployed test technologies fall under the NBT rubric, including boundary-scan test, processor-controlled test (PCT) and numerous built-in self test (BIST) technologies, such as Intel® IBIST (Interconnect Built-In Self Test).

Boundary-Scan Test

Boundary-scan test, based on the IEEE 1149.1 Boundary Scan Standard, was developed in the mid-1990s because fine-pitch pins on chips could not be probed or the pins were disappearing under the silicon die in ball grid array (BGA) packages. Boundary-scan tests are applied to a circuit board through a connector and the four-wire interface on boundary scan's Test Access Port (TAP). On chips, this interface is commonly referred to as the 'JTAG port', which comes from the informal name of the working group that began development of the standard, the Joint Test Action Group.

Since its development, the boundary scan standard has been adopted extensively by the industry and it is now deployed in chips, on circuit boards and in systems. Because of its widespread acceptance, the boundary-scan infrastructure has been appropriated by other applications and related standards. It is used to program logic and memory devices in-system, for example, and it provides the basis for the IEEE 1149.6 standard for testing high-speed AC-coupled interconnects. As mentioned previously, the new IEEE 1149.7 standard enhances the original 1149.1 standard and offers a more compact two-wire interface while maintaining compatibility with the original 1149.1 boundary scan standard. Several other related standards also make use of the embedded boundary-scan infrastructure in chips and on circuit boards.

Processor-Controlled Test

Processor-controlled test (PCT) makes use of the boundary-scan infrastructure to access a circuit board's processor. Control of the processor is temporarily given over to the PCT system so that test algorithms can be applied at processor speeds through the input/output pins that connect devices on the circuit board to the processor. In this way, PCT propagates test patterns through the processor onto the structural interconnects of the circuit board. PCT can exercise the functionality of the circuit board as well as detect and diagnose structural faults.

Built-in Self Test

With regards to NBT, built-in self test (BIST) refers to test mechanisms or instruments that are embedded into chips and which can be applied in non-intrusive structural board test applications. A particular example of this is Intel®'s Interconnect Built-in Self Test (IBIST) technology which is being embedded by Intel and other semiconductor and IP providers into next-generation chips and chip sets. The embedded Intel IBIST functionality can be applied in a number of ways, including structural tests in NBT applications. It can also be used in design validation applications to validate the performance of high-speed serial buses on circuit boards.

Non-intrusive Board Test on the ScanWorks® Platform for Embedded Instruments

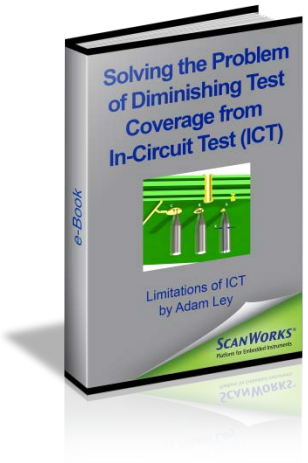
The ScanWorks® platform for embedded instrumentation is particularly well suited to NBT applications for several critical reasons.

First, the ScanWorks platform provides the access, automation and analysis functionality needed by NBT. Non-intrusive access is derived from ScanWorks' track record as the leading tool for boundary-scan testing, although other interface technologies could provide the basis for accessing NBT technologies in the future. Beyond access, ScanWorks automates the operations of multiple non-intrusive test technologies such as boundary scan, processor-controlled test and Intel® IBIST, while melding multiple technologies into a cohesive test strategy. Once NBT test technologies are operational, test results must be analyzed. ScanWorks' diagnostic and debugging tools make coherent sense of the test data produced by NBT.

The second factor that makes ScanWorks a leading NBT solution is the synergy that develops from integrating the industry's leading boundary-scan test, PCT and Intel® IBIST tools in the same platform environment. Taken individually, each of ScanWorks' test technologies provides its own significant level of test coverage. Taken together on the ScanWorks platform NBT provides comprehensive test coverage and diagnostics as good as – or better than – the older intrusive test technologies like ICT, MDA, flying probe and others.

Learn More

In-circuit test seemed ideal for simplifying test generation and execution when it was first introduced. Fortunately, new test access standard and software-driven tools offer alternative to probe-based testing. To learn more, get our e-Book. "*Solving the Problem of Diminishing Test Coverage from In-Circuit Test (ICT)*".



Register Today!