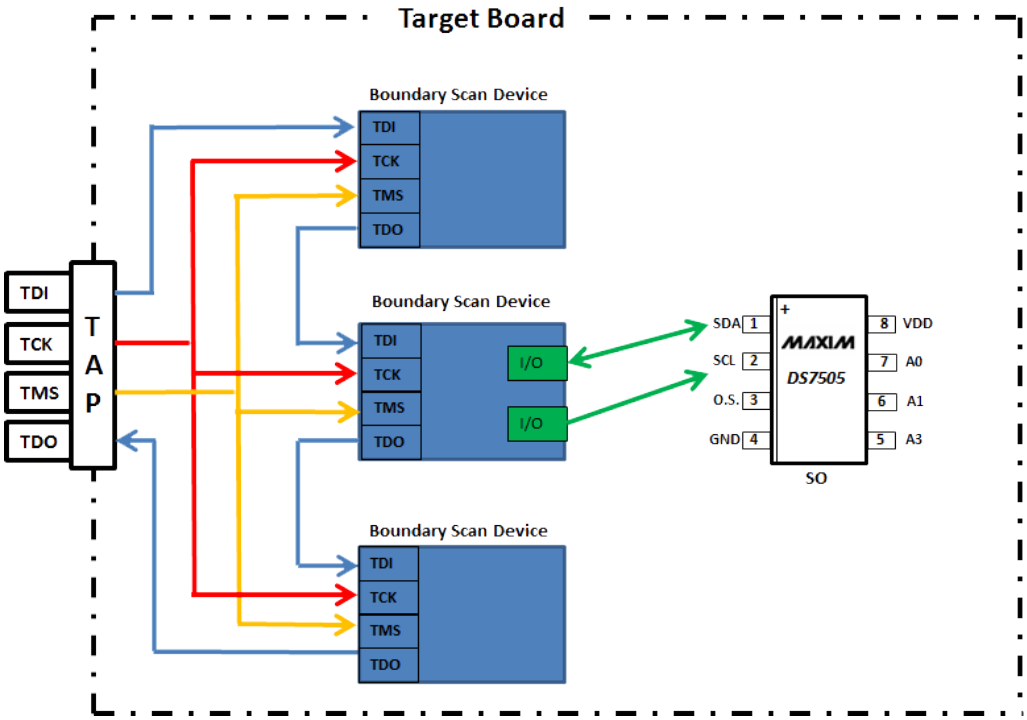
FUNCTIONAL TEST ON I2C AND SPI SYSTEM MONITORS WITH JTAG



E-BOOK

BY KENT ZETTERBERG

Functional Test on I2C & SPI System Monitors with JTAG

By Kent Zetterberg – Product Manager

Kent Zetterberg started his career in the automation industry, working with systems from ABB, Siemens and others. Following graduation from the University of Gävle with a Bachelor's of Science Degree in Computer Engineering, he worked 15 years in the telecom industry where he held various positions involving hardware test and debug. He joined Ericsson AB in Sweden in 1997 where he developed functional test programs for processor boards, and designed interface boards and test fixtures. At Ericsson he became an expert in boundary scan and eventually led the boundary scan team. With ASSET Kent has held several positions in support, serving as a customer trainer and European support team leader. Currently he is the technical product manager for ScanWorks boundary-scan test products.

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Executive Summary

Many contemporary electronic systems feature a wide range of system monitoring devices that keep track of certain conditions or operating parameters while the system is functioning. Should the monitor detect that the parameter has fallen outside of a predefined range; the monitor will take some sort of action, like alerting the on-board processor when the ambient temperature exceeds a certain upper limit. By and large, system monitors communicate over standardized communication interfaces like the SPI (Serial Peripheral Interface) or the I2C (Inter-Integrated Circuit) buses. Validating the functionality of these system monitors during prototype board bring-up is usually difficult and time consuming. Often, functional tests are not available during prototype board bring-up or functional tests can't be run on the prototypes because they won't boot yet. The stakes are large because any delays during board bring-up can jeopardize a new product introduction.

An effective alternative to the approach of relying on traditional functional test to validate monitor devices is to employ boundary scan/JTAG, which is usually a structural test methodology, to perform pseudo-functional test and program monitors with their operating firmware. This eBook describes how the on-chip and on-board boundary scan infrastructure can be applied to test and program system monitor devices even when these devices do not have boundary scan capabilities themselves.

Prototype Board Bring-Up

Testing and programming system monitors (Table 1) and other types of devices that interface to the I2C or SPI buses can jeopardize new product introductions because the traditional methods that have been deployed in the industry in the past rely heavily on functional test methods, which assume functioning prototypes. During prototype bring-up, operating firmware and software is often not available yet and, even if it is, it is still laborious and time consuming for engineers to develop the required functional test processes, which may prove to be inadequate should a defect be encountered on a circuit board. Functional tests are notoriously poor at pinpointing structural faults like shorts and opens. If a prototype is suspected of having a fault because it has failed a functional test, the engineers are faced with another lengthy process of trying to diagnose and isolate the problem through functional tests. In the end, precise diagnostics may be impossible.

Table 1: Example of system monitors and other types of SPI/I2C devices

Temperature monitors
Voltage and current monitors
Power management devices
Fan-speed control
Clock management devices
Managing analog-to-digital (AD) converters
Managing digital-to-analog (DA) converters
Read real-time clocks
Configuring audio codecs
Controlling communication devices (UART, USB, Ethernet, CAN, etc.)
Communicating with a system display
Programming of EEPROMs
Reading configuration data from SPD EEPROMs on SDRAM, DDR SDRAM, DDR2 SDRAM memory sticks or memory modules such as DIMM and other stacked PC boards
Communicating with application specific devices

Boundary-scan test methods (IEEE 1149.1/6 JTAG) supported by a capable boundary-scan toolset can address these difficulties by performing both structural and functional tests in one and the same test step. Boundary scan is able to perform structural and functional tests at the same time by emulating the bus functions of I2C, SPI and other communications interfaces.

Then, when structural faults are found, boundary scan is able to quickly isolate the defect down to a particular pin on a device. Moreover, boundary scan processes and tests can be applied to a circuit before any firmware or operating software is available. In addition, while boundary-scan based structural and functional tests are being run on these devices, they also can be programmed with their operating code. The opportunity to save time is particularly critical during prototype board bring-up before a board design has been released for volume manufacturing, because delays in the design schedule at this point can threaten the profitability of a new product if it is delivered late to the marketplace when its window of opportunity has begun to close. In addition, these same boundary-scan methods and the specific tests generated during prototype bring-up can be deployed again during production, saving additional time in test development and reducing test costs through re-use.

Volume Production

In a production environment, functional test is usually the most time consuming and expensive step. Even if the SPI or I2C buses are linked an external connector and test engineers can use, for example, USB-based protocol analyzers to access the buses as well as the devices on them, adding such USB pods or similar devices to test fixtures is expensive both from the standpoint of the added expense of the pods themselves and from the standpoint of the extra design and maintenance costs associated with modifying the fixtures. It would be more cost-effective to re-use a boundary-scan controller to perform these tasks, especially if boundary-scan test has already been deployed in this particular manufacturing environment. In the past, some of these monitoring devices were typically programmed with their operating firmware during the functional test step in production. Functional test can be very time consuming, so adding device programming to this step only lengthens the its duration. In addition, programming a monitor so it can be included in a functional test suite is problematic because at that point the device has not been test yet. Structural defects or other faults could be present and these could impede the functionality of the device during functional test. Even if the test engineer is dealing a particular monitoring device that has been designed into other circuits previously and which he has experience with, it can behave differently in a new design with a different architecture and operating environment.

In addition, using boundary-scan to program these devices is much easier than functional test because some boundary-scan tools support libraries of ready-to-use device model which can be quickly incorporated into programming algorithms.

Deploying boundary scan on a production line can reduce costs throughout the assembly process. For example, if in-circuit testers (ICT) are also being used, a boundary-scan station can perform some of the structural tests that the ICT testers were doing. This will reduce the number of ICT test pads needed on the circuit board being tested since boundary-scan does not access the unit under test (UUT) via test pads. This reduces the cost of the board. And, since ICT is simplified by shifting some of the structural test to boundary scan, the complexity of ICT fixtures can be reduced as well, decreasing the cost of designing, fabricating and maintaining the fixtures.

How is it done?

The easiest and most effective way to test and program monitors with boundary scan is to deploy boundary-scan tool that employs a device model approach where the functions, registers, and pin-maps of the I2C or SPI devices are described in a simple text-based format. It's also very helpful when the I2C or SPI device's native read, write, start, stop, acknowledge and other functions are available in the model files used by the boundary-scan tool. The most sophisticated boundary scan tools have verified the device models contained in their libraries so that the models can be easily re-used in other boundary-scan test applications without modifications.

Some boundary-scan test tools feature an automatic test pattern generation (ATPG) engine which is able to re-target test patterns through the boundary-scan pins and registers on an adjoining device and deliver these patterns to I2C or SPI devices whose functions and registers then become available to the boundary-scan tool.

The use case described below describes how boundary scan is able to read out over an I2C bus the temperature sensed by a temperature monitor, the Maxim DS7505. (The principles described in this example apply to SPI devices as well.) Figure 1 is a generic block diagram of the board populated by four devices, three boundary scan devices in a boundary-scan chain and the Maxim temperature sensor which is connected to one of the boundary-scan devices.

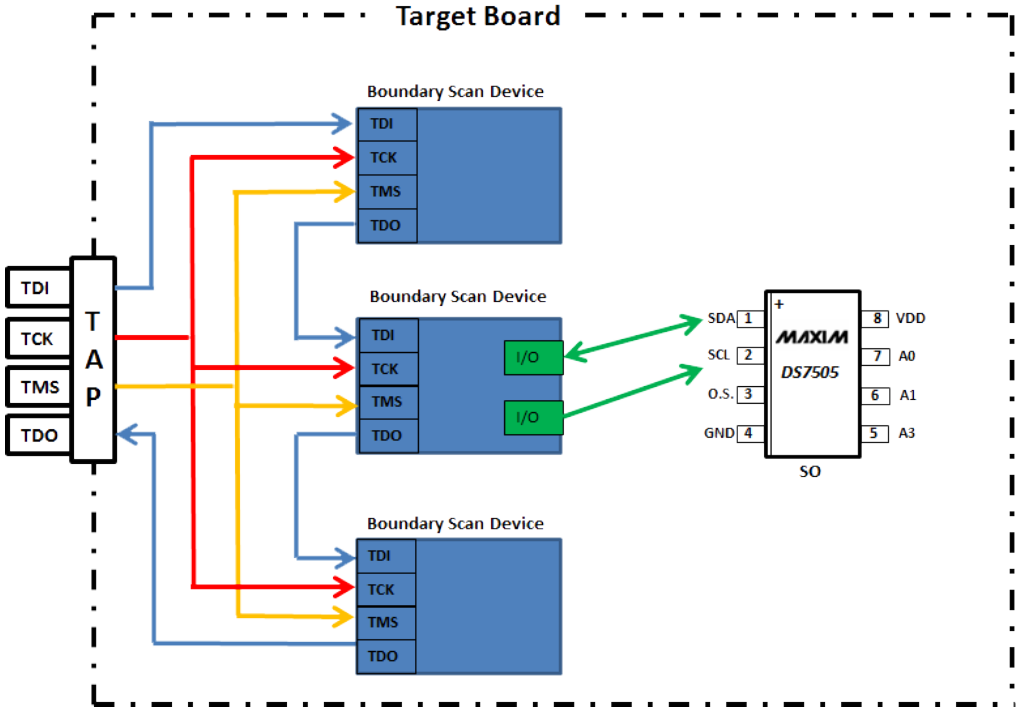


Figure 1: Board-level block diagram with a system monitor connected to a boundary-scan device.

To access the I2C device the boundary-scan tool must be provided certain information, including:

- The structure and composition of the boundary-scan chain
  - The order of the boundary-scan devices on the chain can be extracted from the board's netlist or this can manually defined.
  - The boundary-scan architecture of each device on the chain will be described in the devices' BSDL (Boundary Scan Description Language) files. These BSDL files are provided by the supplier of each chip. Often BSDL files are available on a chip vendor's web site.
- How the I2C device is connected to the boundary scan device

  - Again, the board's netlist provides information of how the I2C device is connected to the boundary-scan device. The netlist can be imported from a computer-aided design (CAD) tool to the boundary scan tool.
- What is the functionality of the I2C device (and perhaps other surrounding non-boundary scan devices)
  - Information on the I2C device is provided in a device specific model. This model will contain information on the device registers which will be accessed to test the functionality of the device.

The following is an example of pseudo code which will address the I2C device in this example.

```
Proc I2C_ReadTemp (DeviceAddress)
{
    I2C_Start
    for i=0 to 7
    {
        I2C_WriteBit (DeviceAddress[i])
        i++
    }
}
```

The device model should also contain all the primitive procedures for writing/reading data over the I2C bus. The following is typical pseudo code for writing a bit over I2C:

```
Proc I2C_ReadBit (Bit)
{
    Set SCL = 0
    Set SDA = Bit
    DRScan
    Set SCL = 1
    DRScan
}
```

Data read from the device is evaluated by the model. In this case, the upper limit for temperature (50 degrees) is specified in the model. This limit determines whether the device PASSes or FAILs the boundary-scan test. Less than 50 degrees is a PASS, over 50 degrees is a FAIL.

The following is an example of the device model's pseudo code for processing the data gathered by the Maxim temperature sensor.

```
If Temerature >= 50 then
{
    Print "FAIL"
    Print "Device is too hot"
```

```
        Set FailFlag 1
}
```

NOTE: In some designs the I2C or SPI devices will not be connect directly to an adjacent boundary-scan device. Often, series resistors, buffers or other non-boundary-scan devices will intercede between the monitor and a boundary scan device. When this is the case, information of the functionality of these so-called 'cluster' or non-boundary-scan devices might be required by the boundary-scan tool. This type of info is often contained in cluster models that may be provided by the boundary-scan tool provider and stored in a cluster library.

Summary

The illustration below (Figure 2) summarizes the data and the connections needed to perform functional testing on system monitors with boundary scan. The following are required: a capable boundary-scan test tool that conform fully to the standard and is supported by model libraries, BSDL files of the pertinent devices in the design, boundary-scan chain descriptions, netlists of the design, bill of material files, and CAD files. The last remaining prerequisite is a model of the targeted system monitor or I2C/SPI device. When this is obtained, the boundary-scan tool should be able to perform structural and functional tests the design, and program the I2C/SPI device.

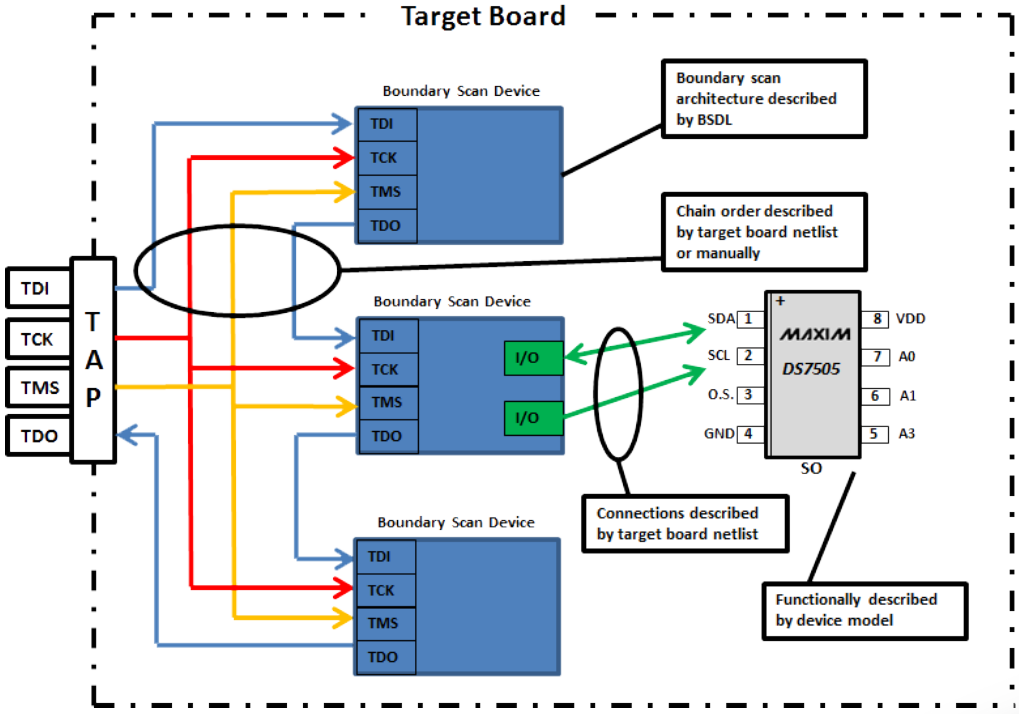
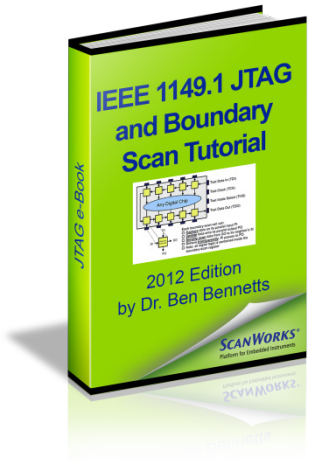


Figure 2: Block diagram showing connections needed to perform functional tests with JTAG.

Learn More

This e-book will tell you about the standard and how it can be put to work in the design, verification and manufacturing process. It also provides information of JTAG's relationship with other test techniques such as In-Circuit Testing (ICT), functional test, CPU emulation and others. To learn more, get our e-Book. "*IEEE 1149.1 JTAG and Boundary Scan Tutorial*".



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