ASSET INTERTECH

Whitepaper:

FPGA-Controlled Test (FCT): What is it and why is it needed?

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Executive Summary

Functionally, the role that FPGAs (field programmable gate arrays) have played in computer and communications systems has grown in parallel with the number of gates and the capabilities of these devices. A recent study by the Linley Group found that the deployment of FPGAs grew 51 percent in 2010, a testament to the rapidly increasing pervasiveness of these devices. Typically, FPGAs have been deployed by system designers for downstream, end-user functionality, such as logic engines, peripheral I/O management, communications coordination, graphics and multimedia processing, as well as other types of functionality. Now though, these versatile and flexible devices are emerging as a likely platform for next-generation embedded board test and measurement capabilities which can be employed upstream during design, development and manufacturing, and/or in ancillary downstream applications in the field following product launch, such as ongoing continuing engineering, remote diagnostics, troubleshooting and others.

This trend toward FPGA-controlled test (FCT) is a part of the larger shift toward embedded instrumentation as a more effective methodology for validating, testing and debugging circuit boards. Much of today's leading-edge electronics technology has simply progressed beyond the reach of legacy, intrusive test technologies such as oscilloscopes and in-circuit test (ICT) systems. Because these legacy methodologies are based on making contact with chips on boards and circuit boards themselves, they are hobbled by the physical nature of probing. The next wave

of validation and test technologies – which includes FCT – will be dominated by internal, non-intrusive software-driven embedded instrumentation methodologies.

FPGA-Controlled Test: Board-Tester-in-a-Chip

The precedent for embedding test and measurement instrumentation into semiconductors is well established. Chip suppliers have been doing it for years to characterize, validate and test their devices. Recently, the usefulness of these embedded instruments has been extended to circuit board validation, test and debug. Now, the next logical step is to embed the multiple instruments that would make up a board tester into an FPGA and thereby extend the test coverage capabilities of software-driven non-intrusive board test (NBT) and validation even further.

Such a board tester might be inserted into an FPGA for temporary or permanent purposes. For example, during circuit board development, first prototypes often are delivered before the firmware for an FPGA or the operating system has been completed. At this point, the structural, functional and performance capabilities of the prototype hardware must be tested to validate the design in preparation for software integration. Previously, functionally validating the hardware was severely limited without the board's firmware or OS in place. As a result, development schedules might be delayed while software was being completed. Now, FCT offers an alternative. With FCT, testers made up of multiple instruments can be inserted into an FPGA on the prototypes and subsequently removed when they have helped to validate, test and debug the design. In addition, there could be a need for this FCT tester later in the lifecycle of the circuit board. If so, then some or all of the embedded instruments might remain in the FPGA to perform manufacturing test, ongoing fault analysis, remote diagnostics or troubleshooting by field service.

A Faltering Legacy

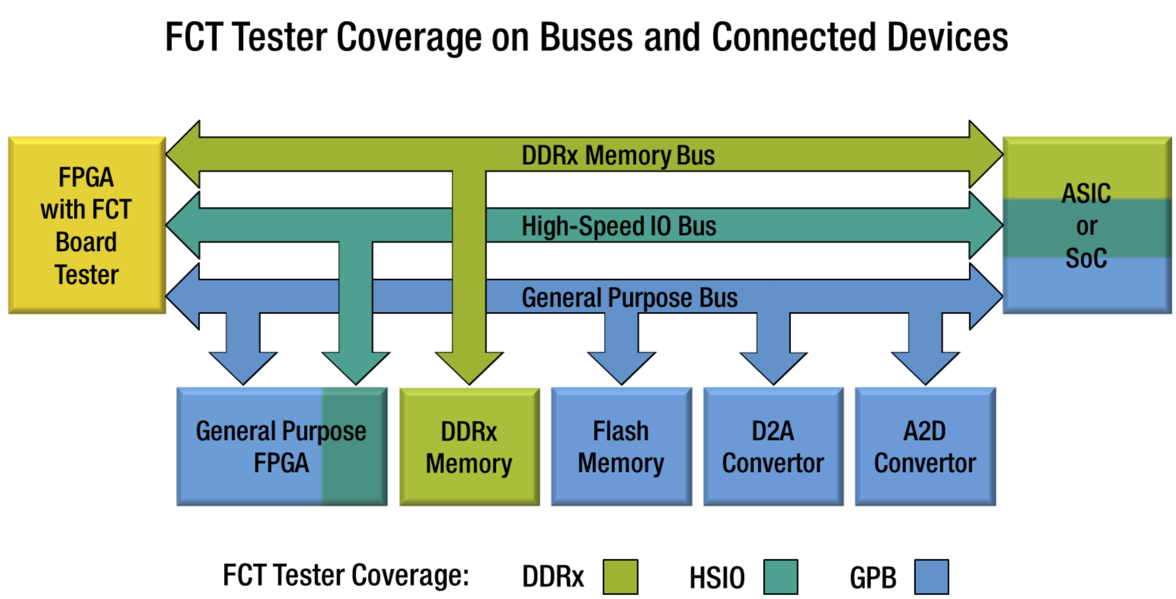
External test and measurement instrumentation, which depends on physical probes to test circuit boards, has performed its tasks admirably, but as complexity and operational speeds have escalated geometrically – while the size of chips and systems has shrunk dramatically – the effectiveness and capabilities of external instruments have eroded accordingly. As a result, providers of traditional external and modular instruments are investing in enhanced software for their equipment. They claim this increases their instruments' visibility into circuit boards, enhancing their effective test coverage. Unfortunately, no amount of extrapolation through higher order mathematics can provide the accuracy and authenticity of the empirical data that is observed and compiled by internal, non-intrusive, software-driven embedded instrumentation. FCT is another manifestation of this trend toward internal embedded instrumentation. For designers who are validating and bringing up boards, for manufacturing test engineers who are testing boards in high-volume production, and for field service or continuing engineering organizations, FCT is an effective way to take an inside look at what's happening on boards and in systems.

The coverage FCT delivers

The board coverage delivered by FCT is significant, but it will depend upon the goals and objectives established by the engineers responsible for test, validation or debug. Several methodologies for quantifying board test coverage have been suggested by industry organizations. For example, iNEMI (International Electronics Manufacturing Initiative) has codified a method called PCOLA/SOQ/FAM. The letters in the name stand for the following metrics that are used to quantify test coverage: Presence (is the device present on the board?), Correctness (is this the correct device?) Orientation (is it oriented properly?), Live (is it electrically functional?) Alignment (is the device aligned correctly?) / Shorts (are there any shorts?) Opens (are there any opens?), Quality (what is the structural quality?) / Feature (can a feature be detected?), At-speed (can at-speed tests be applied?) Measurement (can performance be measured and confirmed?).

Theoretically, the embedded instruments which comprise an FCT board tester will be able to validate, test and debug the devices that are connected to the FPGA. Instruments and signals are inserted and connected to the signals between the FPGA and other devices on the board. (See Figure 1 below.) This is the most straightforward approach to the coverage potential delivered by FCT, but additional coverage could be obtained in certain cases by developing routines where the FCT tester could apply tests beyond the devices and the interconnects that are linked directly to the FPGA.

Figure 1: Potential FCT Coverage



Many different types of instruments could compose an FCT board-tester-in-a-chip. Table 1 contains a partial list.

Table 1 : Some FCT Instruments

Some of the instruments suitable for FPGA-controlled test (FCT)
- Digital pattern generator -Digital capture buffer - SerDes BERT (bit error rate test) - SPI/I2C Master interface - Fast Flash memory programmer

How FCT Works

A key characteristic of FCT is its adaptability
The instruments and testers inserted in one FPGA may never be replicated exactly the same in another FPGA on a different circuit board. Each FCT board-tester-in-a-chip will likely be different from every other since the configuration of an FCT tester will be dictated by the circuit board design that is being tested and the test objectives of the engineers testing the board. As a result, each FCT tester must be easy to assemble, configure and insert into an FPGA. Fortunately, several industry standards can be applied to FCT.

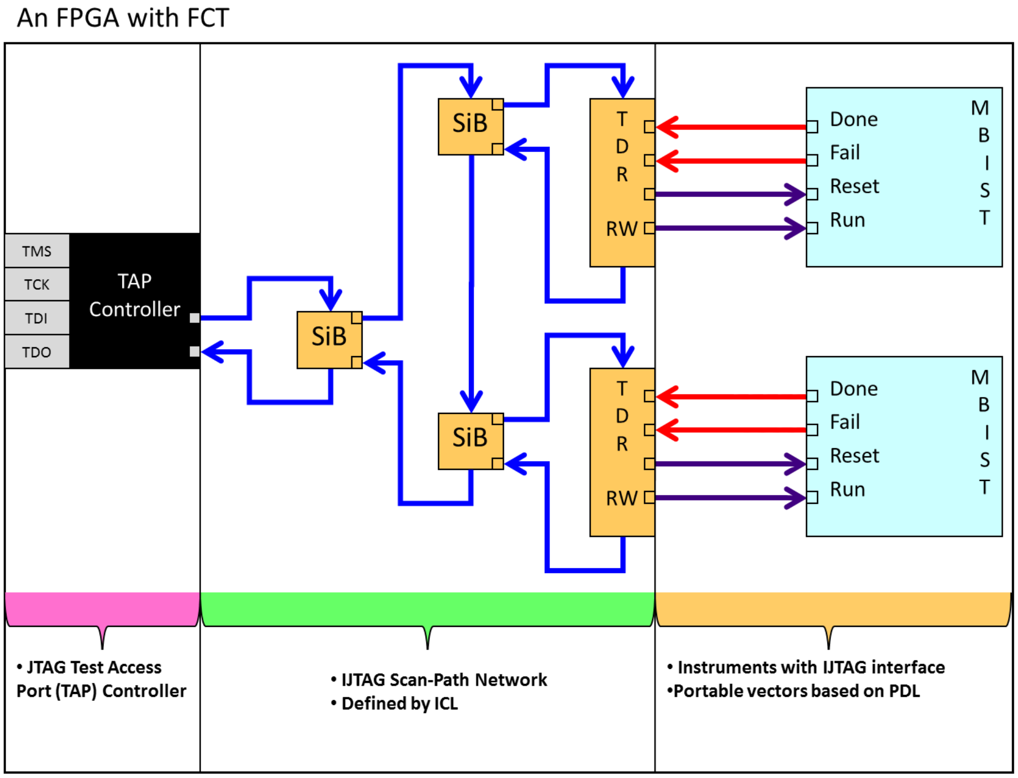
- ***IEEE 1149.1 Boundary-Scan (JTAG)***

Through its Test Access Port (TAP), the boundary scan standard provides an access method into an FPGA and an infrastructure for test-related communications throughout a circuit board.

- ***IEEE P1687 Internal JTAG (IJTAG)***

In addition to defining a standard interface for embedded instruments to ensure their portability, the IJTAG standard will establish an on-chip architecture for the instruments which make up a tester. When the standard is approved in early 2012, IJTAG will establish two languages. One (Instrument Connectivity Language: ICL) will be used to describe the architecture connecting the various on-chip instruments in an FCT board tester and the second (Procedural Description Language: PDL) will control and manage the operations of embedded instruments. The figure below shows an example of a basic IJTAG infrastructure on an FPGA. To simplify the illustration only two memory built-in self test (MBIST) instruments are shown, but many other types of instruments could be deployed at the same time and in the same FPGA.

Figure 2: A simplified IJTAG architecture on an FPGA



The IJTAG Standard as Operating System

Once inserted into an FPGA, the instruments must be managed, controlled, scheduled and coordinated to meet the objectives of the validation, test or debug engineer. This role, which amounts to an operating system for the embedded FCT board tester, is enabled by the IEEE P1687 IJTAG standard.

Beyond defining a standard interface for embedded instruments, the IJTAG standard also specifies an on-chip architecture for them. This is accomplished by the two languages that are a part of the standard. ICL describes the scan paths that connect the instruments and provides access to the outside world. In addition, an ICL description of an on-chip architecture can specify IJTAG Segment Insertion Bits (SIB) which can alter and control the scan paths so that the application of test vectors can be optimized. That is, SIBs can be used to turn off certain segments of the scan paths can when they are not needed and turned back on again when they are.

The IJTAG standard's second language, PDL, represents the test vectors or operational procedures that are applied by the embedded instruments.

One of the key elements in the IJTAG standard which enables the flexibility and re-configurability in the on-chip architecture is the Segment Insertion Bit (SIB). (See Figure 2.) SIBs allow on-demand access to instrument interface registers. Instruments are engaged in a test process when an instrument's SIB is selected. This includes the instrument in an active scan chain which can then be used to communicate with the embedded instruments on the chain. Then test vectors can be launched from the FPGA instruments onto the board to test peripheral chips and routes and to gather results data.

An Industry First: ASSET's ScanWorks FCT

The ASSET ScanWorks platform for embedded instruments was the first environment to support the IJTAG standard. Enabled by its IJTAG tools and its heritage as a leader in boundary-scan (JTAG) test, ScanWorks is able to function as an automated environment for FCT. Instrumentsare selected from a ScanWorks library and matched with a description of a supported FPGA device from another ScanWorks library. After the user sets the parameters on the instruments selected, ScanWorks automatically generates all of the on-chip constructs for the FCT board-tester-in-a-chip, synthesizes the code required by the FPGA and creates the software image of the tester for loading into the FPGA. Once inserted, ScanWorks provides a drag-and-drop user interface to operate and manage the tester.

For more information on ASSET's ScanWorks FCT technology, please visit www.asset-intertech.com.

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