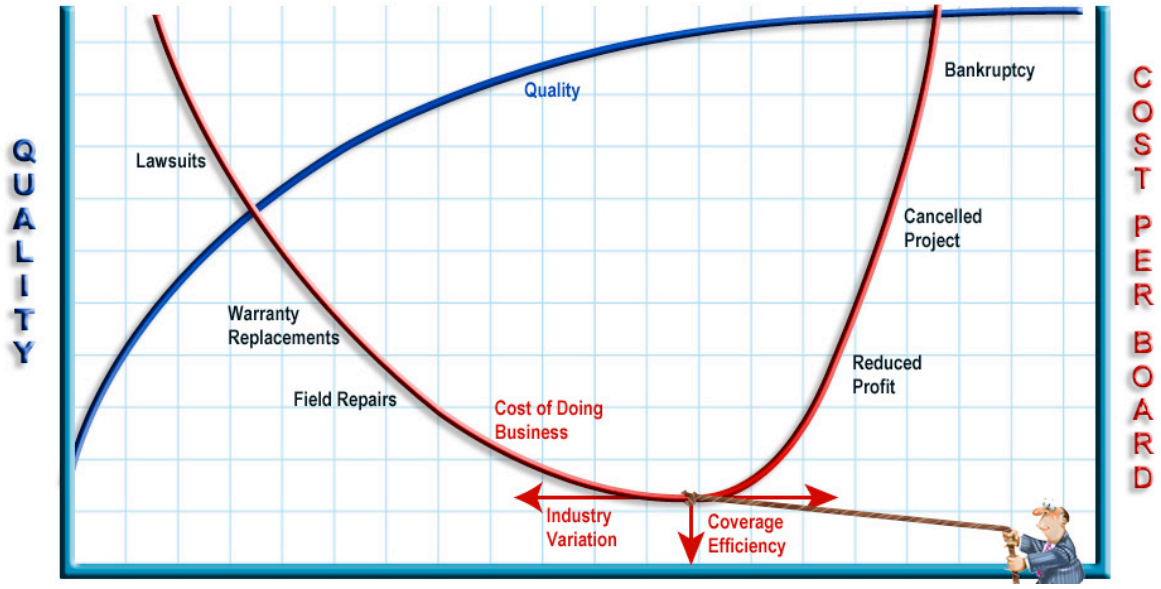
DEFECT COVERAGE FOR NON-INTRUSIVE BOARD TESTS



BY ADAM LEY

Defect Coverage for NBT

By Adam Ley, Chief Technologist, Non-intrusive Board Test

Adam serves customers by ensuring that ASSET's non-intrusive board test (NBT) methodologies comprise a best-in-class solution to meet the evolving need for improved coverage of board test in the face of ongoing erosion of physical access. Pursuant to ASSET's strong support for standards, Adam is an active participant in IEEE 1149.1, having previously served terms as working group vice chair and as standard technical editor (for the 2001 revision), as well as in nearly all related standards, to include: 1149.4, 1149.5, 1149.6, 1149.7, 1500, 1532, 1581, P1149.1.1, P1149.8.1, iNEMI boundary-scan adoption, PICMG MicroTCA, and SJTAG (system JTAG). Adam's experience prior to ASSET spanned over a decade at Texas Instruments, Sherman TX, where he had roles in application support for TI's boundary-scan logic products and for test and characterization of new logic families. Adam earned the BSEE degree from Oklahoma State University, Stillwater OK, in 1986.

Defect Coverage for NBT

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Overview

Non-intrusive board test (NBT)[i] is an emerging test methodology that integrates several complementary embedded-instrumentation-based test technologies to restore test coverage lost due to diminishing physical (probe) access to printed circuit boards (PCBs). The non-intrusive test, embedded instrumentation-based technologies that make up NBT include boundary-scan test, processor-controlled test, and built-in self test. In fact, these technologies form a perfect complement. They are all non-intrusive, typically requiring access only to the common board-level debug/test access port, but each one brings its own distinct elements of defect coverage to the NBT strategy. Boundary-scan test provides a core capability of test for PCB structure (e.g. shorts & opens); processor-controlled test adds elements of test for product function (e.g. test execution at full processor speed); and built-in self test delivers aspects of test for system performance (e.g. on-margin/measurement).

Considering that a framework to assess the overall test coverage in multiple dimensions is desired in order to weigh the full impact of the NBT test strategy, this whitepaper reviews some of the frameworks that have been proposed for measuring test coverage, such as Agilent's PCOLA/SOQ and iNEMI's PCOLA/SOQ/FAM. Since NBT can provide elements of structural test, such as boundary-scan test, as well as functional test (processor-controlled test) and performance test (built-in self test) to discover at-speed faults and/or insufficient operational margins, the defect coverage provided by NBT maps well against the criteria of these coverage frameworks.

But providing just extensive test coverage is not enough; the coverage benefit must be attained cost-effectively. Being software-driven, and so avoiding the expense and complexity of hardware systems that dominate the existing intrusive board test technologies, NBT delivers optimized cost-of-coverage as a critical advantage. As a result, NBT is emerging as a cost-effective alternative for new deployments or as a cost-reducing complement where intrusive methods are still used.

The Drive to Non-intrusive Board Test (NBT)

For the last 30 years or more, the electronics industry has mostly relied upon a hands-on approach to test and measurement. The older board test technologies and associated external instrumentation that typify this approach include in-circuit test (ICT), manufacturing defect analysis (MDA), flying probe, oscilloscopes, logic analyzers and others. These methods, while diverse, are all intrinsically dependent on physical (probe) contact to test PCBs; as such, they are classified as intrusive board test (IBT). Beginning more than 10 years ago and taking on even greater importance over the last two to three years, a hands-off approach to test – non-intrusive board test (NBT) – has become an increasingly essential facet of contemporary board test strategies. Recent developments in basic electronic technology and the evolving economics of electronic test have combined to make NBT and the embedded instrumentation test technologies that comprise it, such as boundary-scan test, processor-controlled test (PCT) and built-in self test (BIST), a necessity.

Where We've Been
(external instrumentation≡intrusive board test)

The access needed by external instrumentation to physically probe PCBs has been diminishing significantly for quite some time now; faster and more complex chips with high-speed serial interconnects on dense boards with blind and buried vias combine to make probing difficult, costly and even prohibitive. By their nature, board test technologies such as ICT, MDA, flying probe, and others are hardware intense. They rely on physical probes, expensive bed-of-nail fixtures and other hardware features; and the necessary points of physical contact are typically not related to the product mission or commissioning, which is to say that they are intrusive and in many cases pervasive.

Where We're Heading
(embedded instrumentation≡non-intrusive board test)

By contrast, non-intrusive board test (NBT), as an application of embedded instrumentation, is a software-driven methodology. As such, it allows the integration of complementary test technologies like boundary-scan test, processor-controlled test and built-in self test (BIST) to

deliver the test coverage that is disappearing from the older, intrusive test technologies. The NBT technologies typically require electrical contact to only a small set of board signals and these are often (or should be) brought out to a card edge, header, etc. as they are used at least for product commissioning (such as in-system programming).

As noted, the NBT technologies use the embedded instrumentation contained within the on-board silicon to deliver board test coverage, rather than relying on substantial external access. Embedded instruments are intellectual property (IP) blocks, either standardized or proprietary, within devices that facilitate validation, test and debug of chips, boards and systems. Control and access is typically via the Test Access Port (TAP) defined by IEEE Std. 1149.1 (JTAG).

Final Destination: Economic Benefits of NBT

When compared to the older intrusive test methodologies, NBT technologies are more agile, software-driven and much more cost-effective. Whereas basic ICT systems often come with a starting price tag in excess of $250,000 and a life-cycle cost over a million dollars, a personal computer-based NBT station can be deployed in a manufacturing line for less than $25,000; a tenth of the cost of an ICT system. In addition, NBT does not require complex test fixtures, which are expensive to produce and maintain, especially when every design change triggers the production of a new fixture.

NBT can counteract the ever-escalating cost of intrusive test technologies. Because it is software driven, NBT is extremely flexible and very adaptable. In particular, NBT can be quite efficient when new product designs are transitioning from development to high-volume manufacturing. During this phase of a product's lifecycle, circuit board designs are still being qualified and numerous design changes are being made. For example, if ICT were the board test technology used on beta versions of a new board design, an ICT test fixture costing tens of thousands of dollars would be needed for each batch of prototype boards produced. Moreover, another version of the ICT test fixture would be needed whenever the qualification process discovered a flaw that triggered a design change. The cost of ICT test fixtures can escalate quickly. In contrast, NBT is not limited by test fixtures. A design change might trigger a software change or the

recompilation of a circuit board's NBT tests, but expensive hardware re-spins of test fixtures are avoided entirely.

What is Non-intrusive Board Test?

Unlike the older generations of electrical test technologies, non-intrusive board test (NBT) does not involve placing a metal probe on a circuit board, test pad or chip pin to test the electrical continuity of the connection between the chip and the trace on the circuit board. For NBT, a simple connector on the printed circuit board links the board, often by way of the 1149.1 (JTAG) TAP, to the software-driven NBT test station, which is typically operated on a personal computer (PC).

Essentially, NBT technologies apply electrical tests by way of on-chip instruments that are embedded within the circuit board; readily available embedded instruments include the 1149.1 boundary-scan architecture, emulation-based processor run control, input/output (IO) built-in self test, core built-in self test, etc. The embedded instruments are invoked to exercise the chips and thus, the board; test responses are observed and any failures are analyzed to assess the integrity of the board and its constituent structures. Extensive diagnostic capabilities pinpoint the locations of defects to facilitate rapid repair.

In addition, a host of other technological advancements are moving test strategies away from the older intrusive test technologies. These include several industry standards of the IEEE. For example, IEEE P1149.7 defines a compact two-wire boundary scan interface that enhances the TAP with capabilities for ease of access to multi-die chips, like system-in-package (SIP), system-on-a-chip (SOC) and others. And IEEE P1687 is being developed to define the access to, and management of core and IO instruments on chips.

Several currently deployed test technologies fall under the NBT rubric, including boundary-scan test, processor-controlled test, and built-in self test technologies, such as Intel® IBIST (Interconnect Built-In Self Test), as discussed below.

Boundary-Scan Test

Boundary-scan test, based on IEEE Std 1149.1, was conceived in the 1980s and adopted as a standard in 1990. Its adoption was accelerated in the mid-1990s because fine-pitch pins on chips could not be probed or the pins were disappearing under the silicon die in ball grid array (BGA) packages. Boundary-scan tests are applied to a circuit board through a connector and the four-wire serial interface on the 1149.1 TAP. When implemented, this interface is commonly referred to as the 'JTAG port', after the name of the working group that began development of the standard in 1985, the Joint Test Action Group.

Since its development, this standard test access port and boundary-scan architecture has been adopted extensively by the industry and it is now deployed in chips, on circuit boards and in systems. Because of its widespread acceptance, the boundary-scan infrastructure has been appropriated by other applications and related standards. It is used to program logic and memory devices in-system, for example as defined by IEEE Std 1532, and it provides the basis for IEEE Std 1149.6 for testing high-speed, differential and/or AC-coupled, advanced digital networks as well as other standards (IEEE 1149.4, P1149.7, P1149.8.1, P1687, etc.).

Processor-Controlled Test

Processor-controlled test (PCT) makes use of a debug port, which is most often a modest expansion of the 1149.1 (JTAG) TAP, to access a processor's on-chip emulation/run-control instrument. By way of the run control facility, control of the processor is assumed by the test station so that test routines can be applied at processor speeds through the input/output pins that connect devices on the circuit board to the processor. In this way, PCT propagates test patterns through the processor onto the structural interconnects of the circuit board. PCT can exercise the functionality of the circuit board as well as detect and diagnose structural faults.

As an inherently functional test, PCT is device- and bus-centric; that is, it will exercise the devices and buses on a circuit board. In addition, because it operates at CPU speeds as an "at-speed" test, it will detect faults which only manifest themselves while the board is running at operational speeds. Static tests such as ICT, MDA, flying probe and boundary scan, on the other

hand, are effectively DC tests. And of course, PCT, which reads and writes from/to targeted devices on a board, verifies these aspects of the board's functionality, which static tests cannot.

Built-in Self Test

Built-in Self Test (BIST) commonly refers to test mechanisms or instruments that are embedded into chips and which can be applied in non-intrusive board test applications. A particular example of this is Intel® Interconnect Built-In Self Test (IBIST) technology which is being embedded by Intel, Avago and other semiconductor and IP providers into next-generation chips and chip sets. The embedded Intel IBIST functionality can be applied in a number of ways, including structural tests in NBT applications.

For Intel processors, the same debug port interface which is used for access to boundary scan and processor-controlled test also pertains to Intel IBIST. Intel IBIST can test high-speed serial buses such as Intel® QuickPath Interconnect (QPI) and PCI Express (PCIe) links on a PCB where test pads cannot be inserted because they would disrupt the signal integrity of these interconnects, adversely affecting functional performance.

Coverage Assessment Methodology

The overall goal of any test strategy is to provide maximum coverage at minimum cost, as illustrated in Figure 1.

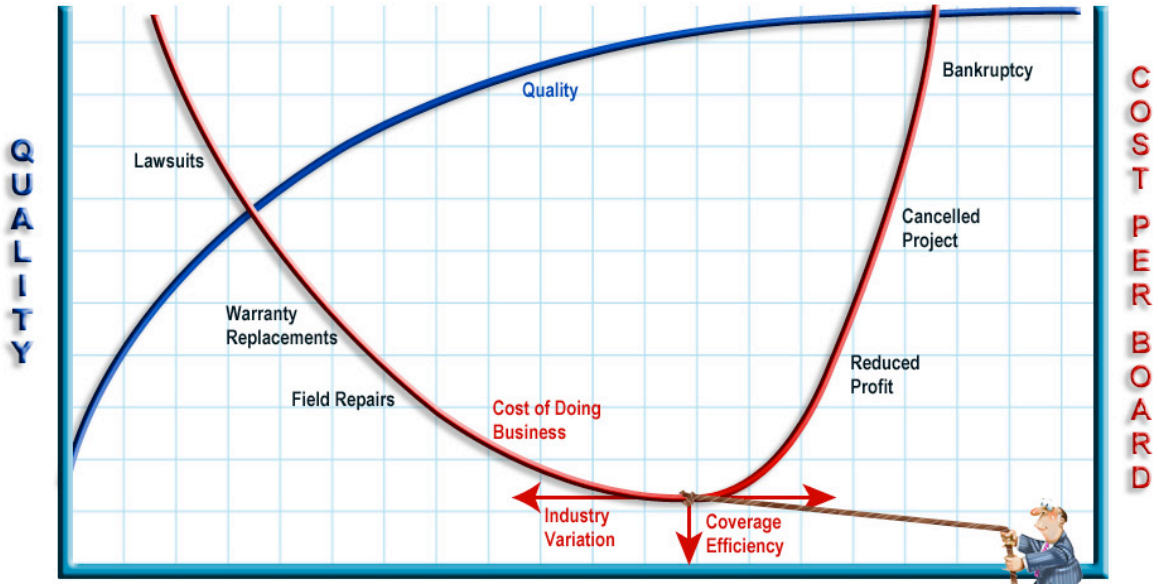


Figure 1: Coverage Optimization

Coverage that is too low will result in significant warranty returns and a high cost of replacements after the product is released in the field. Coverage that is too high becomes exorbitantly expensive and can dramatically affect a product's total loaded cost, driving up price and making it uncompetitive in the market.

But what does coverage really mean and how is it defined?

Defects and the Defect Universe

Over recent years, several frameworks have been proposed for evaluating defect coverage in a test-neutral fashion: PCOLA/SOQ[ii] was introduced to assess such coverage on a structural basis. iNEMI has proposed PCOLA/SOQ/FAM[iii] as a model that accounts for the unique value of board functional test above and beyond structural test methods. With the emergence of NBT as a new methodology to be considered in a total board test strategy, its overall impact within that strategy needs to be assessed.

NBT, which provides for elements of both structural test and functional test and a further aspect of performance test, should be considered within a similar framework. Parker[iv] gives guidance on how boundary-scan test can be assessed within the PCOLA/SOQ framework. The impact of processor-controlled test (PCT) on overall board test strategy has been explored by Fenton and

Hammond[v]. Johnson[vi] provides guidance on the effectiveness of Intel® IBIST (Interconnect Built-In Self Test) to detect structural defects.

These efforts need to be fully considered, but further extended to comprehend the full spectrum of faults addressed by NBT, which as previously noted, may include at-speed faults and insufficient-margin faults beyond the conventional shorts and opens faults. In so doing, the ability of NBT to cover the complete breadth of the defect universe (as in Figure 2) can be fully assessed.

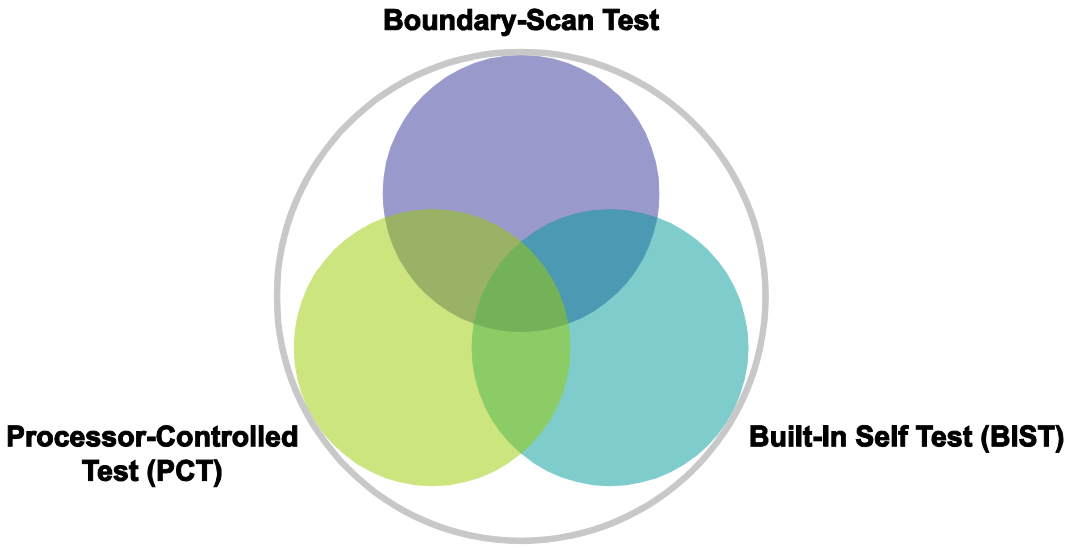


Figure 2: NBT Covers the Defect Universe

Keep in mind that, in practice, it is impossible to achieve the holy grail of 100% test coverage. In the generalized case there is always an additional measurement that can be made or a corner case which is unaddressed. The directive of test engineering is to get the most efficient and effective strategy in place, and this strategy may vary based on a given board's characteristics.

Properties of Devices and Connections (PCOLA/SOQ/FAM)

A summary of the defect properties assigned to devices and connections in the iNEMI PCOLA/SOQ/FAM framework is illustrated in Figure 3.

Structural: *Devices*	**P**	Presence
	C	Correctness
	O	Orientation
	L	Live
Structural: *Connections*	**A**	Alignment
	S	Shorts
	O	Opens
Functional: *Devices & Connections*	**Q**	Quality
	F	Feature
	A	At-Speed
	M	Measurement

Figure 3: iNEMI PCOLA/SOQ/FAM Framework

The defect universe for a given board to be tested is enumerated by assigning the relevant properties to each of its structural elements, devices and/or connections. While most of these properties are fundamental, meaning that they pertain only and directly to the element of interest, the shorts property is associative. The shorts properties are enumerated such that, for a given connection, "C," a "short-P-to-X" property is instantiated for each other connection, "X," within a predetermined proximity (typically within a circle of a defined radius that is centered on "C"). The properties in the functional class, FAM, may be assigned to either devices and/or connections, as appropriate.

Tests

All tests, whether structural or functional in nature, are assessed versus the defect universe by viewing each defect in turn against the rhetorical question: "What does it mean when a test passes?" If it can be determined that a given test can pass only in the absence of the given defect, then that defect can be said to be covered by that test.

Grading Non-intrusive Board Tests, a Case Study

For the purpose of exploring the application of the PCOLA/SOQ/FAM coverage assessment framework in the grading of NBT, a case study will be considered. This grading will be evaluated in the context of a design based on the Intel® Xeon® Processor 5500 Series, as

illustrated in Figure 4. Implementation matters for such designs are detailed in a separate whitepaper[vii].

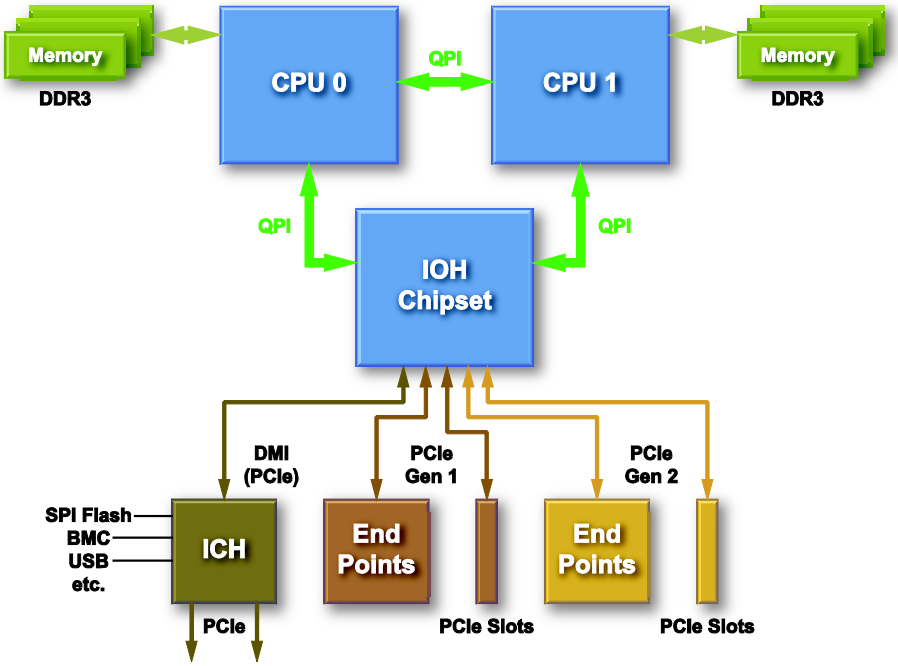


Figure 4: A Common Topology for Intel® Xeon® Processor 5500 Series-based Design

Virtually all of the board can be tested using NBT.

With good board design-for-test (DFT), boundary scan can be used to test where it is impossible to put test pads, such as on the QPI links (shown in green). Boundary scan can also be used to reduce the number of test points needed, dramatically reducing fixture costs. And boundary scan can be used for the lifecycle of the product, from prototype, through manufacturing, and repair and return.

Processor-controlled test can exercise the kernel of the board's devices and buses with an at-speed functional test, again reducing the need for test points. And because it is a low-level (pre-boot) functional test, processor-controlled test can run without the BIOS or OS loaded, it has excellent diagnostics and runs much faster than traditional functional tests.

Intel IBIST can be used to validate the shape and size of an eye diagram via margining tests, and also the Bit Error Rate (BER) requirements on QPI and PCIe links. With a four-corner or fast-cross test, IBIST can also verify the link speed, determine the size of the eye, and detect some structural faults in production test.

Each of these NBT constituents (boundary scan, processor-controlled test and Intel IBIST) will be elaborated in turn and it will be demonstrated how they benefit coverage.

Boundary-Scan Test

The overall test strategy for Intel® Xeon® Processor 5500 Series-based designs should focus particularly on QPI and PCIe interconnects, as these buses use high-speed serial signaling and thereby preclude the use of test pads used by legacy bed-of-nails technologies. Boundary scan is essential for QPI nets, as there is no other deterministic means of detecting shorts and opens thereon, and as QPI constitutes the main bus through which all processor traffic runs, its performance is critical.

PCIe is an AC-coupled high-speed serial bus, and IEEE 1149.1 DC signals cannot traverse the capacitor. IEEE 1149.6 could play a role here within the boundary-scan test technology, but it is not supported in this case. Hence, boundary scan by itself does not suffice, but processor-controlled test (PCT) and Intel IBIST provide viable test solutions.

As well, boundary scan by itself cannot be used to detect shorts and opens on the memory buses. Other technologies must be used, such as processor-controlled test (PCT), which is discussed in the next major section.

On the whole then, where boundary-scan test is supported by the CPU and the chipset, particularly on the QPI bus, it provides adequate coverage against the PCOLA/SOQ matrix. Of course, even for those devices and connections to which it pertains, boundary-scan test provides no coverage against the FAM properties.

Processor-Controlled Test

PCT uses emulation technology to read and write memory and registers throughout all CPU-addressable devices on a board, by which means structural and functional faults can be identified. It has the advantage of being independent of board DFT, as long as the debug port guidelines are followed, making it much simpler to implement than other technologies.

PCT takes control of the CPU via its debug port. PCT then instructs the processor to sequentially test all addressable devices on the board under test. These tests are normally carried out without booting the board to its operating system, so device initialization is handled by the PCT test program in place of the BIOS.

From a functional point of view, PCT can test all CPU-addressable devices, including the DDR3 memory and PCIe devices that boundary scan is unable to test. Structural faults are also detected and diagnosed as a by-product of the functional testing.

Processor-controlled test provides coverage against the PCOLA/SOQ matrix on nets where it may be difficult to place a test point, or on nets that are not testable via other methods, such as QPI, PCIe, nets that are not covered by boundary scan due to device non-compliance or board DFT issues, etc. PCT also supplements traditional static testing with an at-speed fault coverage spectrum and so picks up some coverage of the Feature and At-speed properties from the FAM side of the matrix.

Built-In Self Test

For our case study, Intel® IBIST is ubiquitous and typifies the benefits of BIST in the suite of NBT technologies. Special 1149.1 instructions set up the tests, start them, determine when they complete, and read back failure information. The actual pattern generation and error checking is done by the Intel IBIST embedded instruments at speeds much greater than boundary scan can support.

For QPI testing, both the CPU(s) and IOH(s) can be used as masters and slaves respectively, fully exercising all links bi-directionally. For PCIe testing between the PCIe switches and

slots/risers, plug-in cards that establish communication with the PCIe bus controller are required. Since Intel IBIST testing of the PCIe bus is done in loopback mode, both sides will be covered.

IBIST is a functional test which uses pseudo-random bit sequence (PRBS) patterns as a foundation for pattern generation and checking, bit error rate testing (BERT) and margining. Much research has gone into how this technology would catch real-world manufacturing problems such as various shorts to the bus, missing parts, and incorrectly installed parts (e.g. tombstoned capacitors).

IBIST pattern generation and checking, although comprehensive on difficult-to-test QPI and PCIe nets, does not provide total structural test coverage. So it should certainly be used in conjunction with processor-controlled test, and with boundary scan (especially if IEEE 1149.6 support on PCIe is available). It should be noted that high-speed serial nets of these sort are expressly immune to common mode noise induced by some structural faults, in which case the links will “appear” to operate normally; but IBIST as a manufacturing test will capture link degradation indicators.

In order to detect QPI and PCIe lane performance degradation, the more advanced capabilities of IBIST BERT and margining are applied. For example, marginalities such as component drift across different device lots, trace defects, solder voids or micro-cracks, missing or bad terminations/capacitors, etc. can result in a degraded eye or high bit-error rate.

The total picture for BIST then includes coverage of At-Speed and Measurement (BER) aspects of the FAM matrix.

Summary

Bringing all of the elements of NBT together for this case, as exemplified by the Intel® Greencity Reference Platform, we see the coverage picture of Figure 5. The assessment of total coverage versus the PCOLA/SOQ/FAM matrix is presented in Figure 6.

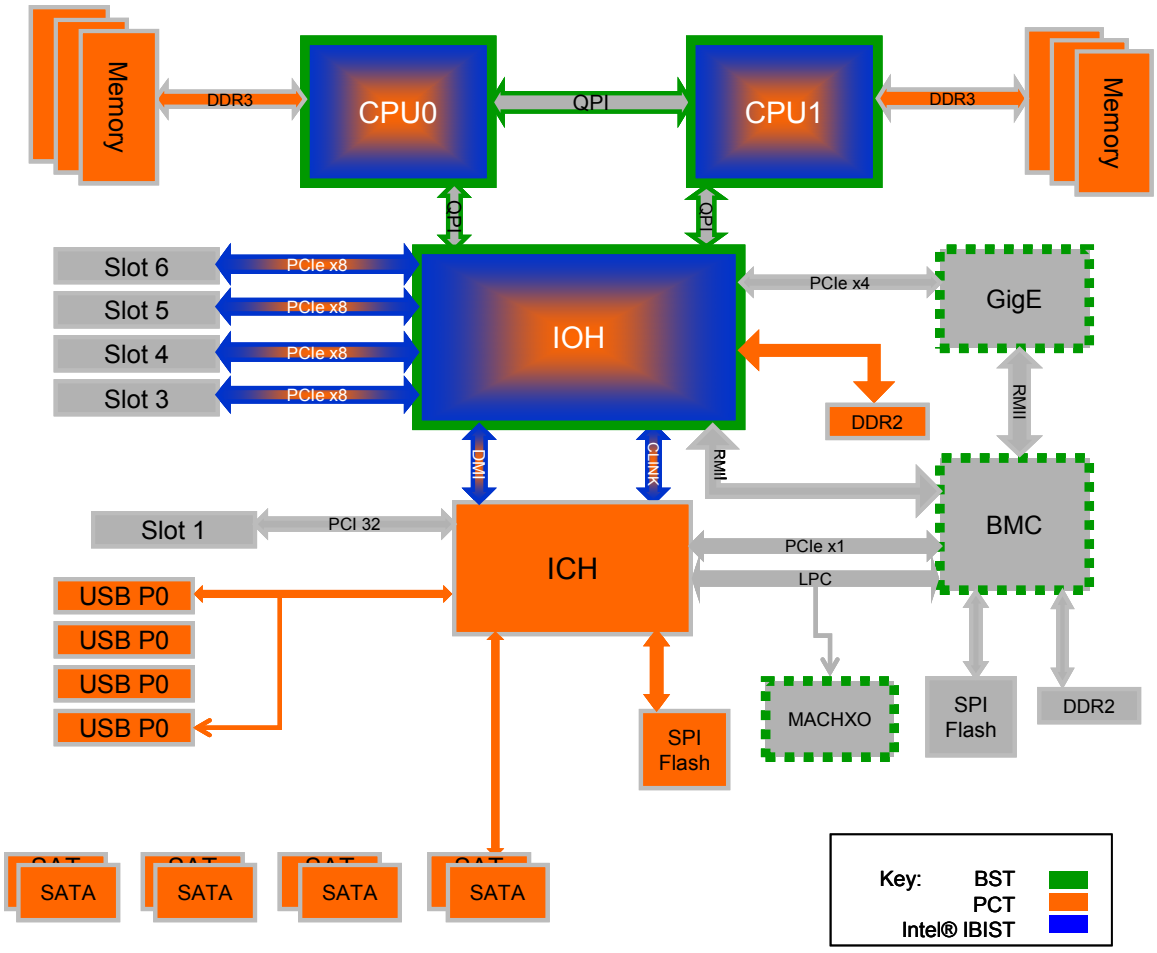


Figure 5: Block Diagram View of NBT Coverage for Intel® Greencity

Structural: *Devices*	**P**	Presence	✓✓✓
	C	Correctness	✓✓✓
	O	Orientation	✓✓✓
	L	Live	✓✓✓
	A	Alignment	
Structural: *Connections*	**S**	Shorts	✓✓✓
	O	Opens	✓✓✓
	Q	Quality	✓
Functional: *Devices & Connections*	**F**	Feature	✓
	A	At-Speed	✓✓
	M	Measurement	✓

Key B-Scan
PCT
Intel ® IBIST

Figure 6: Defect Coverage for Non-intrusive Board Tests

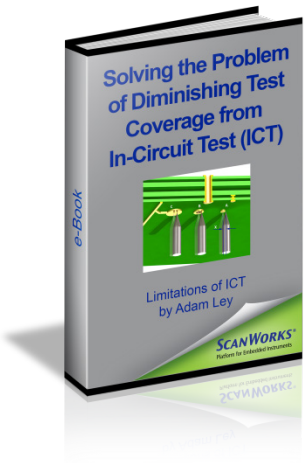
Conclusion

Along with this paradigm shift toward higher speed, smaller chips and denser/more complex printed circuit boards comes a raft of new testing challenges. For high-speed interconnections like QPI, PCIe, DDR3 and others, traditional test technologies suffer from the constraints of limited test access. New technologies which leverage the power of embedded instrumentation within silicon have resulted in non-intrusive board test solutions which complement or replace the older, intrusive technologies.

By evaluating the NBT strategy through the prism of the coverage assessment methodology, it can be seen that NBT, with all of its disparate elements, meets the testing requirements of today's real world designs. While none of the NBT technologies may stand on its own for the most challenging case, a strategy that deploys all of the NBT methods, boundary-scan test, processor-controlled test, and built-in self test, will deliver a robust and cost-effective test capability.

Learn More

In-circuit test seemed ideal for simplifying test generation and execution when it was first introduced. Fortunately, new test access standard and software-driven tools offer alternative to probe-based testing. To learn more, get our e-Book. "*Solving the Problem of Diminishing Test Coverage from In-Circuit Test (ICT)*".



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