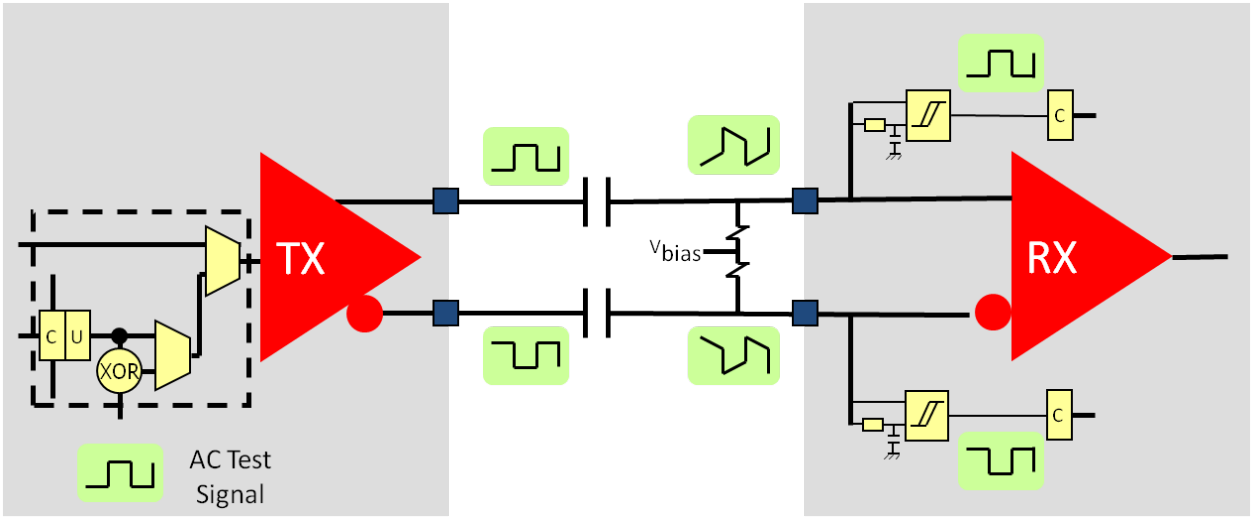
# IEEE 1149.6 Tutorial | Testing AC-Coupled and Differential High-Speed Nets





BY

Adam Ley

*By Adam Ley, Chief Technologist, Non-intrusive Board Test and JTAG*

Adam serves customers by ensuring that ASSET's non-intrusive board test (NBT) methodologies comprise a best-in-class solution to meet the evolving need for improved coverage of board test in the face of ongoing erosion of physical access. Pursuant to ASSET's strong support for standards, Adam is an active participant in IEEE 1149.1, having previously served terms as working group vice chair and as standard technical editor (for the 2001 revision), as well as in nearly all related standards, to include: 1149.4, 1149.5, 1149.6, 1149.7, 1149.8.1, 1500, 1532, 1581, P1149.1.1, iNEMI boundary-scan adoption, PICMG MicroTCA, and SJTAG (system JTAG). Adam's experience prior to ASSET spanned over a decade at Texas Instruments, Sherman TX, where he had roles in application support for TI's boundary-scan logic products and for test and characterization of new logic families. Adam earned the BSEE degree from Oklahoma State University, Stillwater OK, in 1986.

# Testing AC-Coupled and Differential High-Speed Nets

## A Tutorial on standard IEEE 1149.6

### Table of Contents



### List of Figures/Tables

## Executive summary

In recent years the deployment of advanced digital networks on circuit boards has grown tremendously. These chip-to-chip interconnects, which are largely comprised of AC-coupled and/or differential networks, are much more difficult to test electrically for structural faults than the DC-coupled and single-ended nets they supersede. Having recognized this challenge, an IEEE working group was formed to develop a suitable companion to IEEE 1149.1 boundary scan (JTAG). Its work, approved and published as IEEE 1149.6 Standard for Boundary-Scan Testing of Advanced Digital Networks, specifies supplemental boundary-scan cells for provision on advanced digital networks and corresponding boundary-scan instructions that are capable of generating stimuli and capturing responses in a manner suitable to the presence of AC coupling and/or differential signaling. This tutorial explores the background that gave rise to IEEE 1149.6 and explains its basic features. This tutorial is not a replacement for a careful study of the complete standard IEEE 1149.6 specification, which can be found at: http://standards.ieee.org/findstds/standard/1149.6-2003.html

## Why is IEEE 1149.6 needed?

The original IEEE 1149.1 boundary scan standard was developed primarily for DC-coupled and single-ended interconnects such as shown in Figure 1.

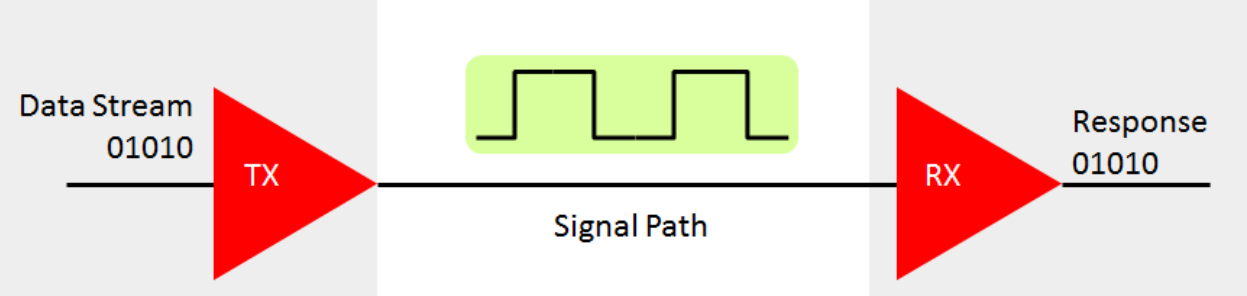



**Figure 1: DC-coupled single-ended signaling**

While it makes some allowance for differential interconnects, such as shown in Figure 2, the design and provision of IEEE 1149.1 boundary-scan cells can result in poor test coverage of such interconnects depending on if each differential lead in the pair is equipped with boundary scan cells. It is not unusual that only one of the leads in the pair has a boundary-scan cell, resulting in

fault detection on only one of the nets. Or the boundary scan cell is implemented behind the differential driver or receiver, resulting in fault detection only to the pair level rather than net or pin-level detection.

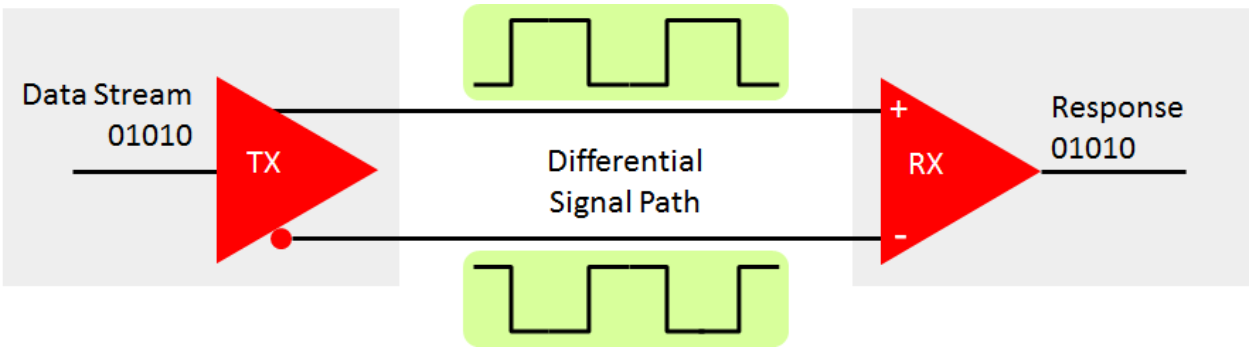



**Figure 2: DC-coupled differential signaling**

Further, since the IEEE 1149.1 boundary-scan cells are restricted to the domain of DC stimuli, there's no test coverage at all for interconnects that are AC coupled, see Figure 3.

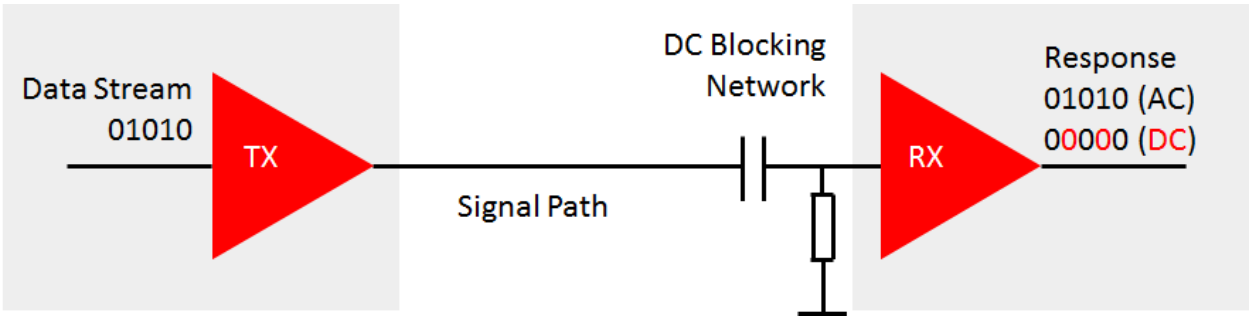



**Figure 3: AC-coupled single-ended signaling**

On the other hand, interconnects that are AC coupled or differential or both, as Figure 4 shows, have become more prevalent.

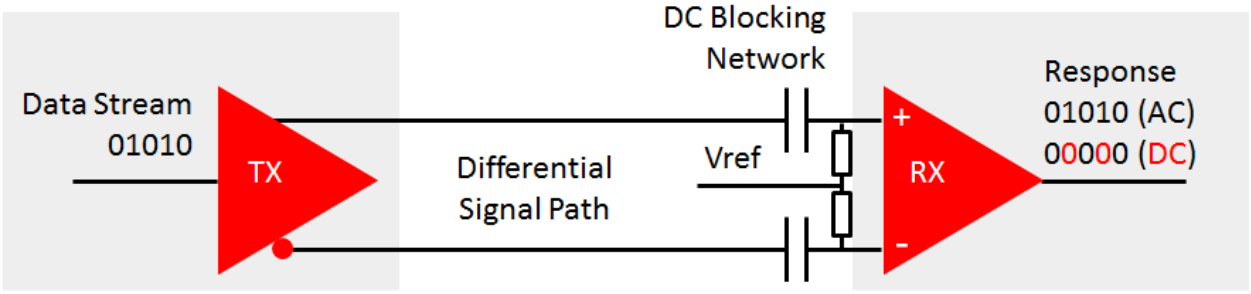



**Figure 4: AC-coupled differential signaling**

Further to the point, all of the buses listed in Table 1 comprise interconnects that are capable of high-speed transmission, exceeding at least 1 gigatransfers per second per lane (GT/s). Several now exceed 5 GT/s. As the speed of such buses increases, great care must be taken in design and layout of the printed circuit board, often requiring differential signaling for reliable communications. Moreover, some of these buses allow for the transmitters and receivers in different devices to operate at different voltage levels (DC offset). When this is the case, the interconnects must be AC coupled.

**Table 1: High-speed buses on circuit boards**

| | |
|---|---|
| Fibre Channel | www.fibrechannel.org |
| Gigabit Ethernet | standards.ieee.org |
| HyperTransport | www.hypertransport.org |
| Infiniband | www.infinibandta.org |
| PCIe (PCI Express) | www.pcisig.com |
| RapidIO | www.rapidio.org |
| SATA (Serial ATA) | www.serialata.org |
| QPI (Intel® QuickPath Interconnect) | www.intel.com |
| XAUI (10GbE Attachment Unit Interface) | standards.ieee.org |

## Differential signaling

At higher speeds in the range of 1 GT/s and higher, interconnects become more susceptible to electrical noise which compromises the integrity of the data transferred across the line. Corrupted data could be received or system performance could degrade as the result of retransmission of data to get it right.

One source of noise on an interconnect is signal reflection at the receiving end of the line. As the slew rate (voltage/time) of the signal increases, amplitude of reflections is exacerbated with the result that the integrity of the signal is compromised. Differential networks address this problem by employing two wires to transmit the same data (see again Figure 2 and Figure 4). The receiver compares these two signals, operating on the difference, which is twice the amplitude of the singulated signals and so is less prone to error.

The effective doubling of signal voltage at the differential receiver allows for lower single-ended voltages, which in turn allows the use of low voltage differential signaling (LVDS). Reducing

the voltage in this way not only reduces power consumption of the system, but also effectively lowers the signal slew rate for a given data rate (transfers/time). This, in turn, provides for reduced amplitude of reflections at a given data rate and acceptable signal integrity at a higher data rate.

Other sources of noise are cross talk and ground bounce, which present as common mode noise, meaning that both legs of the differential network see the same noise signal. Since the differential receiver operates on the difference between the positive and negative legs, noise that is common to both legs is effectively rejected. The reduced signal slew rate of LVDS also provides further benefits for reduction of crosstalk, ground bounce and radiated emissions.

The system-level benefits of AC-coupled and/or differential low voltage interconnects can be summarized as:

1. Lower signaling voltage
2. Reduced power consumption and heat
3. Higher data rates
4. Lower emitted noise
5. Greater noise immunity

Given these benefits, the presence of AC-coupled and differential interconnects is expected to become even more ubiquitous, which makes solving the problem of how to test them all the more critical.

## AC coupling

An AC-coupled net cannot be adequately tested with standard IEEE 1149.1 boundary scan because the boundary-cells only present DC level (see again Figure 1 and Figure 2) and, as a result, cannot transfer stimuli through an AC coupling such as a DC blocking capacitor (see again Figure 3 and Figure 4). In other words, with reference to Figure 3, if the signal driven from the device on the left has a voltage offset with respect to the signal to be received by the device on the right, then the DC component of the signal must be blocked (such as with the illustrated

capacitor), creating an AC-coupled connection, which allows for the drivers and receivers to be biased independently such that each is optimized for its own design and process technologies.

Unfortunately for boundary-scan test, this prevents the use of DC stimuli per conventional IEEE 1149.1. Alternatively, then, IEEE 1149.6 defines a boundary-scan method that is suitable for transferring stimuli across an AC coupling, thus enabling the generation of test patterns for shorts and opens on AC-coupled nets (see again Figure 3 and Figure 4).

## Where are AC-coupled interconnects found?

Many high-speed interconnects occur between serializer/deserializer (SERDES) devices, such as shown conceptually in Figure 5.

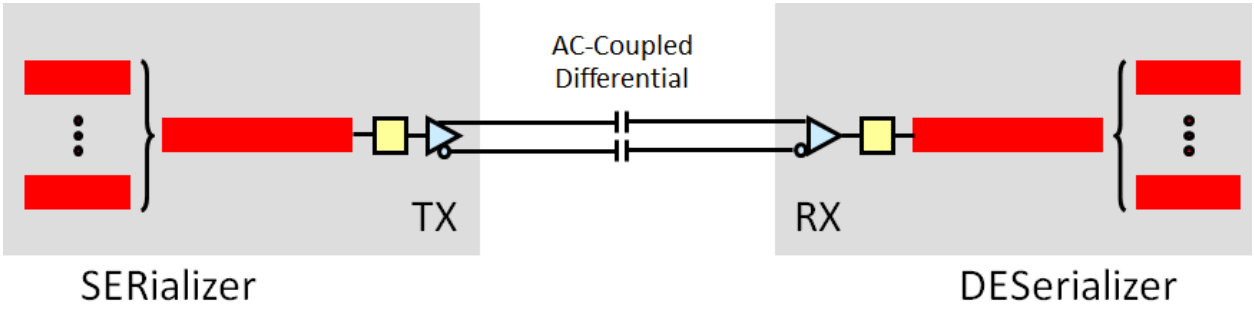



**Figure 5: SERDES concept**

SERDES devices process data in multiple parallel registers at a relatively low rate, such as 200 megatransfers per second (MT/s). Before transmission, all parallel data is collected into a serializing register and transmitted at a much higher frequency.

A simple illustration of this process might involve 10 parallel registers of equal length and working at 200 MT/s collecting data into a single serializer register. This data would then have to be transmitted at the least 10 times the internal speed of the parallel registers of 2000 MT/s or two GT/s.

At the receiving end of the transmission line, a SERDES receiver would place the data into a single register at two GT/s and then break it back down into blocks of data that could be inserted into multiple parallel registers where it would be processed at the original rate of 200 MT/s.

This example points out that the transmission speed on a SERDES line is much faster than the on-chip data processing rate, most often necessitating an AC-coupled and/or differential interconnect.

IEEE 1149.6 plays a critical role by detecting shorts and opens at the external bonding points of such devices and along the external interconnections between them. See Figure 6 for a representation of the different parts of these interconnects. Of course, the fault-tolerant nature of differential signaling systems means that some defects may still escape detection by the relatively low-frequency testing enabled by IEEE 1149.6. Such defects on differential interconnect may dictate a higher-frequency test strategy, but such methods in general are outside the scope of this IEEE 1149.6 tutorial. If information on such methods is of interest, more information can be found at: [http://www.asset-intertech.com/Solutions/High-Speed-I-O-Check](http://www.asset-intertech.com/Solutions/High-Speed-I-O-Check).

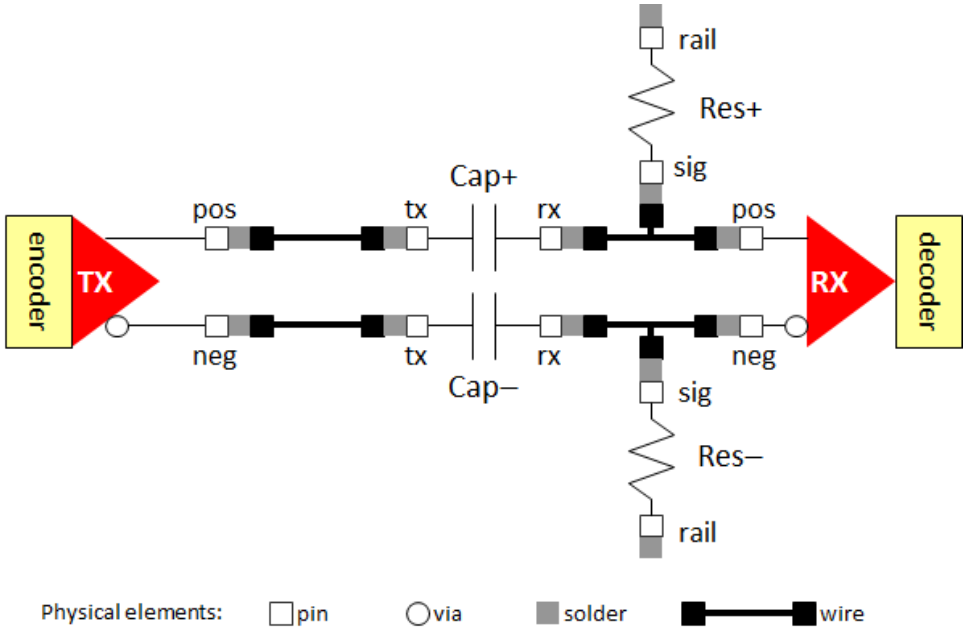



**Figure 6: IEEE 1149.6 interconnect parts**

## IEEE 1149.6 supplemental architecture

Although the objective of IEEE 1149.6 is to solve test problems associated with high-speed buses based on AC-coupled and/or differential interconnects, this test method must also work with DC-coupled and/or single-ended interconnects since circuit boards may contain both of these types. Of course, testing an AC-coupled line requires a time-varying signal as opposed to the static time-invariant signal found on DC-coupled pairs. This is the main feature that differentiates the IEEE 1149.6 boundary-scan architecture from that of IEEE 1149.1.

IEEE 1149.6 specifies a modified boundary-scan cell upstream of the differential driver (Figure 7, left side). This cell is capable of delivering a single pulse or a train of pulses to the individual legs of the interconnect pair (as a function of the contents of the boundary-scan cell update latch and the TAP controller state).

The standard also calls for a special form of test receiver on each receiving leg (Figure 7, right side). These edge sensitive receivers are capable of determining whether the incoming AC signal is rising or falling. A rising edge on a leg indicates that its signal voltage level is increasing, while a falling edge on a leg indicates that its signal voltage level is decreasing. In this way, the incoming AC signal is digitized and the result is captured in normal boundary-scan cells placed at the outputs of the test receivers. Under normal circumstances, the values captured in the two receiver scan cells should always be complementary.

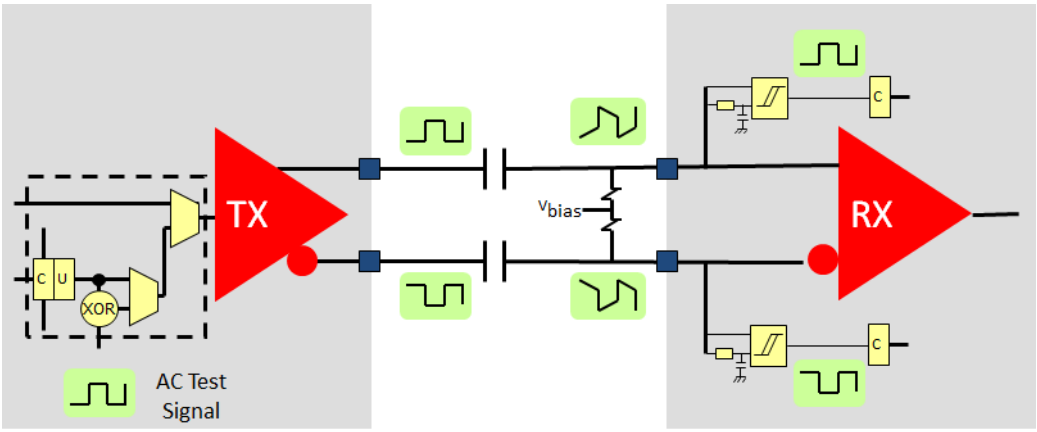



**Figure 7: IEEE 1149.6 interconnect test solution**

As a result, IEEE 1149.6 affords much better fault coverage, particularly of opens, and there is no impact on mission-mode performance.

Figure 8 offers more detail on the IEEE 1149.6 modified driver boundary-scan cell. Essentially, multiplexers route a single AC pulse or train of pulses into the transmitter driver and onto the differential signal legs. Note that the actual signal into the driver can be either the AC test-signal, a DC test-signal coming from the boundary-scan cell or the mission-mode signal. In this way, such a boundary-scan cell will support IEEE 1149.1 EXTEST operations as well as the IEEE 1149.6 requirement to drive a pulse (or a train of pulses). This is an important consideration for a board that contains a mixture of IEEE 1149.1 and IEEE 1149.6 devices.

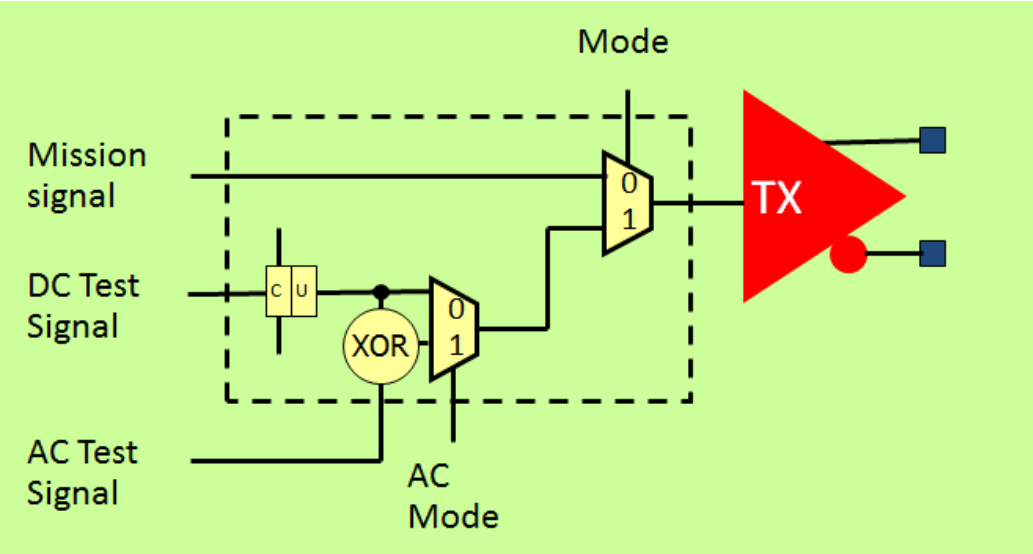



**Figure 8: Modified boundary-scan transmit cell for IEEE 1149.6**

Figure 9 shows the details of the IEEE 1149.6 test receiver suitable for both DC and AC EXTEST. At the single-ended receiver end, the AC signal is fed into what is called a hysteretic comparator, which compares the received signal with a delayed version of itself in order to determine the rising or falling nature of the signal. The output – a logic 1 if the signal is rising; a logic 0 if it is falling – is passed to the downstream boundary-scan cell where it can be captured and scanned out in the normal way.

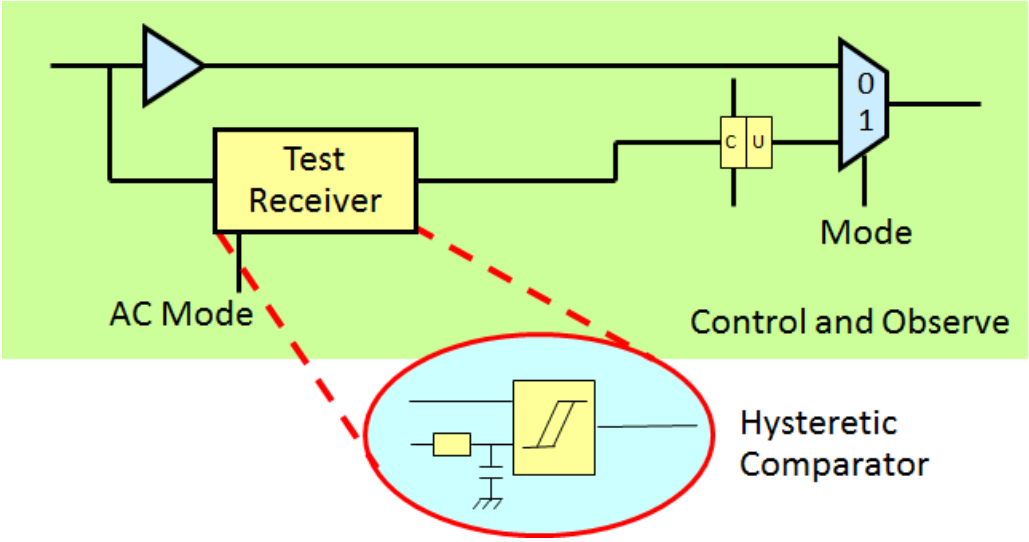



**Figure 9: IEEE 1149.6 test receiver and boundary cell**

## IEEE 1149.6 supplemental instructions

IEEE 1149.6 calls for two instructions that supplement those of IEEE 1149.1 so as to support the additional architectural features. These instructions (Figure 10) are EXTEST_PULSE and EXTEST_TRAIN.

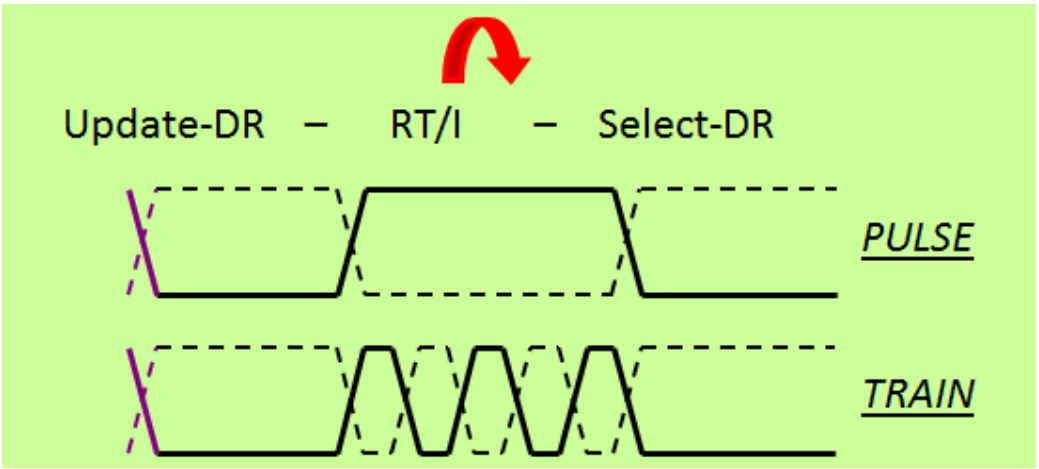



**Figure 10: EXTEST_PULSE and EXTEST_TRAIN**

As the name suggests, EXTEST_PULSE generates a single pulse. The pulse is framed by way of entry to (leading edge) and exit from (trailing edge) the Run-Test/Idle TAP controller state (Figure 11).

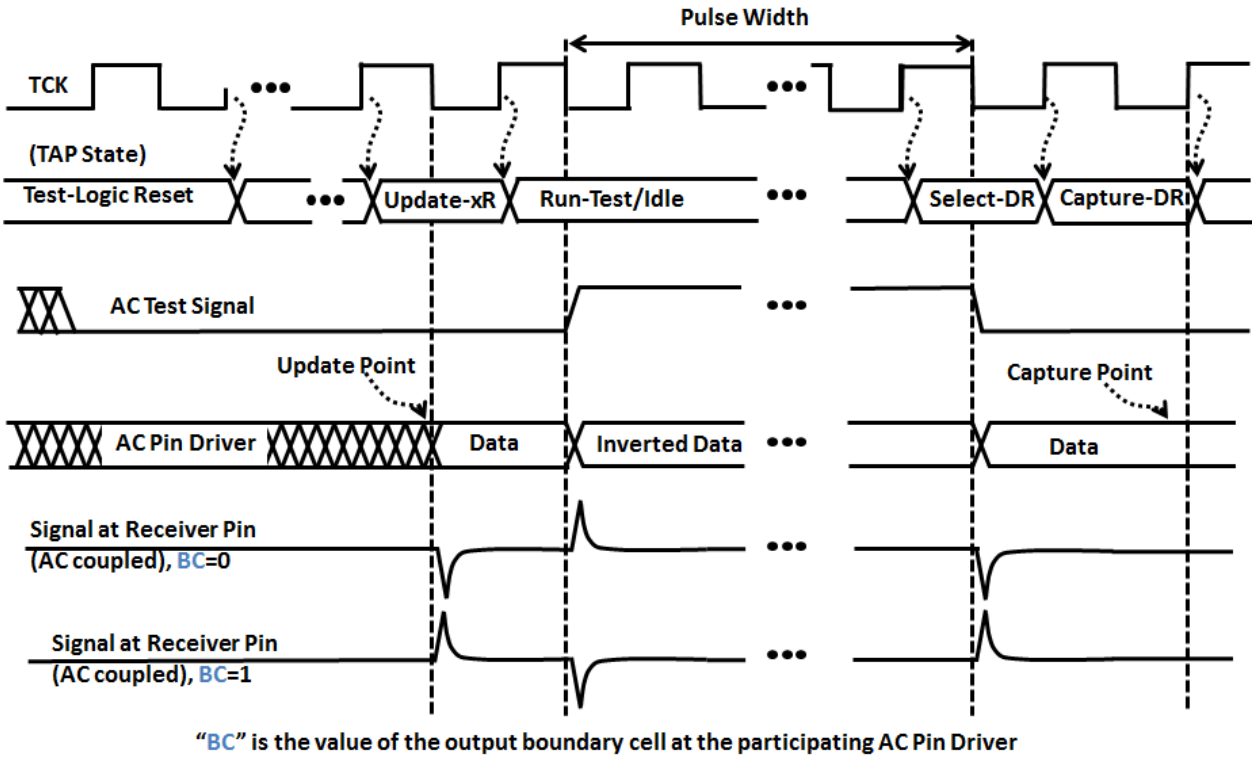



**Figure 11: AC signals when operating EXTEST_PULSE**

On the other hand, EXTEST_TRAIN generates a stream of pulses (Figure 12). The pulse train starts (initial edge) upon entry to the Run-Test/Idle TAP controller state and continues (toggle edge) on each subsequent rising TCK edge until the Run-Test/Idle state is exited.

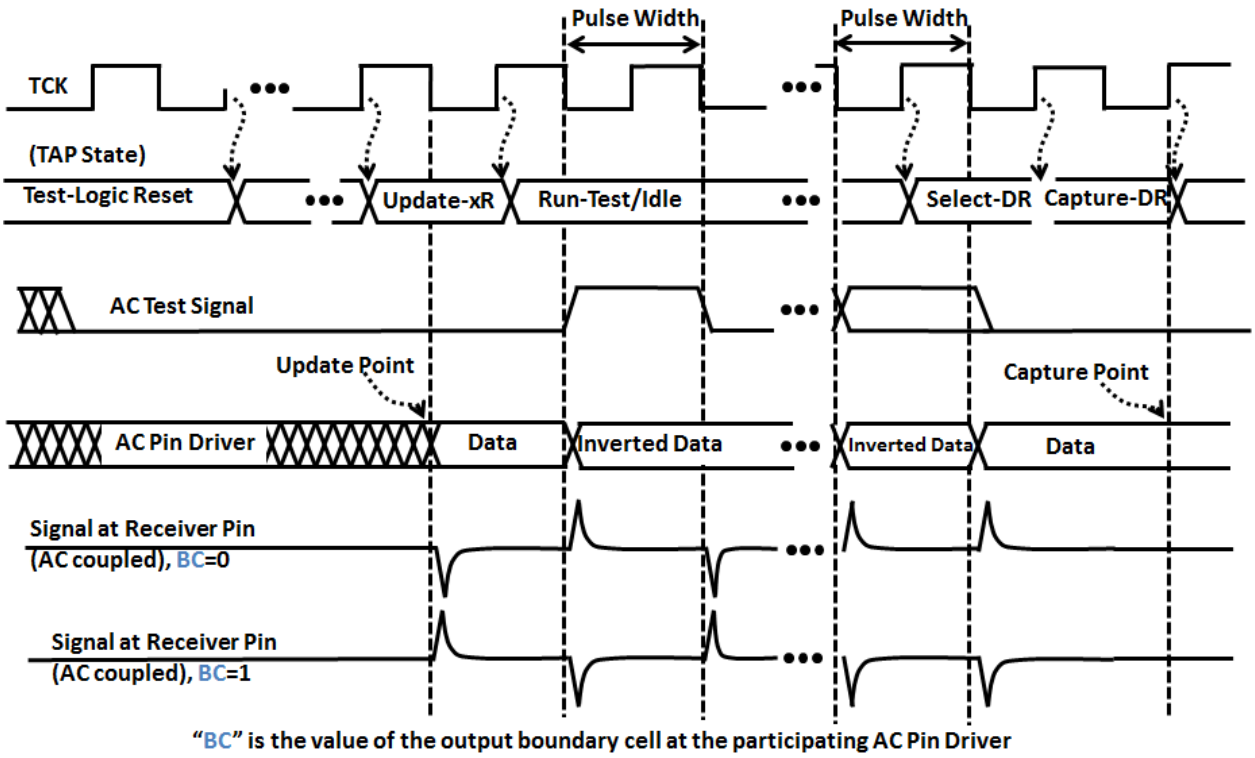



**Figure 12: AC signals when operating EXTEST_TRAIN**

In this way, either EXTEST_PULSE or EXTEST_TRAIN can generate target edges that are a function of the test data held in the update latches of the boundary-scan cells and establish the AC thresholds for the edge detectors in the IEEE 1149.6 test receivers.

## Conclusion: IEEE 1149.6 interconnect test - typical application

In one of the most common uses of IEEE 1149.6, a processor-based board is involved in communicating over a PCI Express (PCIe) bus to, for example, a video card, a memory card, an Ethernet communication, or to any other application specific devices. The interconnect test aspect of such is particularly interesting in board bring-up, prototype validation, and production, since the IEEE 1149.6 standard allows for pin-point fault detection without functional software running on the unit under test.

For example, looping back TX+/- to RX+/- over a PCIe connector, see Figure 13, will detect opens on the processor, connector or add-in loopback card due to missing BGA balls, connector plated through-hole issues, etc. by the means of IEEE 1149.6.

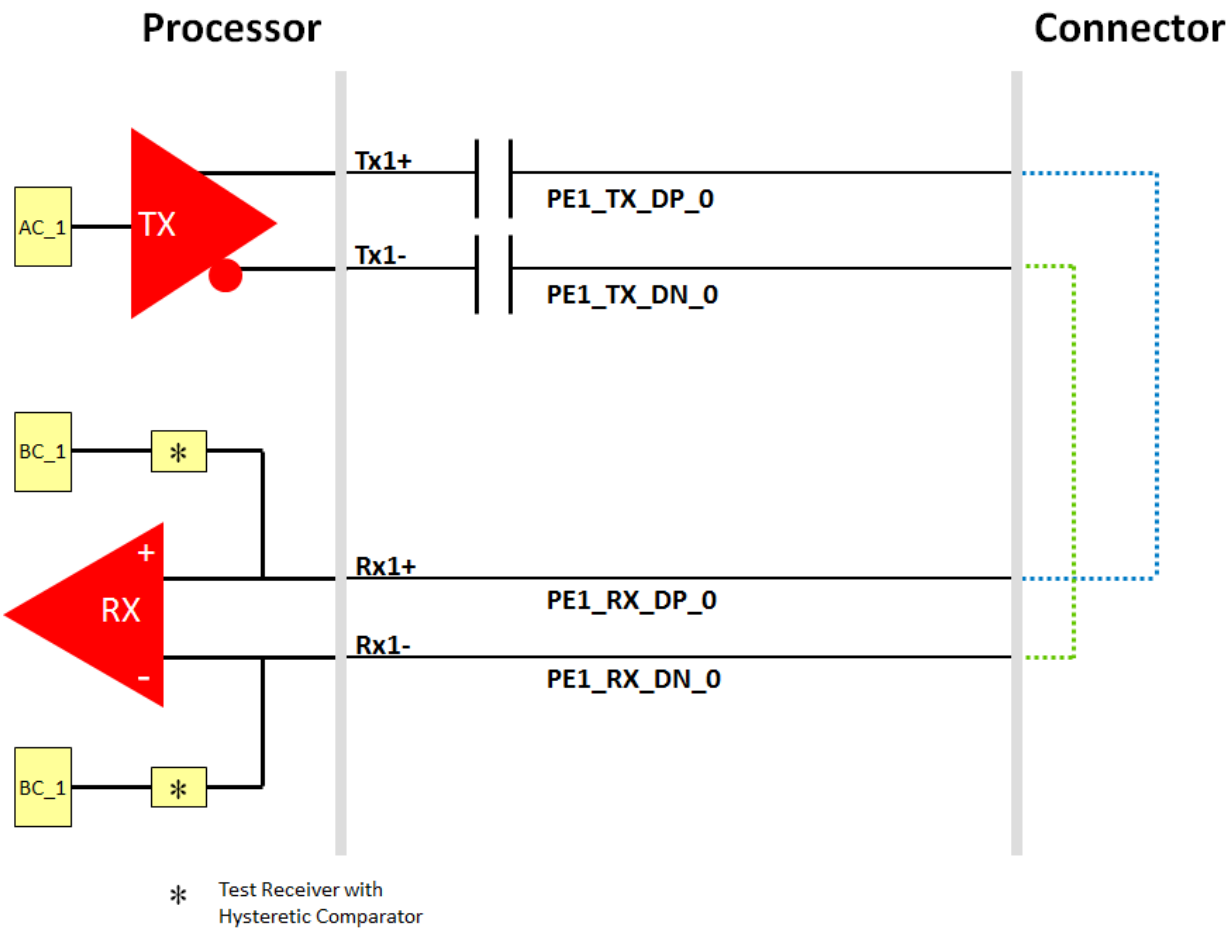



**Figure 13: Typical IEEE 1149.6 interconnect test application**

## References

"IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks," *IEEE Std 1149.6-2003*, 2003.

"IEEE Standard Test Access Port and Boundary-Scan Architecture," *IEEE Std 1149.1-2001*, 2001.

Duzevik, I., "Design and implementation of IEEE 1149.6," *Proceedings International Test Conference*, vol.2, pp.87-95, 30 Sept.-2 Oct. 2003.

Eklow, B., "An update on IEEE 1149.6 - successes and issues," *Proceedings International Test Conference*, pp.536-542, 8-10 Nov. 2005.

Eklow, B.; Barnhart, C.F.; Parker, K.P., "IEEE P1149.6: a boundary-scan standard for advanced digital networks," *Proceedings International Test Conference*, pp.1056-1065, 8-10 Oct., 2002.

Eklow, B.; Barnhart, C.; Ricchetti, M.; Borroz, T., "IEEE 1149.6 - a practical perspective," *Proceedings International Test Conference*, vol.1, pp.494-502, 30 Sept.-2 Oct., 2003.

Eklow, B.; Parker, K.P.; Barnhart, C.F., "IEEE 1149.6: a boundary-scan standard for advanced digital networks," *IEEE Design & Test of Computers*, vol.20, no.5, pp.76-83, Sept.-Oct. 2003.

Foutz, B.; Chickermane, V.; Bing Li; Linzer, H.; Kunselman, G., "Automation of IEEE 1149.6 boundary scan synthesis in an ASIC methodology," *Proceedings Asian Test Symposium*, pp.381-388, Nov. 2006.

Hong-Shin Jun; Sung Soo Chung; Sanghyeon Baeg, "Removing JTAG bottlenecks in system interconnect test," *Proceedings International Test Conference*, pp.173-180, 26-28 Oct. 2004.

Parker, K.P., *The Boundary Scan Handbook*, 3rd ed. Boston: Kluwer Academic Publishers, 2003.

Rearick, J.; Patterson, S.; Dorner, K., "Integrating boundary scan into multi-GHz I/O circuitry," *Proceedings International Test Conference*, pp.560-566, 26-28 Oct. 2004.

Sanghyeon Baeg; Sung Soo Chung, "Analytical test buffer design for differential signaling I/O buffers by error syndrome analysis," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.13, no.3, pp.370-383, March 2005.

Shaikh, S.A., "IEEE standard 1149.6 implementation for a XAUI-to-serial 10-Gbps transceiver," *Proceedings International Test Conference*, pp.543-550, 26-28 Oct. 2004.

Sung Soo Chung; Sanghyeon Baeg, "AC-JTAG: empowering JTAG beyond testing DC nets," *Proceedings International Test Conference*, pp.30-37, 30 Oct.-1 Nov., 2001.

Sunter, S.; Roy, A.; Cote, J.-F., "An automated, complete, structural test solution for SERDES," *Proceedings International Test Conference*, pp.95-104, 26-28 Oct. 2004.

Vandivier, S.; Wahl, M.; Rearick, J., "First IC validation of IEEE Std. 1149.6," *Proceedings International Test Conference*, vol.1, pp.632-639, 30 Sept.-2 Oct., 2003.

Whetsel, L., "Adapting JTAG for AC interconnect testing," *Proceedings International Test Conference*, vol.1, pp.641-650, 30 Sept.-2 Oct., 2003.

Young Kim; Lai, B.; Parker, K.P.; Rearick, J., "Frequency detection-based boundary-scan testing of AC coupled nets," *Proceedings International Test Conference*, pp.46-53, 30 Oct.-1 Nov., 2001.