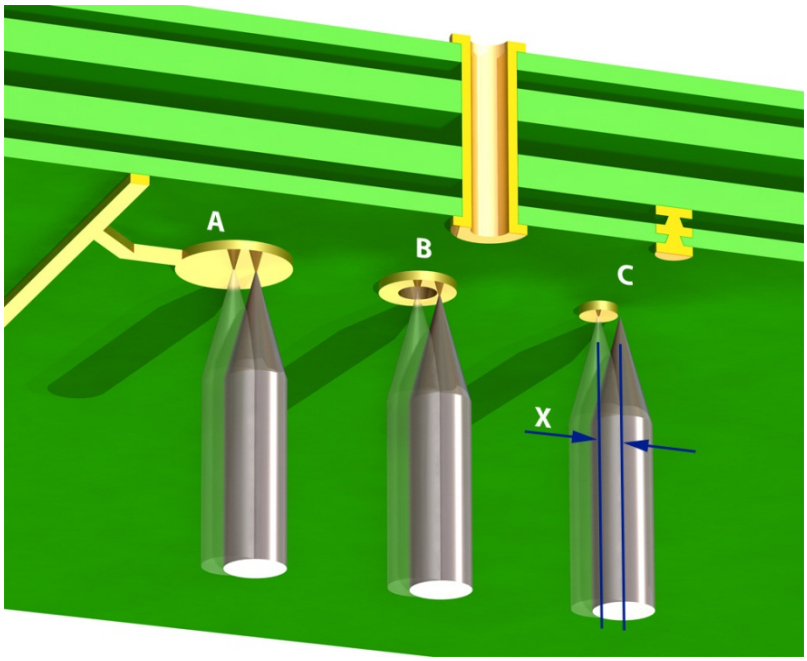
SOLVING THE PROBLEM OF DIMINISHING TEST COVERAGE FROM IN-CIRCUIT TEST (ICT)

Non-intrusive test technologies deliver test coverage beyond the reach of ICT



LIMITATIONS OF ICT WHITE PAPER

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Limitations of ICT White Paper

By Adam Ley, Chief Technologist, Non-intrusive Board Test

Adam serves customers by ensuring that ASSET's non-intrusive board test (NBT) methodologies comprise a best-in-class solution to meet the evolving need for improved coverage of board test in the face of ongoing erosion of physical access. Pursuant to ASSET's strong support for standards, Adam is an active participant in IEEE 1149.1, having previously served terms as working group vice chair and as standard technical editor (for the 2001 revision), as well as in nearly all related standards, to include: 1149.4, 1149.5, 1149.6, 1149.7, 1500, 1532, 1581, P1149.1.1, P1149.8.1, iNEMI boundary-scan adoption, PICMG MicroTCA, and SJTAG (system JTAG). Adam's experience prior to ASSET spanned over a decade at Texas Instruments, Sherman TX, where he had roles in application support for TI's boundary-scan logic products and for test and characterization of new logic families. Adam earned the BSEE degree from Oklahoma State University, Stillwater OK, in 1986.

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Executive Summary

Over the last few decades, in-circuit test (ICT) has been integral to the growth of the electronics industry. Now though, because of rapidly accelerating speeds and new levels of complexity, chips, circuit boards and systems are moving beyond the reach of the intrusive probes and bed-of-nails fixtures that ICT depends on. This white paper explains the technical and economic factors that are contributing to the gradual but inevitable demise of ICT and how non-intrusive board test (NBT) has emerged as a more cost-effective and thorough test technology for the manufacturing floor. Certainly ICT will continue to have its place, albeit current trends indicate it will soon be relegated to special case testing or for testing rudimentary circuit board designs. Simply stated, electronics manufacturers (original equipment manufacturers or original design manufacturers) are finding it increasingly difficult to make a credible business case for ICT, especially when NBT offers better test coverage and a lower cost structure.

Overview

The amount of circuit board test coverage delivered by ICT is being diminished by advancements in technology while the cost-efficiency of ICT is challenged on the basis of straightforward economics. On the technical front, a host of new technologies and circuit board design techniques have conspired against ICT. Specifically, today's sophisticated board design techniques that are rapidly becoming or have already become integral to mainstream electronic design do not provide physical access for probes, which are essential to ICT's bed-of-nail test fixtures. What's more, system and board designers don't want to provide ICT access. At best, designing in tests pads on a circuit board for ICT probes could slow system performance to unacceptably low levels; at worst, the system's ability to function as specified could be placed in jeopardy. Test pads on circuit boards could, in fact, break the system. On the economic front, ICT systems are very expensive to procure, maintain and operate. Complex bed-of-nail test fixtures are time-consuming to produce and costly. Many new product introductions have been delayed because engineers had no other choice but to wait weeks at a time for ICT test fixtures to be produced for each re-spin of a board design.

Inevitably, the industry is turning away from antiquated validation, test and debug technologies that are intrusive, probe-based, hardware-intense and unjustifiably expensive. The alternative is a host of new NBT technologies that provide comparable or better test coverage, are software-driven and are comparatively much less expensive to procure, maintain and operate.

Shrinking ICT Test Coverage

Change is inevitable. Over the years, rapid and dramatic advancements in technology have been typical of the electronics industry. Practically all aspects of the industry have advanced by leaps and bounds. Chip speeds have skyrocketed while advanced chip packages have made physical access to chip pins for test equipment nearly impossible. New circuit board design and fabrication techniques have been developed to take advantage of new chip capabilities. At the same time, the test equipment that verifies the quality, performance and functionality of manufactured circuit boards has attempted to keep pace with advancing requirements and a myriad of new obstacles. Some of the current requirements that are being placed on test

equipment are eliminating or significantly diminishing the role of intrusive legacy test technologies like in-circuit test (ICT). Fortunately, non-intrusive, software-driven board test technologies are filling this void by delivering the test coverage that ICT has lost. ICT test coverage is shrinking for a variety of technical reasons.

Circuit Density

Circuit density and the availability of physical access for test equipment have an inverse relationship to each other. Increasing circuit density at the chip and board levels has decreased the availability of physical access through test pads, which are the lifeblood of ICT bed-of-nail fixtures. For example, the geometry of chips in ball grid array (BGA) packaging has continued to shrink. Recently, it dropped from .4 mm ball pitch (center-to-center spacing) to .3 mm. The effect that this almost doubling of circuit density has had on the availability of physical access for ICT test probes is significant. With a .4 mm ball pitch, there is enough room for a via to be routed through the circuit board and connected to the chip by way of a high-density interconnect (HDI). But with fine pitch .3 mm BGAs there is not enough room on the board for a via except directly into a ball or pad on the device. (Figure 1)

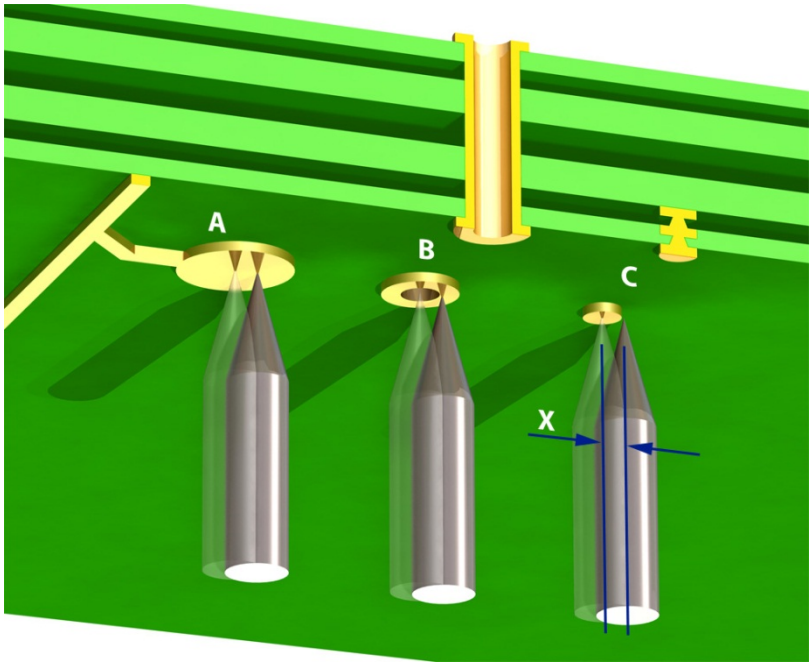


Figure 1: Increasing circuit density – *As circuit density has increased, designers have reduced or eliminated the area previously dedicated to test access. Probing accuracy improvements haven't kept pace with the shrinking geometry of test pads.*

To accommodate smaller device geometries and greater circuit densities, new circuit board manufacturing methods like micro-vias for HDI and others have been adopted – not by choice, but by necessity. These board design and assembly methods have made physical access for ICT even more difficult to come by. For example, the micro-vias that make up HDIs are typically laser-drilled. As such, they are much too small to provide access for an ICT probe by way of a test pad.

Probe-Induced Strain

In general, strain placed on a board by ICT probes can create defects in solder joints anywhere on the board. As a result, the amount of strain, or 'flexture,' that an ICT bed-of-nails fixture places on a board must be monitored very closely (Figure 2). Still, in many cases ICT-induced strain can be much greater than any strain that will ever be placed on a circuit board when it is installed in an operational system. As a result, the strain produced during ICT test, which is intended to verify the quality of the manufactured board, can actually produce on a board many of the defects it is trying to detect.

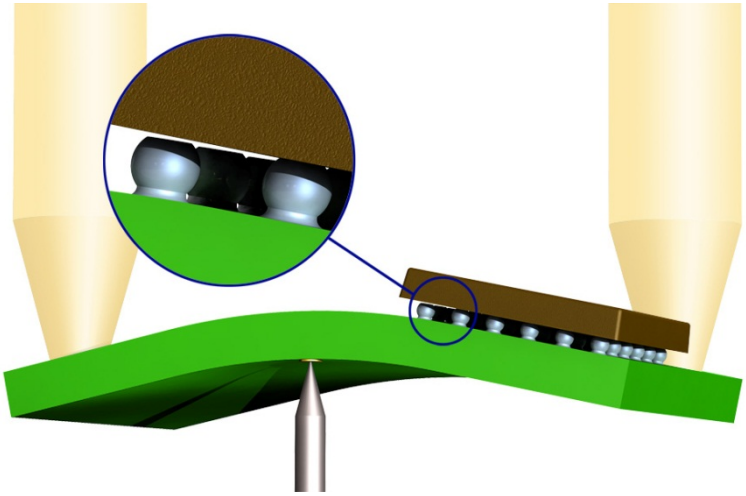


Figure 2: Flexture – *The strain resulting from the force of ICT probes can actually cause the structural failures they are trying to detect.*

In addition, press fit pins (Figure 3), which are typically employed on connectors, can be problematic for ICT testing. Press fit pins are not solid metal. They are formed in a shape that compresses as the pin is inserted into a circuit board. The counterforce exerted by the pin and which results from inserting it into the board, holds the pin in place. If an ICT test probe is placed on a press fit pin for test purposes, the probe exerts force in the opposite direction from which the pin was inserted. This could loosen or completely dislodge the pin from the circuit board. One major computer manufacturer reported system crashes resulting from error over-runs or double-bit memory errors. Technicians at the company found that re-seating the dual inline memory modules (DIMMS), which had somehow become loose in the connectors, would solve the problem, at least temporarily.

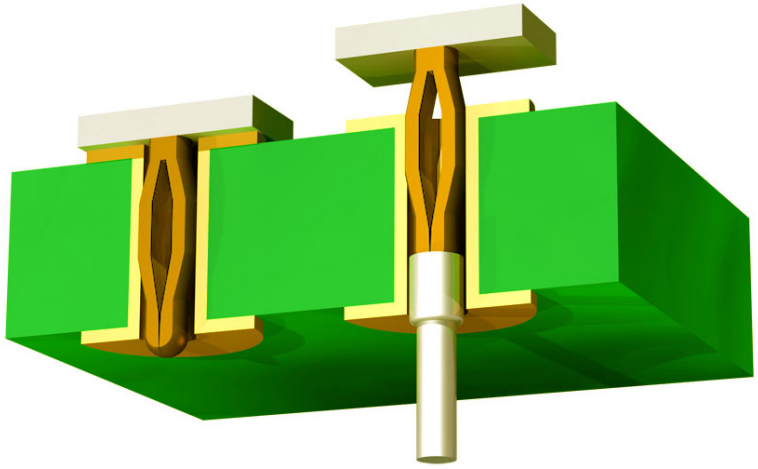


Figure 3: Press fit pins – *Press fit pins can be dislodged when tested on an ICT system.*

Circuit Speed

The speed that data travels across chip-to-chip interconnects on circuit boards is constantly increasing to keep up with the increasing performance of the chips themselves and to support the huge data throughput rates that are typical of today's networked systems as shown in Table 1.

Table 1: Escalating speeds on several popular high-speed buses

Bus	Speed
DDR	
DDR1	400 MT/s
DDR2	1.066 GT/s
DDR3	2.133 GT/s
DDR4	4.266 GT/s
PCIe	
PCIe 1	2.5 GT/s
PCIe 2	5 GT/s
PCIe 3	8 GT/s
PCIe 4 (2014/2015)	16 GT/s
USB	
USB 1-Low	1.5 Mb/s
USB 1-Full	12 Mb/s
USB 2	480 Mb/s
USB 3	5 Gb/s
Serial ATA (SATA)	
SATA 1	1.5 Gb/s
SATA 2	3 Gb/s
SATA 3	6 Gb/s
Direct Media Interface (DMI)	
DMI 1 (2004)	10 Gb/s
DMI 2 (2011)	20 Gb/s

As the speed of data buses on circuit boards approaches 5 gigabits per second (Gbps), the routes become very sensitive to capacitive coupling, electromagnetic interference (EMI) and electromagnetic compliance (EMC) concerns. In fact, placing any sort of test pad on one of these high-speed buses could disrupt signaling to the point where system performance is jeopardized. Bringing an internal route to a surface layer in order to place a test pad on it would create an un-terminated stub on the route and this would induce reflection and ringing. For these and other reasons, many reference designs provided and recommended by the suppliers of high-speed chips such as Intel® and others strictly prohibit the placement of test pads on high-speed buses. As a result, circuit board design techniques have adapted to these new requirements by

eliminating test pads and other means of access for physical probes, including those that comprise ICT bed-of-nail fixtures.

Moreover, many circuit board designs today limit or totally restrict the routes that are placed on the surface layer of a circuit board. At the very least, the most critical routes only come to the surface layer to connect to a device pin (Figure 4). Sometimes a circuit board's surface will function as a power or ground plane to better cope with EMI issues. So, for example, the top and bottom layers of a board may be coated with metal to better control EMI. When this is the case, all of the board's routes are placed on internal layers and only come to the surface layer when they connect to a device pin.

The EMI concerns of board and system designers have also limited the adoption of the bead probe method on ICT. In order to deploy bead probe on an ICT system, the routes must be exposed on the surface layer so they can be probed. Unfortunately, surface routes will radiate significant EMI and this has become increasingly unacceptable.

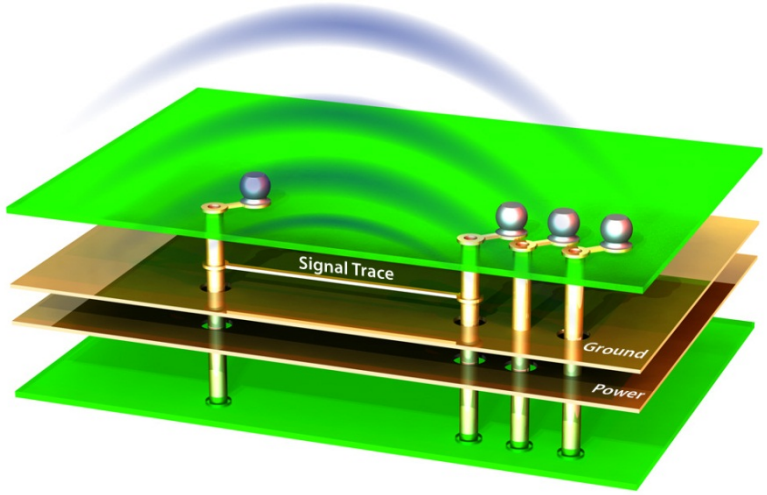


Figure 4: Electromagnetic interference (EMI) – *Many circuit board designs today place the traces on internal layers to reduce EMI emanating from surface layer traces and test pads.*

In addition, vias must frequently be back drilled so they can be properly terminated to ensure the integrity of the signal. A via that is routed from a chip on one side of a board to a test pad on the other side would constitute an un-terminated stub, causing signal reflections and ringing on the

line. Back drilling involves drilling out the via to eliminate the stub. Doing so eliminates the possibility that a test pad for ICT testing could be placed on the via on the opposite surface of the board.

Blind and buried vias are often designed into circuit boards in an attempt to limit the number of layers that make up the board. In both cases, access for external probing is denied to these types of vias. A blind via is routed from one surface layer to an internal layer, but not to the other surface layer of the board. A buried via is totally buried within a board. Buried vias, which are considered a subset of blind vias, may interconnect two internal nodes on internal layers of a board and never come to a surface layer (Figure 5). By not routing a via through all the layers of a board, more area remains available for routing signals on the several or many layers that can comprise contemporary circuit boards. In some cases, this internal routing could reduce the need for additional layers. Unfortunately, physical access to blind vias is problematic and to buried vias impossible. As a result, blind and buried vias can severely reduce the test coverage provided by ICT testers.

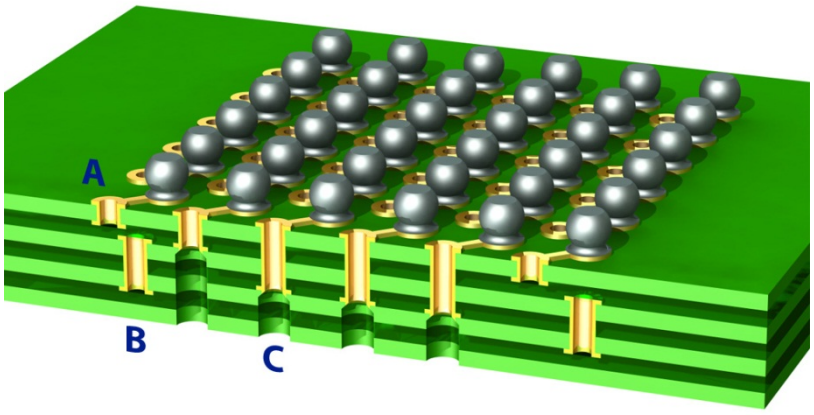


Figure 5: Via stubs – *Illustrated in this figure are a blind via (A), a buried via (B) and a via that has been back drilled (C) to reduce EMI issues.*

The Non-Intrusive Alternative

As a software-based technology, NBT is not subject to the limitations or deficiencies that hardware-based test technologies like ICT must cope with. A simple connector on the printed circuit board typically links the board to an NBT test station, which is usually a personal computer (PC) or laptop running test software and other tools. In many cases, NBT test technologies make use of the JTAG port (that is, the IEEE 1149.1 Boundary-Scan Standard's Test Access Port) to access the circuit board and the chips on it. In addition, NBT will utilize embedded instrumentation intellectual property (IP) in chips and on circuit boards. Several different test and validation technologies can be configured in an NBT test strategy. This increases the effectiveness of NBT since the various test technologies complement each other. Some of the test technologies that can be included in an NBT test strategy are high-speed I/O validation using instruments embedded in chips (HSIO® for Intel Architecture is an example), boundary-scan test (BST), processor-controlled test (PCT), FPGA-controlled test (FCT) and others.

Essentially, an NBT test system will apply test vectors or algorithms that are internal to the circuit board. These tests exercise the board, the data buses on the board and the chips that populate it. Results are observed by the NBT test system and any failures are noted and reported. To facilitate rapid repair or precise re-designs, extensive diagnostic capabilities pinpoint the locations of most failures.

Because a software-driven NBT test strategy is unfettered by the physical test probes of ICT and it is able to draw on the strengths of several test technologies, it can incorporate the three critical types of testing: structural, functional and performance testing. Moreover, NBT's test technologies can be implemented on one test platform, simplifying NBT's deployment on the manufacturing floor.

The NBT test technologies – BST, HSIO validation, PCT and FCT – are capable of validating, testing and debugging a fault spectrum much larger than ICT's. For example, unlike ICT, which tests circuit boards at the speed of the ICT tester and not the speed of the circuit board or the devices on the board, an HSIO toolkit can validate the full-speed operational performance of I/O

and memory buses. For example, a Bit Error Rate Testing (BERT) HSIO tools will uncover which lanes on a high-speed serial interface are malfunctioning while margining tools can plot an eye diagram to determine the signal integrity on the individual lanes which make up a high-speed bus.

PCT is another at-speed test method. By taking advantage of a processor's debug port, PCT is able to access the rest of the board to perform debug, device initialization, at-speed functional test with structural diagnostics and other test functionalities.

FCT, which temporarily inserts test and measurement instruments into an on-board FPGA, is also able to assert test algorithms at the operational speeds of the board. The nature of any particular FCT test suite will depend on the instruments inserted into the FPGA and this will be determined by the objectives of the test strategy for that particular circuit board. For example, if the memory on a certain circuit board did not have adequate test coverage, the test team could deploy FCT tools to test the design's memory buses and chips before any functional firmware had been integrated into the hardware. An FCT memory built-in self test (MBIST) embedded instrument could apply sequences of reads and writes to memory locations coupled with specific data patterns and addressing schemes. For example, FCT's MBIST instrument might apply at-speed back-to-back reads between two addresses to determine whether the address decode is capable of resolving at the rated operating speed.

Economically Speaking

Two of the most basic measures of a business' cost structure are fixed costs and variable costs. On both of these metrics, ICT is a very expensive test technology for an electronics manufacturer, especially when compared to a less costly NBT strategy that could provide better test coverage.

An advanced ICT system can come with a starting price tag in excess of $250,000, although less expensive and less capable ICT systems are certainly available. , A personal computer-based NBT station can be deployed in a manufacturing line for less than $25,000, a tenth of the cost of an advanced ICT system. In addition to the fixed procurement costs of ICT vs. NBT, NBT's

variable costs are far less than those of ICT. Specifically, NBT does not require sophisticated bed-of-nails test fixtures as ICT does. These fixtures are quite expensive to produce and maintain, especially when every design change on a circuit board usually triggers the production of new fixtures.

NBT is able to avoid the ever-escalating costs of intrusive test technologies like ICT because NBT is software driven. As such, NBT is extremely flexible and very adaptable. In particular, NBT can be quite efficient when new product designs are transitioning from development to high-volume manufacturing. During this phase of a product's lifecycle, circuit board designs are still being qualified and numerous design changes are sometimes needed. If ICT were deployed to test prototype versions of a new board design, an ICT test fixture costing tens of thousands of dollars would be needed whenever new prototype circuit boards were produced. Normally, numerous design changes will occur to circuit boards before a product is completely qualified for release to volume manufacturing. When this is the case, the cost of ICT test fixtures can escalate quickly.

Moreover, the complexity of ICT fixtures has increased dramatically in order to keep up with the increasing complexity of circuit boards. Circuit boards with high pin-counts or which are densely populated require very expensive ICT fixtures. The very high costs of a test fixture make ICT a poor fit for manufacturing lines where a high variety of products are manufactured in low volumes.

In contrast, NBT is not constrained by test fixtures. A design change on a circuit board might trigger a software change in an NBT test program or the recompilation of the board's NBT test suite, but expensive hardware re-spins of test fixtures are avoided entirely.

Once Intrusive, Always Intrusive

Perhaps recognizing the limitations of intrusive test technologies, suppliers of ICT testers have incorporated some form of BST (boundary-scan test) into their products. Unfortunately, an ICT test system is not an effective platform for BST when compared with standalone BST systems such as ASSET's ScanWorks platform for embedded instruments. Executing on an ICT tester

saddles BST with the limitations of ICT. In contrast, standalone boundary-scan systems avoid these limitations by executing from a standard personal computer.

Examples of how ICT limits the effectiveness of BST are many. Most ICT testers have a maximum test clock (TCK) of one or two MHz, which is far too slow for testing high-speed memories like DDR2/3. Moreover, most installed ICT testers do not currently support the boundary-scan standard for high-speed AC-coupled nets, IEEE 1149.6. This precludes testing high-speed buses like PCI Express™, XAUI and SATA with ICT. In addition, running BST on an ICT will require isolation of the main probes in the test fixture to reduce noise from those probes and to make the test repeatable and deterministic. Accommodating this restriction often necessitates a dual-stage ICT fixture, which drives up the cost-of-test significantly as well as operational complexity.

Some ICT testers support a boundary-scan derivative technology, which is referred to by several proprietary names such as Powered Opens testing, CoverExtend, ToggleScan or Digital Framescan. These techniques use boundary-scan signaling and a capacitive sensing plate placed in contact with a lead frame or connector to test non-boundary-scan devices. Again, this technique is also limited by ICT's slow test clock, its non-support of high-speed AC-coupled boundary scan (IEEE 1149.6) and other deficiencies. Some ICT systems claim they can extend boundary-scan test coverage to non-boundary-scan devices by running functional test patterns through data converters, by reading clock times or sensor outputs, and other such test vectors. Developing these types of tests is extremely difficult, requiring a great deal of manual labor when compared to benchtop boundary-scan test systems like ScanWorks, which support easy-to-use programming languages such as Tool Command Language (Tcl). In general, ICT systems do not support the range of advanced programming languages that benchtop boundary-scan systems do like Standard Test and Programming Language (STAPL) and others.

Test re-use across a system's entire life cycle is another benefit of benchtop boundary-scan test not found in ICT testers. High-cost ICT testers only make economic sense in a high-volume/low-mix manufacturing environment, but even in this type of application the eroding test coverage of ICT is rendering it less cost-effective all the time. In contrast, a benchtop BST platform such as

ScanWorks can be deployed throughout the life cycle, beginning in design for board bring-up, followed by volume manufacturing, and eventually migrated to debug and repair operations. Boundary-scan tests developed early during the design stage can be re-used until product obsolescence, reducing the total cost-of-test significantly.

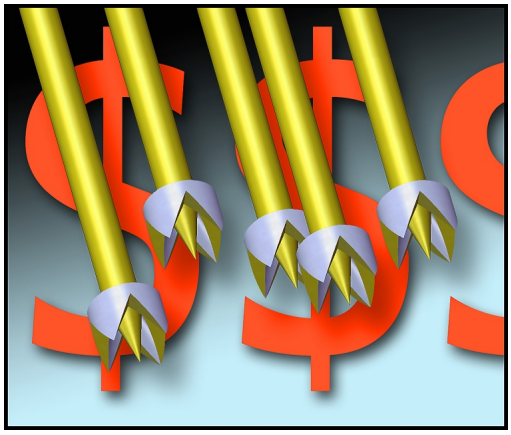
Conclusions

Although intrusive test technologies like in-circuit test (ICT) have been quite effective on the manufacturing floor for many years, recent advancements in basic electronic technologies are disrupting legacy test methods. In just the last five years, the advancements in microprocessors, communications chips, memory and other base technologies have been phenomenal. In reaction to this, circuit board design and assembly techniques have changed dramatically to accommodate increasing processing speeds, greater circuit densities and the high data throughput requirements that are placed on today's systems. As a consequence, the test coverage delivered by legacy intrusive test systems has eroded while their fixed procurement and variable maintenance costs have escalated dramatically.

Fortunately for electronics manufacturers, non-intrusive software-based test technologies have emerged over the last 10 years. By capitalizing on the strength of software – its low procurement cost relative to hardware-intense test systems like ICT, its flexibility, adaptability and agility – these non-intrusive board test (NBT) technologies offer an array of significant solutions today and will continue to do so as electronic technology advances in future.

Learn More

Learn more about NBT and the economic benefits it holds. Register for the white paper, "Economics, Technology Drive Industry to Non-Intrusive Board Test," and you'll find out how NBT can counteract the ever increasing life-cycle costs of ICT and other intrusive test technologies.



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