ASSET INTERTECH

Guidelines for Board Design For Test (DFT) Based on Boundary Scan/JTAG Part 2

Prepared by
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for ASSET InterTech, Inc.

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ABSTRACT:

This document is Part 2 of a 2-part document that contains a series of DFT JTAG Guidelines for boards to be tested primarily through the use of boundary scan or JTAG, based on the IEEE 1149.1-2001 Standard.

About The Author/Presenter

Easy, Affordable, Powerful

Dr R G "Ben" Bennetts is an independent consultant in Design-For-Test (DFT), consulting in product life-cycle DFT strategies, and delivering on-site and open educational courses in DFT technologies.

Previously, he has worked for **LogicVision**, **Synopsys**, **GenRad** and **Cirrus Computers**. Between 1986 and 1993, he was a free-lance consultant and lecturer on Design-for-Test (DFT) topics. During this time, he was a member of **JTAG**, the organization that created the IEEE 1149.1 Boundary-Scan Standard.

He is currently an Advisor to the Board of Directors of **ASSET InterTech**, advising the company on future directions of boundary-scan technology. He is also a core-group member of **IJTAG** and **SJTAG** (and currently the SJTAG Chairman), a co-founder and past Program Chair of the IEEE **Board Test Workshop**, founder of the IEEE **European Board Test Workshop**, and the founder and current Chairman of the IEEE's **BTTAC** organisation.

Ben has published over 100 papers plus three books on test and DFT subjects.

Slide 3
Last revised: March 2006

DFT Guidelines: Part 2

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Boundary-Scan Testability: Board-Level Guidelines (2)

Cluster and In-System Configuration

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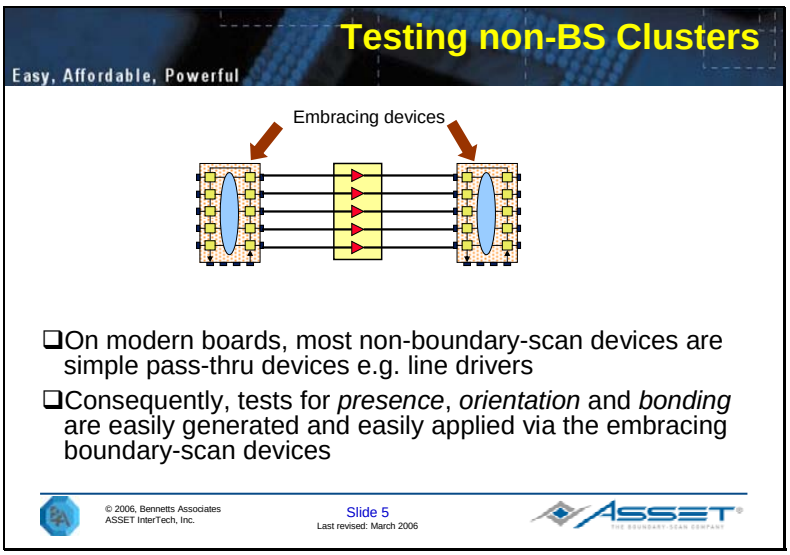
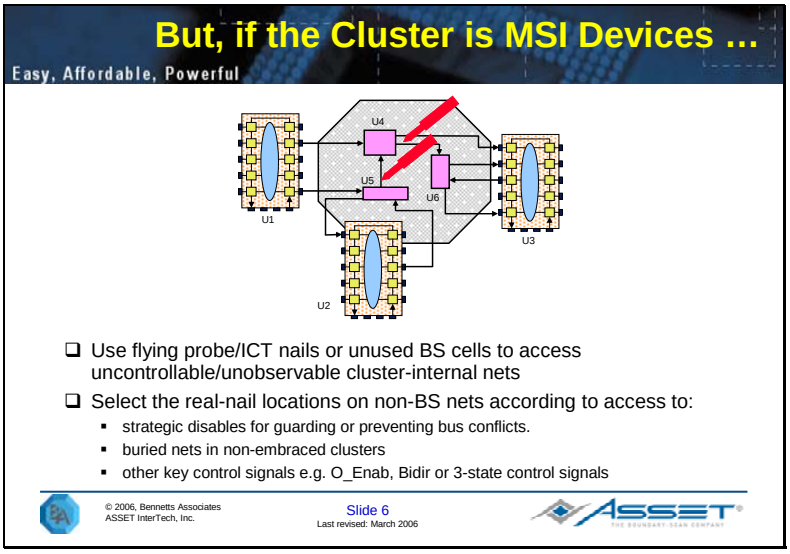
In this section, we will look at DFT JTAG guidelines specific to the design of boards containing non-boundary-scan clusters and the special case of RAM and PLD clusters (in-system configuration).



On most modern boards, the only non-boundary-scan devices are simple line drivers (buffers), with or without inversion, or re-routing devices such as multiplexers. These devices are generally known as “pass thru” devices. It is a simple matter to generate *Presence, Orientation* and *Bonding* tests for such devices and then apply the tests via the embracing JTAG or boundary-scan devices.

But, on older boards, there may be non-boundary-scan MSI devices i.e. devices with more complex functions, such as flip-flops, counters, shift registers, etc. The next slide discusses how to handle such devices.

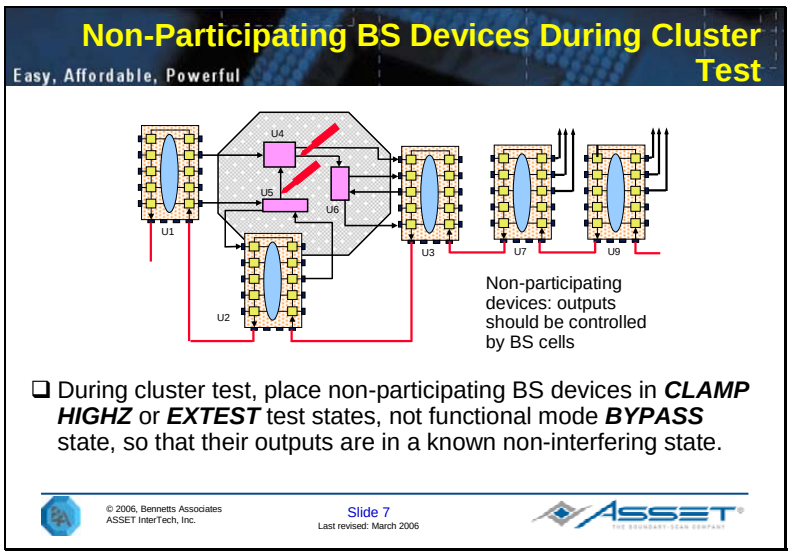


Testing non-BS MSI devices for opens and shorts via a JTAG (boundary-scan) interface (cluster testing) may not achieve 100% stuck-at and 2-net short fault coverage. Patterns for the non-boundary-scan clusters can be taken from the extensive libraries of In-Circuit Testers and validated via a fault simulator.

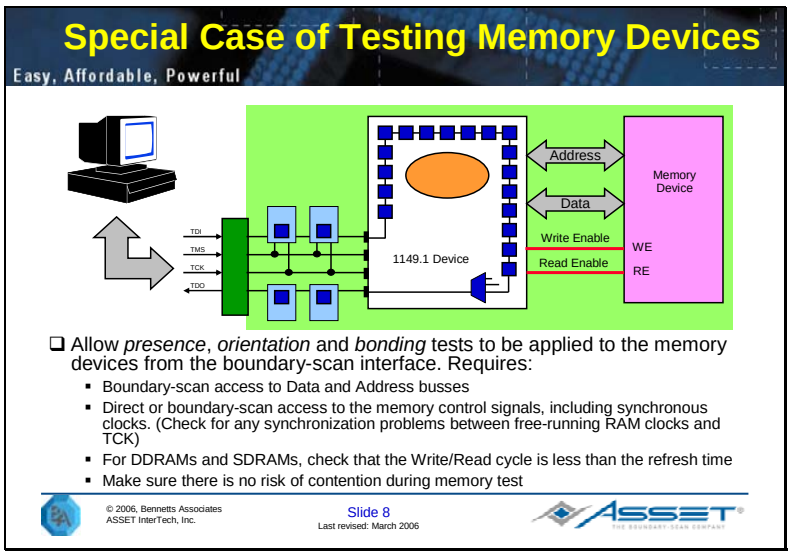
To maximize fault-coverage on non-BS MSI devices, ensure maximum access to their pins either via boundary-scan or JTAG registers or direct from the primary connection to the board, or by using real nails (from a flying probe or bed-of-nails fixture).

If the board is to be tested using a mix of real nails (from a flying probe or bed-of-nail fixture) and virtual nails (from JTAG/boundary-scan cells), choose the selection of the real nail access nets carefully i.e. where they will contribute the most to additional fault coverage – see Part 2 of this series. Some vendors have access-analysis tools to assist in the selection process. Note: the selection process will also impact physical layout, causing certain nets to be brought to the surface of the board for physical probe purpose.

Where possible, provide direct access to key control signals on non-BS devices so that they can easily be configured into the correct state during test. If direct control is not possible, provide indirect control from an unused boundary-scan cell.



Boundary-scan/JTAG devices that do not participate in cluster testing should be placed into known safe states. One way to do this is to hold them in a test state rather than a functional state. The CLAMP, HIGHZ and EXTEST instructions can all be used to achieve this objective.

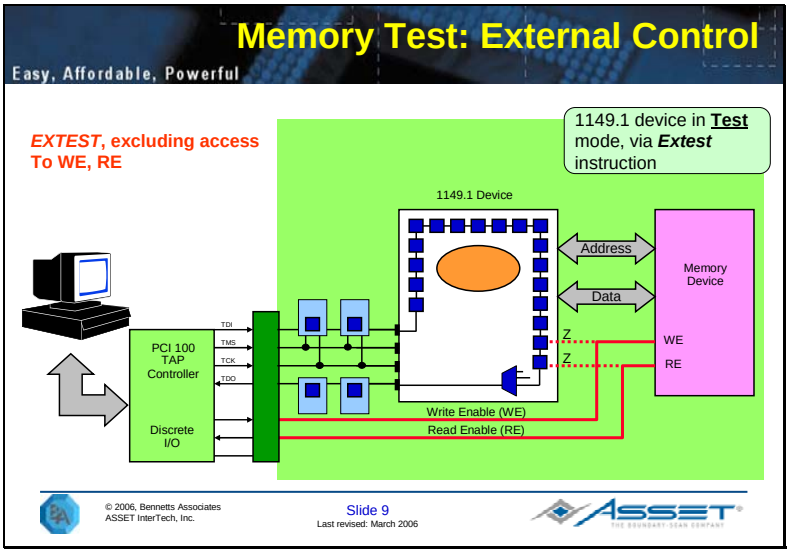


A boundary-scan (JTAG) interface can be used to test the *presence, orientation* and *bonding* of on-board RAM devices. The tests require JTAG (boundary-scan) access to the Data, Address and Control lines of the RAMs. Commercial PC-based test systems support this use of boundary-scan (JTAG) registers.

In the case of RAM devices that are not accessible from JTAG/boundary-scan devices, 1149.1-compliant buffer devices can be used to restore JTAG access. National Semiconductor and Texas Instruments make 1149.1-compliant buffer devices for use on board internal busses e.g. the TI Octal and Widebus™ devices. It is preferable

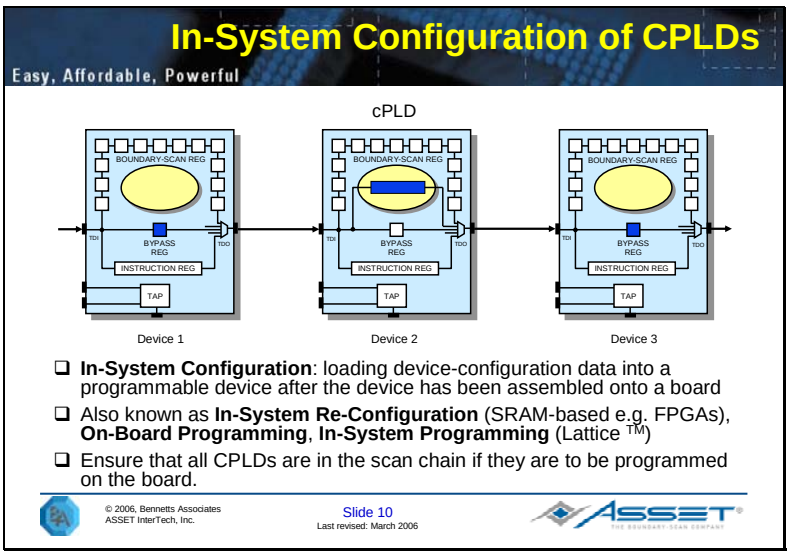
to use these devices for buffering bus signals rather than non-BS buffer devices. In the case of the TI devices, the boundary-scan registers can be set up to become a pseudo-random pattern generator (output scan cells) and CRC data compactor (input scan cells). A typical example of such a device is the SN74LVTH18502A Widebus™ Universal Bus Transceiver.

Details of all these devices can be found on the vendor's web sites – see the "To Probe Further …" slide.



Here we see that the *WE* and *RE* control signals have been brought out to an edge-connector position to allow programmable IO pins (from the tester) to provide the control signals. This considerably reduces the time it takes to check the *presence, orientation* and *bonding* of the memory device.

If you do this, make sure that there is no damage caused by back-driving to the output drivers of the normal source of the control signals. If there is the potential for damage, design the *WE* and *RE* sources to be tristate sources and place in high-Z state during the test mode, as shown.

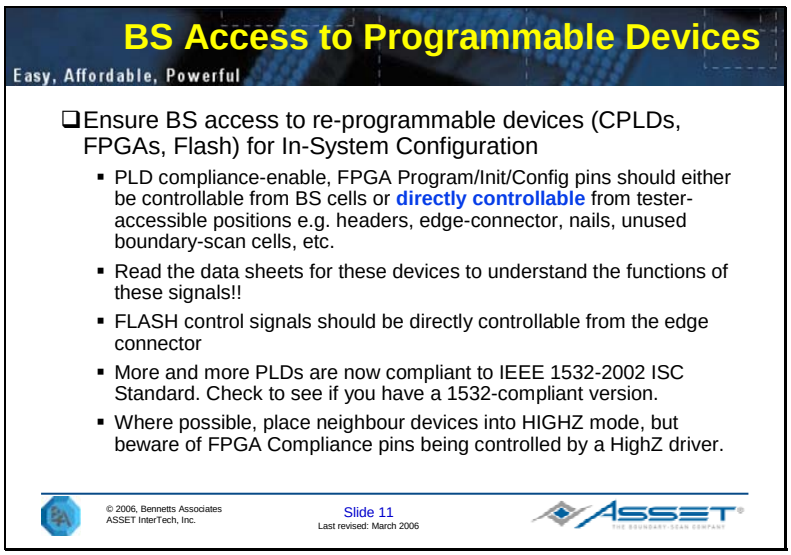


In-System Configuration (ISC), or *In-System Programming* (ISP) as it is often known, has become a major new application of 1149.1 boundary scan or JTAG. Basically, ISC is the ability to load configuration data into a *Complex Programmable Logic Device (CPLD*), *Field-Programmable Gate Array (FPGA)* or even a *Flash* device whilst such devices are mounted on a board.

The benefits of ISC are numerous:

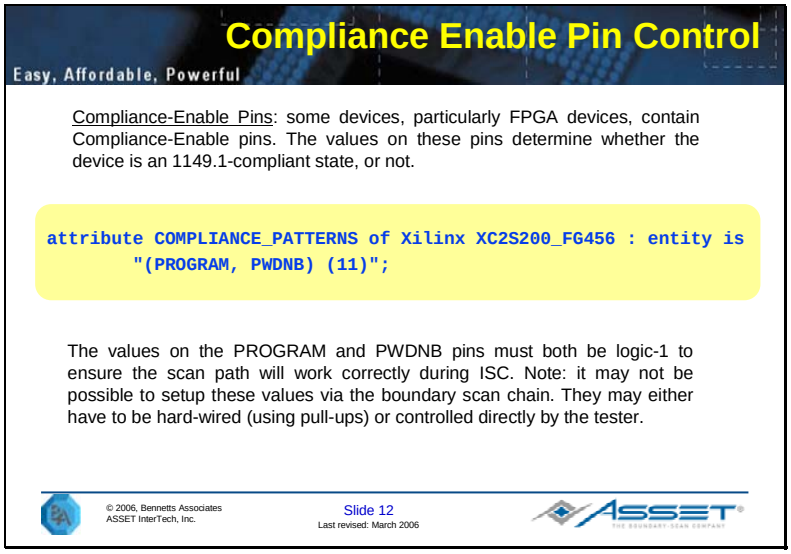
- simplifies inventory management,
- reduces or removes the need for off-line programming stations,
- enables rapid prototype configuration and re-configuration, thereby increasing design flexibility,
- removes the need for on-board sockets which are often a cause of pin damage,
- reduces risk of damage caused by mechanical handling and electro-static discharge leading to improved quality of parts,
- allows just-in-time programming (also known as design for postponement) and last-minute changes e.g. choice of language, personal details (SIMM cards), et cetera
- and allows program upgrades for System and Field-Service debug.

The programming of the CPLD device is carried out via the board-level JTAG (boundary scan) access path – that is, from the edge-connector through surrounding devices to the programmable device. Surrounding JTAG/boundary scan (and non-boundary-scan) devices must be placed in a safe state so as not to interfere with the in-system programming process. Boundary-scan/JTAG devices are first preloaded with safe values (using the PRELOAD instruction) and then placed in Bypass register mode using either the HIGHZ or CLAMP instruction. Placing surrounding JTAG devices in bypass register mode also facilitates rapid access to the programmable device.

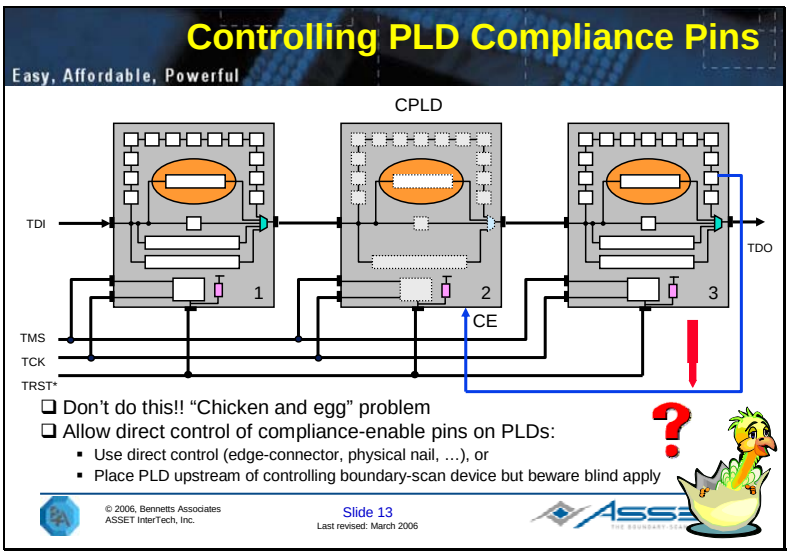


If the board contains programmable devices, such as CPLDs or FPGAs, make sure that the devices can be programmed, and re-programmed, from a boundary-scan/JTAG interface – see next slide. Ideally, such devices should be compliant to the new IEEE 1532 - 2002 In-System Configuration Standard.

All significant control signals that control the operational status of on-board devices must be directly controllable when the board is in test mode. This includes board Power-On Self Test, Boot or Program signals e.g. Power-Down, Init, Reset, PRGM_, BOOT_



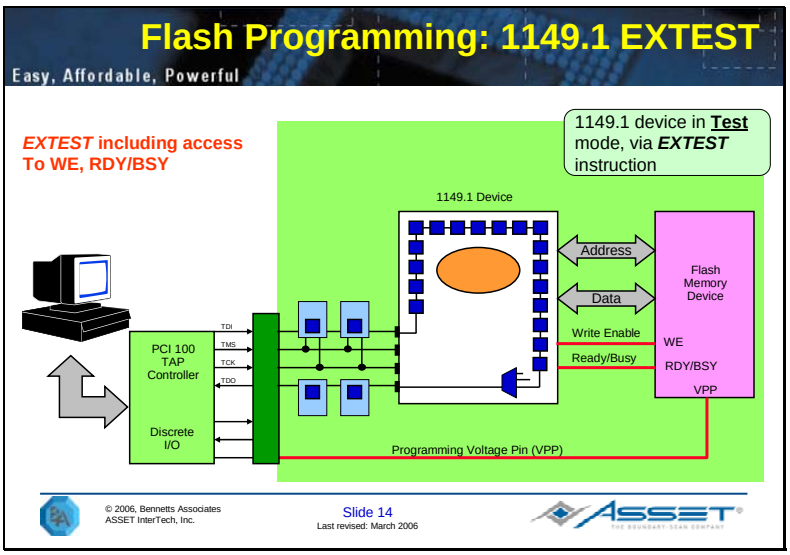
Xilinx xc2s200: an example of a programmable device that has compliance pins to establish the 1149.1 logic. The two pins, PROGRAM and PWDNB, must both be held at logic-1 to establish the boundary-scan logic.



Do not place control of compliance-enable pins downstream of the programmable device. If you do this, the chain cannot be established – a classic chicken and egg problem. One solution is an automatic power-up reset circuit on the board that has control of the compliance-enable pins. Another solution is to place the programmable device downstream of the controlling device. (Note, this will not work if there is a defect that prevents the upstream devices from being correctly chained – see below.)

Better still is to provide independent control of the compliance-enable signal e.g. through a physical nail or external connection: not through an unused boundary-scan cell.

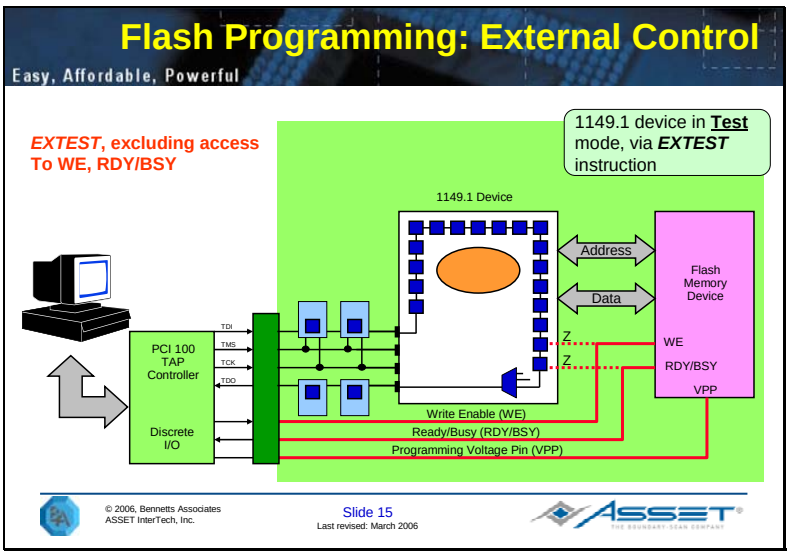
Beware also the "blind apply" e.g. if the scan-chain order of the devices above are switched to 1-to-3-to-2, then it can be argued that the upstream path 1-to-3 can be set up and used to control the compliance-enable pins of the downstream device 2. This is true but assumes that there is no problem with the 1-to-3 path plus there is no problem with unknown values being presented to device 2's compliance-enable pins during the initial set-up phase. It is much better to allow direct control on the compliance-enable pins.



The next few slides takes a closer look at the ability to program flash memory devices through the boundary scan or JTAG registers of adjacent devices connected to the flash *Address* and *Data* pins.

Programming flash devices in this way has become very popular, especially amongst high-volume consumer-product vendors, such as cellular (mobile) telephone manufacturers. The slide above shows a basic system in which all access to the flash is from the boundary-scan (JTAG) register of a single ASIC but it would take too long to change the *Write Enable* values though the boundary scan register. The next slide shows a scheme where access to the flash Write/Read control pins is direct.

Note: Over voltages, such as VPP, can either be supplied direct or can be provided by on-board FETs which are themselves controllable via a boundary-scan or JTAG cell, preferably in the same device that is in EXTEST mode to program the Flash device i.e. the ASIC device above.



Flash Programming Set-up and Constraints

Boundary-scan or JTAG programming device is in EXTEST mode. All other devices are in BYPASS or CLAMP/HIGHZ mode. All output pins must be controlled to safe values.

Flash-programming control signals, such as *Write Enable*, *Ready/Busy* and *Over-Voltage VPP* pins, are controlled directly from the Discrete I/O pins of the interface pod.

For Write: address and data information is shifted into the boundary-scan (JTAG) register (Shift + Update).

For Read: data is shifted back into the boundary-scan (JTAG) register and shifted out (Capture + Shift).

Write/Read time = Function (TCK; length of the boundary-scan (JTAG) register; indirect/direct access to WE, RDY/BSY; availability/non-availability of VPP).

WE signal

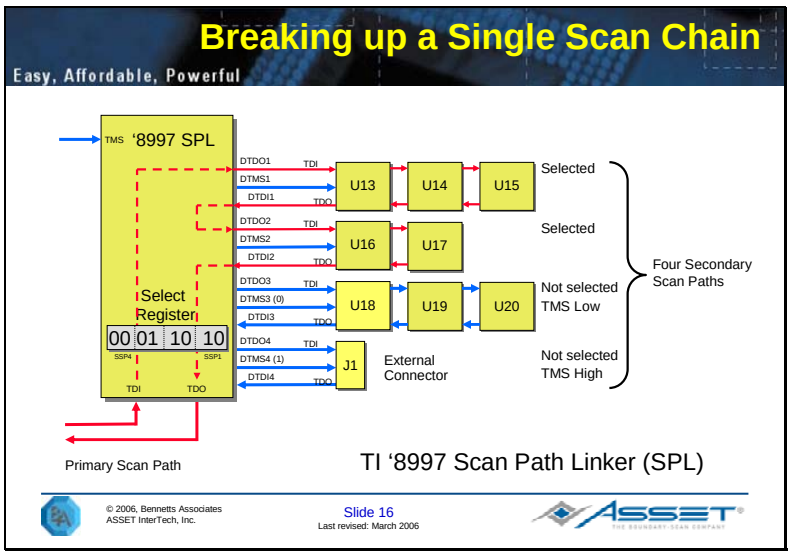
It takes three full scan loads to toggle WE high-low-high while holding the address and data steady. If we control WE outside boundary scan/JTAG, we cut the number of scans by 3: one scan for the address and data, then toggle WE virtually instantaneously.

RDY/BSY signal

Flash programming is a charge-pumping technology, the timing of which is not precise.

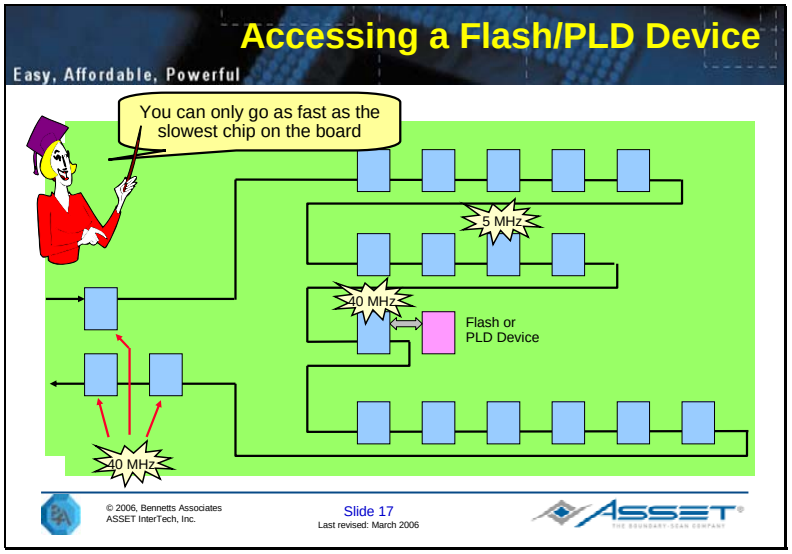
Many Flash devices have a Ready/Busy pin to say when a byte/word has completed being programmed. The alternatives are: interrogate the status byte of the device through JTAG or boundary scan (yet more cycles) or wait the maximum time for which programming is guaranteed to have completed.

Monitoring RDY/BSY directly allows the tester to program the next word/byte immediately the previous one has completed.



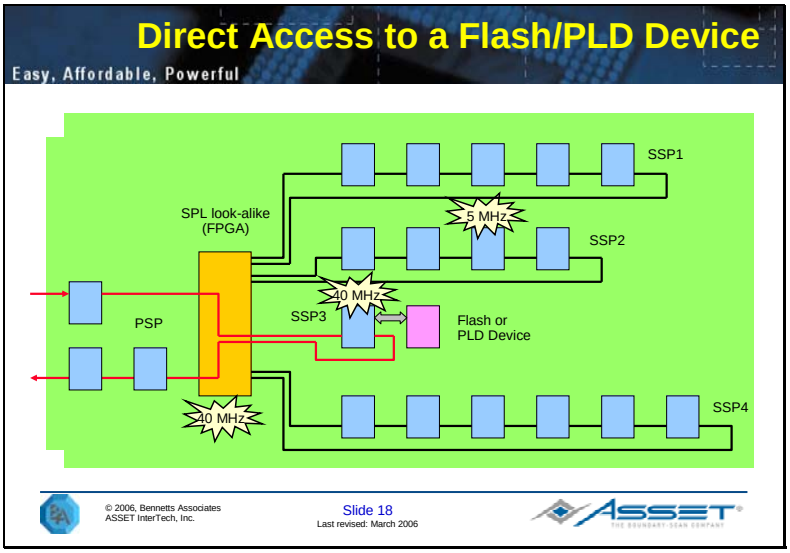
The slide shows a device from Texas Instruments called the '8997 Scan Path Linker (SPL). This device allows dynamic selection of secondary scan chains to be linked in with the primary scan chain. Such a device can be used to select, or otherwise, a subset of a main scan chain for a specific reason e.g. direct access to a flash device for programming purposes.

The Secondary Scan Paths (SSPs) are either included or excluded from the Primary Scan Path based on the configuration loaded into an SPL internal register called the ***Select Register***, selected by the SCANSEL instruction. In the example above, SSP1 and SSP2 are selected and linked together. SSP3 and SSP4 are excluded from the scan chain. The order of the scan chain is Primary TDI to SSP1 to SSP2 back to Primary TDO.



Here we see a Flash (or PLD) device accessible from an ASIC JTAG/boundary-scan device. Let us assume that we wish to program this device at the maximum rated frequency of 40MHz – the max TCK for the ASIC.

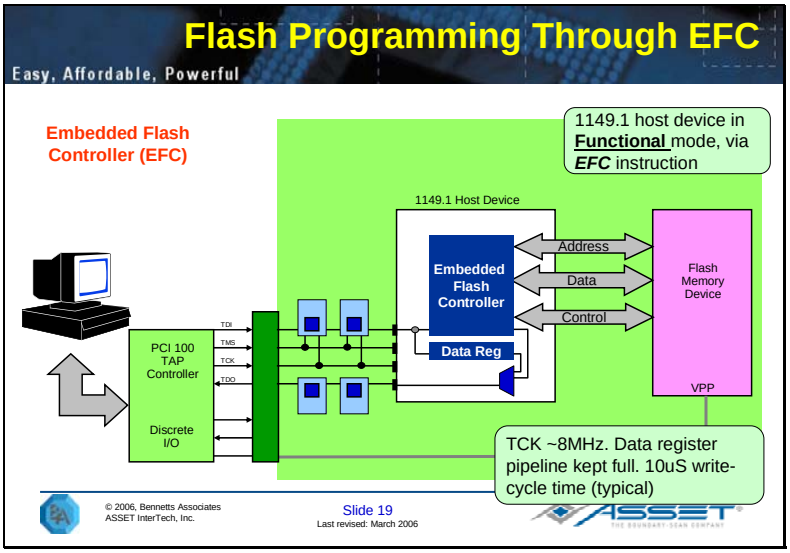
One problem however is that TCK can only be as fast as the slowest device in the chain. If the ASIC can accept a TCK of, say, 40MHz but another device in the chain is only able to run at a TCK of, say, 5MHz, then the maximum speed of the whole active chain is limited to 5MHz. This may produce an unacceptable reduction in the flash programming time.



A solution is to use a 40MHz TCK FPGA programmed to behave like a Texas Instruments '8997 Scan Path Linker (SPL) or National Semiconductors Enhanced ScanBridge device to exclude the slow JTAG/boundary-scan devices in the chain, as shown. The SPL has four secondary scan paths, each individually selected through a special SPL configuration instruction called SCANSEL. The ScanBridge device has three secondary scan ports, again each individually selectable. More information on these devices can be found on the TI and National Semiconductors web sites – see the "To Probe Further…." slide.

Note: a limitation with the TI and National Semiconductor devices is that they work at relatively low maximum TCK frequencies: 20MHz for TI's devices and 25MHz for National's devices. This was why the suggestion above is based on an FPGA look-alike. Another concern is that the TI and National Semiconductor devices are currently 5v devices whereas the boundary-scan or JTAG devices in the chain may be working at somewhat lower supply voltages. The reader should check with the suppliers of these devices to see if lower-voltage devices are available. Alternatively, check the product offerings of Lattice (ispGDX family) or Firecron at www.lattice.com and www.firecron.com

An alternative solution is to use removable/replaceable jumpers to bypass all JTAG or boundary-scan devices in the chain except the Flash or PLD devices – see the emulation slide for an example of the use of jumpers.

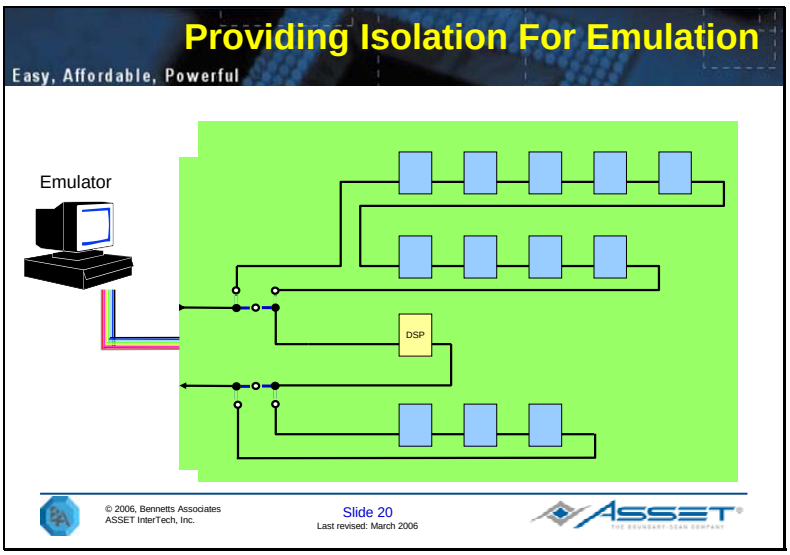


Another Solution: embed an Embedded Flash Controller (EFC) inside a host 1149.1 device, controlled via the device's 1149.1 structures. The host device TDI-TDO provides a path to an internal Data register to load the initial Address and Data. Once initialised, the embedded controller implements the programming procedure for the Flash, including all necessary control signals for Write and Read back. Incrementing the Address can be automatic.

Advantages are:

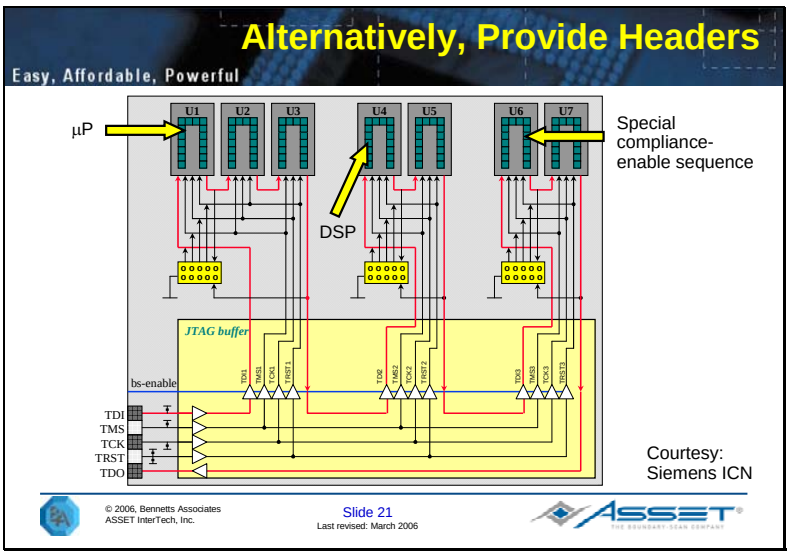
- Flash writing can be at SysClk speeds, not TCK speeds.
- Flash data-bus width can be at full system-bus width
- One controller can service multiple Flash devices
- The host 1149.1 device is in functional (safe) mode, not test mode
- Flash can be re-programmed many times

Note: this technique is similar in concept to LogicVision's 1990's memBIST-XT product, used for testing *presence*, *orientation* and *bonding* of on-board RAMS via a self-test controller embedded in a host ASIC. See also the Philips and Intellitech's papers on this topic (Frans de Jong (Philips) ITC 2001, P17.1 and Clark & Ricchetti (Intellitech), D&TC, May-June 2003, pp.78 – 87). Note also that these proprietary techniques are patented.



Most device emulators (DSP, RISC Emulators) have a problem unless their device is the only device in the scan chain. If these types of devices are placed in a full board-level boundary-scan (JTAG) chain, this can cause emulation-time and device isolation issues during development/software debug. It is better to provide an ability to isolate the emulation device entirely from the rest of the chain and so leave the other devices in functional mode to support the emulation process.

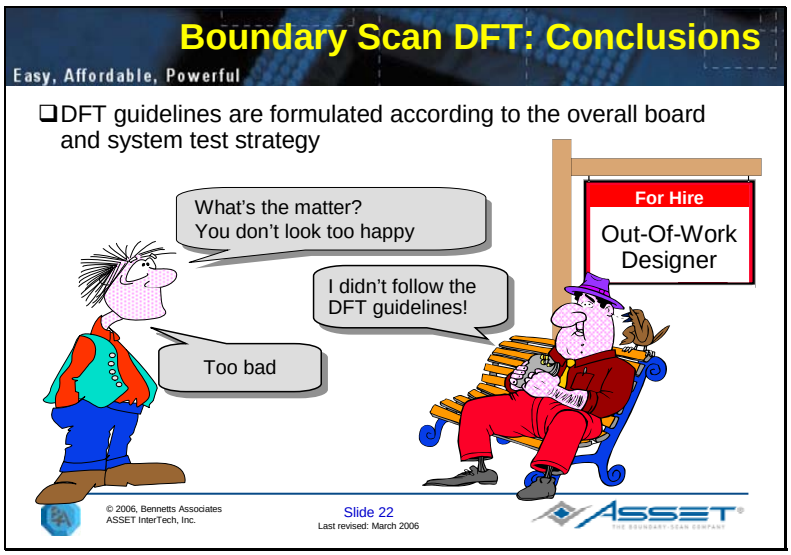
Ways to do this vary from simple jumper selections for TDI/TDO (as shown above) to a connector, all the way up to a multiplexer design selectable from a pin on a header that the emulator/tester plugs into, or a bridge device that supports pass through modes e.g. the Firecron parts.



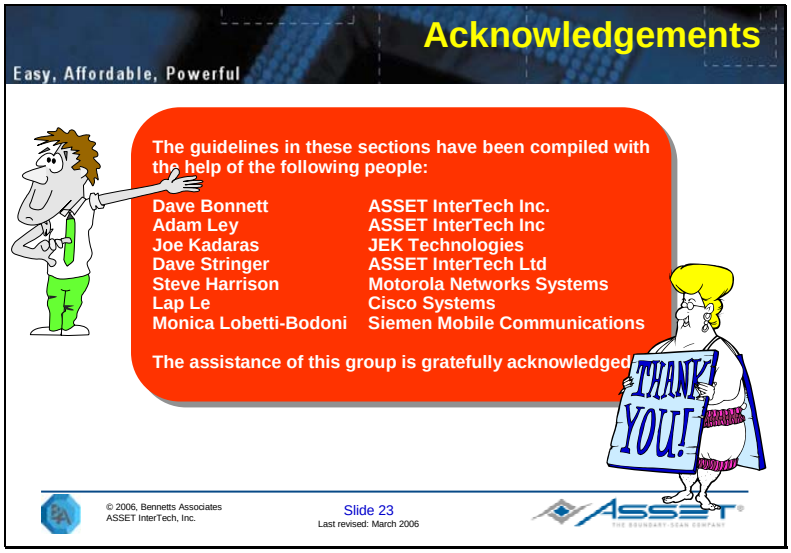
The 1149.1 features may be used also for both the emulation of some devices (DSPs, µControllers, …) and for the data loading of programmable devices. These features are accomplished through the use of proper tools that can be applied through *small connectors* (sometimes called *headers*) to be mounted on the board and connecting the 1149.1 bus where the feature is required. Note that the emulation and the data loading operations are performed in prototype board debug, and typically those small connectors are not mounted during the production release of the board.

Moreover, the connectors are mandatory when the tool cannot handle chains where there are some devices requiring a non-standard compliance/initialisation sequence, or when a simultaneous emulation of various devices working together is required. The proposed architecture (see above) instantiates one of those connectors for each device (or group of devices) making use of the 1149.1 TAP. The architecture results in a partition of the boundary-scan (JTAG) chain in several independent sub-chains: the TAP signals associated with each device/group of devices can be connected/disconnected from the 1149.1 bus through tristate buffers; the tristate buffer mode should be controlled by a signal (*bs-enable*) driven by either the main connector or a dedicated connector. The JTAG (boundary-scan) chain partitioning through tri-state buffers is highly recommended, even where the board designer doesn't require the use of the small connectors, in order to assign the same sub-chain to groups of devices with similar characteristics and requirements (e.g., a group of DSPs, serial FLASH memories, PLDs, FPGAs, or even a single device with a special compliance enable procedure), with the aim of ensuring a fast and practical debugging and diagnostic during the manufacturing tests.

Figure and text reproduced with courtesy of Siemens ICN.



The effect of not following Board DFT Guidelines!!



To Probe Further …. Board

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- Dave Bonnett, “Design for ISP”, ITC 1999, P. 7.3
- Richter & Münch, “Boundary-scan test triumphs over ground-bounce”, T&M World, Aug/Sept 1997
- Dave Stringer, “Boundary-scan testing with FPGAs”, Application Note, ASSET InterTech. **www.asset-intertech.com**
- Frans de Jong et al., “Testing and programming flash memories …”, ITC01, P17.1
- Clark & Ricchetti (Intellitech), D&TC, May-June 2003, pp.78 – 87
- Alan Albee, “A practical guide to combining ICT and Boundary-Scan testing”, ITC01, P 17.3
- Rick Nelson, “PCB test: nails or TAP?”, T&M World, Sept, 2002, pp. 17 – 24
- Bill Eklow et al., “Unsafe board states during PC-based boundary-scan test”, ITC 2001, P. 22.3
- James Stanbridge, “Suggested design provisions for boundary scan test”, Electronic Product Design, Jan, 2001 (See also Board DFT Guidelines, available from JTAG Technologies)

To Probe Further… Web Sites

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- Texas Instruments: **www.ti.com/sc/docs/products/logic**
- National Semiconductor: **www.national.com/appinfo/scan**
- Lattice: **www.lattice.com**
- Firecron: **www.firecron.com**
- Intellitech: **www.intellitech.com**
- BSDL verification service: **www.asset-intertech.com/edft_bsdl_valid.html**
- DFT Guidelines: **www.asset-intertech.com**