ScanWorks®
Platform for Embedded Instruments

2-Day ScanWorks® FPGA-Controlled Test Workshop Details

Class Administration Plan

- Class starts at 8:00 a.m. and ends at 5:00 p.m. each day
- Lunch is 60 minutes
- 2 breaks in the morning and 2 breaks in the afternoon

Section 1: Introduction

Course Logistics
ScanWorks Hardware
ScanWorks Software
Technical Support
FPGA-Controlled Test 101
DFT Guidelines for FPGA-Controlled Test

Section 2: Introduction to a Training Board

Section 3: Overview of the FPGA-Controlled Test Development Process

Embedded Tester Generator
ScanWorks Projects and Designs
ScanWorks FCT actions

Section 4: Getting Started

Overview of ETG
Importing IP into ETG
Exercise 1 – Importing IP into ETG

Section 5: Working with the Frequency Measure IP in ETG

Setting constraints
Pin-mapping the IP
Synthesizing the IP
Overview of exported data from the ETG
Exercise 2 – Working with the Frequency Measure IP in ETG

Section 6: Create a ScanWorks project and design for XEM6002

Create a project and design for the XEM6002
Add ICL to the design description
Create a SPV action to verify the scan chain
Create an SVF action to configure FPGA with Frequency Measure IP
Exercise 3 – Create a design, SPV, and SVF action and apply

Section 7: Create and Run a Frequency Measure based action

Select the FPGA
Select the Instrument
Select Operations and Run
Exercise 4 – Create and Run a Frequency Measure based action

Section 8: Working with the SPI Flash IP in ETG

Setting constraints
Pin-mapping the IP
Synthesizing the IP
Overview of exported data from the ETG
Exercise 5 – Working with the SPI Flash IP in ETG

Section 9: Working with the SPI Flash IP in ScanWorks

Create and Run an SVF action to configure FPGA with SPI Flash IP
Create a SPI Flash IP action
Import pin-map, image file
Define Constraints
Build and Run a SPI Flash IP action
Exercise 6 – Working with the SPI Flash IP in ScanWorks

Section 10: Working with the SPI Master IP in ETG

Setting constraints
Pin-mapping the IP
Synthesizing the IP
Overview of exported data from the ETG
Exercise 7 – Working with the SPI Master IP in ETG

Section 11: Working with the SPI Master IP in ScanWorks

Create and Run an SVF action to configure FPGA with SPI Master IP
Create a SPI Master IP action
Select the FPGA
Select the Instrument
Select Operations and Run
Exercise 8 – Working with the SPI Master IP in ScanWorks

Section 12: Working with Multiple IP's in ETG (Frequency Measure IP, SPI Flash IP, and

SPI Master IP in one FPGA configuration)
Setting constraints
Pin-mapping the IP's
Synthesizing the IP's
Overview of exported data from the ETG
Exercise 9 – Working with Multiple IP's in ETG

Section 13: Working with the Multiple IP's in ScanWorks

Create and Run an SVF action to configure FPGA with Multiple IP
Create actions for each IP (repetition of the above)
Run the actions for each IP (repetition of the above)
Exercise 10 – Working with Multiple IP's in ETG

Section 14: Summary and evaluation