

PRODUCT
BRIEF

ScanWorks® Processor-based Functional Test for DDR Supports Xilinx Zynq Families

Key Benefits:

- Firmware IP ready to run on custom circuit boards with no modifications.
- Supports testing of DDR2, DDR3, DDR4, and LPDDR
- Memory Test Include: Walking 0's and 1's, Address Line Test, Data bus Noise Test, Memory Cell Test, Marching Address test, Burst Transfer Test, Simultaneous Switching Output Test, and Performance Tests
- Slash DDR configuration, tuning and testing efforts
- Excellent solution for new boards with no software, or boards that will not boot

Key Features:

- Testing a SoC device speeds. Captures escapes missed by static testing.
- ScanWorks test action compliant
- Supplied Configuration files for popular development platforms
- Bare-metal application that requires no other software, operating system, or boot loader

Overview

ASSET's ScanWorks® Processor-based Functional Test for DDR (PFTDDR) supports Xilinx's All Programmable SoC portfolio. The Xilinx Zynq families integrate the software programmability of a processor with the hardware programmability of an FPGA, providing you with unrivaled levels of system performance, flexibility, and scalability.

The ASSET ScanWorks PFTDDR provides DDR configuration, tuning and testing via target resident IP. Getting DDR configuration and tuning correct are key elements required for designers to meet the design performance goals. Additionally, PFTDDR provides new functional test IP integrated with the best-in-class ScanWorks test platform. PFTDDR provides high test coverage for all memory devices with at-speed functionality. Combining PFTDDR with ScanWorks PFT delivers greater test coverage to meet design quality requirements of today's high speed designs. ScanWorks tools are designed to maximize development efficiency and simplify the test life-cycle.

PFTDDR uses a target agent (Figure 1), to configure the interface between SoC embedded controller and the memory devices. The agents are installed in On-Chip Memory (OCM) and provide task specific actions: configuration, tuning, and testing DDR memories.

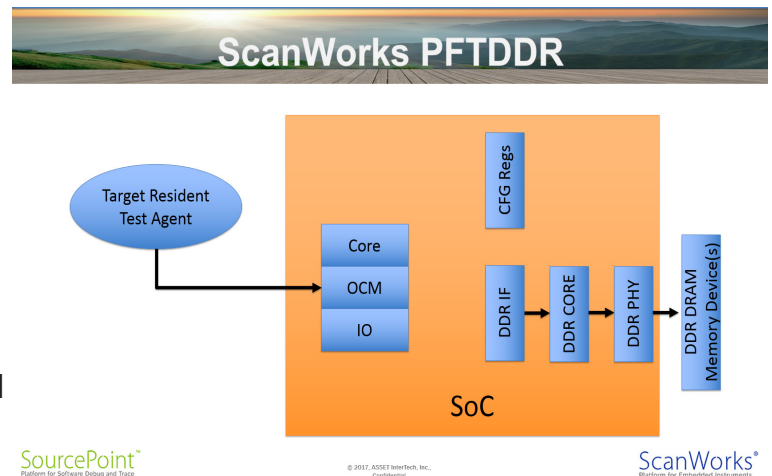


Figure 1. PFTDDR Target Agent with SoC Block Diagram
This tool can slash days off the development efforts required to configure, tune, test and deploy Zynq designs using DDR.

The ScanWorks design environment provides for the control and management of a project resources. Once the resources are configured, the action development is intuitive to create a DDR action. This environment methodology supports rapid transition from development to deployment and ensures consistency regardless of where the project is deployed. Thus eliminating costly communications mistakes.

PFTDDR Development Tool

The ScanWorks PFTDDR Development interface (Figure 2) provides user access to the configuration parameters, configure the desired testing events or task and sequence.

PFTDDR provides comprehensive DDR verification of all memory devices supported by the Xilinx Zynq-7000 SoC family. This IP provides a rich set of memory tests. In addition when used in a develop capacity the IP can perform automated tuning for maximum performance for the specific design.

Starting from scratch can be daunting, however shipped with the product are example board configuration files that support the most popular development platforms from Xilinx and their third party partners. It then becomes a simple matter of connecting the ScanWorks hardware controller to the UUT and launch the ScanWorks application.

ScanWorks PFTDDR can be used in several configuration: stand alone, with ScanWorks PFT, with ScanWorks PFP, with ScanWorks BST or any combination of tools. This flexibility allows the designer and test development teams to maximize efficiency and board test coverage.

ScanWorks Platform for Embedded Instruments

ScanWorks Platform for Embedded Instruments is a seamless software environment to access, run and collect data from any instrument in your chips, circuit boards or systems. The ScanWorks Platform includes products for Boundary-Scan Test (BST), Processor-based Fast Programming (PFP), Processor-based Functional Test(PFT), Processor-based Functional Test for DDR (PFTDDR), Processor-Controlled Test (PCT), FPGA-based Fast Programming (FFP), FPGA-Controlled Test (FCT) and IJTAG test.

ASSET Contacts:

Please contact your ScanWorks sales representative for more information.

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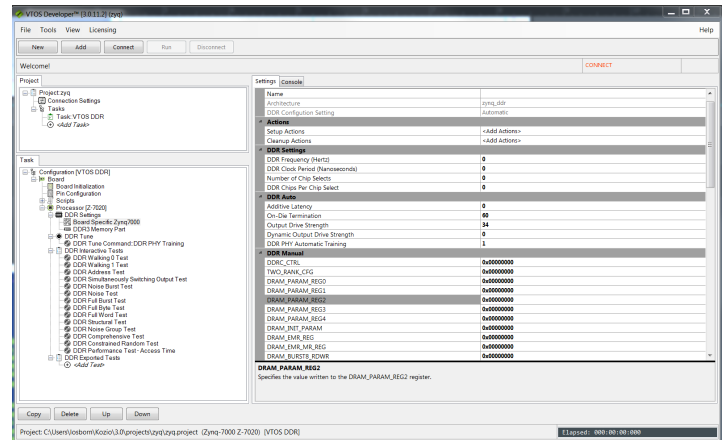


Figure 2. PFT DDR Development