ScanWorks®
Platform for Embedded Instruments

Frequency Measure IP (FM IP) - FPGA-Controlled Test Instrument

Fact Sheet

Introduction

The Frequency Measure IP (FM IP) is an easy-to-use instrument providing verification of system clocks in a board test FPGA environment. The FM IP is used within the ScanWorks® FPGA-Controlled Test (FCT) Development software. When you select and configure the FM IP instrument(s), ScanWorks automatically connects it with other instruments of your choice and turns them into a cohesive, on-chip tester architecture.

The FM IP is included with the FCT Development software. For more information about FCT and other FPGA Instrument IPs from ASSET: visit our website at: https://www.asset-intertech.com/products/fpga-controlled-test.

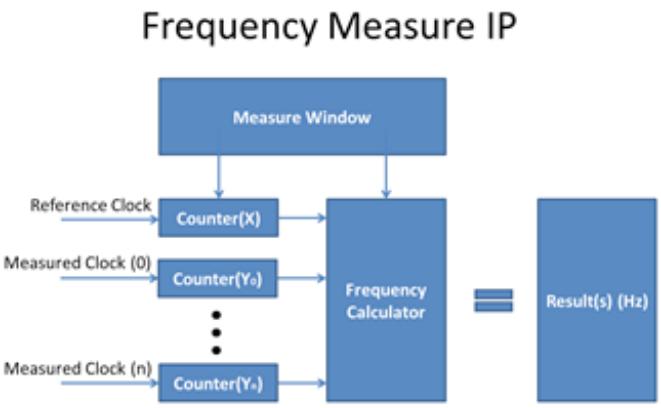

Figure 1

Functional Description

The FM IP uses event counters to accumulate the number of clock events during an adjustable measurement window and calculates the frequency of the measured clock signal, see Figure 1. The FM IP is easily adjusted by setting programmable parameters, including number of measured clocks, the measurement window, and the counter width.

The FM IP includes a number of built-in error detection functions such as counter wrap around, watchdog, status checks, and stuck-at fault detection. The accuracy of the measurement depends on the speed of the reference clock, speed of measured clock, and the measurement window.

The IJTAG IEEE 1687 supported Instrument Connectivity Language (ICL) and Procedural Description Language (PDL) describes the access to the IP, and provides a versatile debug and fault detection environment. High level user accessible functions in the IP are described as procedures in the supplied PDL, accessible from the ScanWorks action interface.

Embedded Tester Generator Configurable Parameters

The Embedded Tester Generator (ETG) software will automatically wrap an IJTAG IEEE 1687 network around the IP and guide you in the parameter setting, pin mapping, and synthesis processes. The following parameters can be set when synthesizing the IP into an FPGA.

Key Benefits:

- Functional verification of system clocks without the use of expensive logic analyzers or oscilloscope
- Eliminates need for signal-distorting test points for system clocks
- Accurate frequency measurement of system clocks
- Can be combined with other structural and functional test as a part of the overall test sequence

Key Features:

- Event counters accumulate number of clock events
- Adjustable measurement window
- Programmable parameters
- Built-in error detection functions
- TCK is used as the reference clock

Limitations:

- The Frequency Measure IP requires a free-running TCK source, therefore it is NOT supported with ASSET's USB-100 pod.

Frequency Measure IP (FM IP) Instrument

Configurable Parameter	
Name	**Description**
DATA_WIDTH	Sets the width of the IP's input data bus. This includes the width of the counter used to count up to the programmed sampling time window.
NUMBER_OF_CLKINPUTS	Sets the number of clock inputs to be measured.
TARGET_CLKCNTR_WIDTH	Sets the width of the IP's output data bus. This includes the width of the counter used to count the transitions of the input clock. TARGET_CLKCNTR_WIDTH must be >= DATA_WIDTH.

The following IO ports can be configured and pin-mapped when synthesizing the IP into an FPGA.

Configurable IO		
Port Name	**IO Type**	**Description**
clkinput [NUMBER_OF_CLKINPUTS -1:0]	Input	Indexed input of clocks to be measured. The width of this bus depends directly on the parameter NUMBER_OF_CLKINPUTS. Duty cycle 50%.

PDL Accessible IP Registers

The following IP registers can be accessed from the PDL (R=Read Only, W=Write Only, RW=Read & Write).

Register Map				
Register Name	**Register Type**	**Register Address**	**Format**	**Description**
IP_ID	R	0x00	Hex - Defaults to 0x00 (width= TARGET_CLKCNTR_WIDTH)	IP ID Register for debug
TEST DATA REGISTER	RW	0x01	Hex - Defaults to 0x00 (during WRITE transactions, WIDTH equals to DATA_WIDTH. During READ transactions, WIDTH equals TARGET_CLKCNT_WIDTH)	Test register for debug
COUNT_LIMIT	W	0x02	Hex - Defaults to 0x00 (width=DATA_WIDTH)	Count limit register address
STATUS	R	0x03	Hex - Defaults to 0x00 (width= TARGET_CLKCNTR_WIDTH)	Three bit register. Bit 2 = TargetFrequency (1 = Target Clock Active, 0 = Target Clock Inactive) Bit 1 = CounterWrapAround Flag (1 = Counter Wrapped Around, 0 = No Counter Wrap-around). Bit 0 = Done Flag)
COUNT_RESULT	R	0x04	Hex - Defaults to 0x00 (width= TARGET_CLKCNTR_WIDTH)	Holds the count of the measured clock.
FREERUNCNTRLIMIT	W	0x05	Hex - Defaults to 0x00 (width=DATA_WIDTH)	Sets a stuck at flag.
CLKSEL	W	0x06	Hex - Defaults to 0x00 (width = log2 (NUMBER_OF_CLKINPUTS))	Selects the measured clock(s).

Below is the list of procedures that are currently available for the FM IP.

PDL Procedures		
Name	**Arguments***	**Description**
MEASURE_CLOCK_INPUT	Yes	Used to measure frequency of clkinput port(s).
* See Detailed Arguments Description Table		

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Detailed Argument Description			
Name	**Arguments**	**Format**	**Argument Description**
MEASURE_CLOCK_INPUT	clksel	Two digit hex. Defaults to 0x00	Selects the measured clock(s).
	measure_window	Two digit hex. Defaults 0x7FF	Sets the size of the measurement window.
	refclk_frequency	Decimal Integer. Defaults to 10000000 (i.e., 10MHz)	User settable to communicate the refclk frequency to be used for clkinput frequency calculations.

ASSET Contacts:

Please contact your ScanWorks sales representative for more information.

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