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Editorial Advisory

Topic: System-level JTAG

Boundary scan (IEEE 1149.1 or simply JTAG) may have begun as a chip- and board-level test technology, but it has evolved over the years to much, much more. Its latest evolution involves system-level applications for test and in-system programming. All indications point to the conclusion that implementing boundary scan from the top down – at the system level – holds even greater promise than the historic applications of the past that proceeded from the bottom chip-level up.

What is system-level JTAG?

System-level JTAG implements a boundary-scan infrastructure across multiple circuit boards, subassemblies and backplanes to encompass the entire system. Once established, this system-wide JTAG infrastructure can be used for a variety of purposes.

Why is system-level JTAG being implemented?

System-level JTAG can reduce an OEM's costs dramatically. For instance, software or firmware upgrades are typically very expensive because they are done manually by an army of field technicians. With system-level JTAG, memory devices, FPGAs or PLDs can be updated remotely with new software without dispatching a single technician.

Another example of system-level JTAG test involves a condition known as "No Fault Found" or "No Trouble Found." A technician is dispatched to return a faulty system to service. The technician replaces one or several circuit boards suspected of causing the problem. Each circuit board removed must be retested and recertified before it can be returned to service. After testing the removed boards, many are labeled "No Fault Found" and are returned to service. The entire process is very costly and, in many cases, unnecessary. System-level JTAG can troubleshoot a system remotely and isolate the problem to a specific board, sometimes correcting a problem without dispatching a technician. The potential for cost savings is huge.

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OEMs are interested in system-level JTAG for a wide variety of purposes. Some field service departments may use it only for troubleshooting. Or, the manufacturing department could use it for final system test. Product engineering could use it to maintain high-availability systems in the field.

Architecturally, what does system-level JTAG look like?

The architecture of system-level boundary scan will depend on the needs of the end user and OEM, although many systems will implement a hierarchical multi-drop boundary scan infrastructure. Each circuit board or subassembly will feature a JTAG gateway device to manage access to scan paths for local boundary scan operations. In many cases, systems involving multiple boards will often deploy a master/slave architecture among the boards that comprise the system. For some systems, a boundary scan kernel may be embedded in-system to perform basic JTAG operations and housekeeping. Other systems will rely exclusively on an external boundary scan system for JTAG processing.

Who is doing system-level JTAG?

Today, system-level boundary scan applications are quickly emerging in applications requiring high availability. These include telecommunications and networking infrastructure systems, aerospace and defense systems, and others. Tomorrow, the benefits of system-level JTAG will find their way into a wide range of system types in many different market segments.

What is ASSET doing with regards to system-level JTAG?

ASSET's ScanWorks boundary scan system with its advanced capabilities is well equipped to help implement system-level boundary scan applications. In fact, several ASSET customers have already deployed system-level JTAG and are currently reaping significant advantage in the marketplace. Some of the capabilities of ScanWorks that are particularly useful in system-level applications are the following:

- Describe system-level JTAG features with ScanWorks Hierarchical Scan Description Language (HSDL)
- Supports all popular scan bridges, multi-drop gateway devices and embeddable test bus controllers from vendors such as TI, Firecron, Lattice Semiconductor and National Semiconductor
- Supports embedded test vector formats for embedded boundary-scan controllers
- Supports multiple scan paths

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- Supports IEEE 1532 and IEEE 1149.6 standards for concurrent in-system programming and the testing of high-speed AC-coupled nets

Where can you find more resources on system-level JTAG?

The ASSET Press Room (http://www.asset-intertech.com/press_room.html) has several sources of information on system-level JTAG, including a white paper entitled “System Test with JTAG” as well as several articles in recent issues of ASSET’s e-newsletter, *Connect – Your Source for Boundary Scan Information*. In addition, ASSET’s system-level JTAG webpage (http://www.asset-intertech.com/scanworks_system_level_jtag.html) features several sources of information.

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