

ASSET InterTech Press Backgrounder

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ASSET: Integrated Circuit, Board and System Test

ASSET InterTech, Inc. provides IEEE 1149.1 boundary-scan (JTAG) diagnostic hardware and software solutions that:

- validates the design of circuit boards
- debugs and tests integrated circuits, board-level products and systems
- performs in-system programming (ISP) of flash memory and programmable logic

The company also offers services to assist design engineers as they incorporate testability concepts and techniques into their projects.

ASSET's ScanWorks® environment is a suite of PC-based tools which can be configured for:

- design validation and debug in development environments
- test creation, application and diagnosis during manufacturing
- troubleshooting and diagnostics during field test and repair.

ASSET InterTech began as a business unit of Texas Instruments, Incorporated. In July of 1995, TI's ASSET product family and related business were acquired by ASSET InterTech, Inc., which was founded by the team that had designed, developed and marketed ASSET for the previous six years. ASSET InterTech has an installed base of more than more than 3,000 systems sold worldwide in hundreds of organizations. Among its customers are prominent companies such as Cisco, Microsoft, Motorola, Agilent Technologies, Lucent, Delphi, Ericsson, Intel, BAE, Rockwell, Alcatel, Tellabs, Huawei, Lockheed Martin, EMC, ITT, Northrop Grumman, Raytheon, Solectron and others. Strategic marketing and development relationships have been established between ASSET and Agilent Technologies, Intel, Parametric Technology Corporation, Xilinx, Lattice Semiconductor, Altera, International Test Technologies and other prominent companies to advance the use of boundary-scan technology by delivering advanced test and ISP solutions.

The Boundary-Scan Market Today and Tomorrow

Prior to the emergence of the IEEE's 1149.1 boundary-scan standard in the early 1990's, the electronics industry had no standard test procedures. With ever shrinking component geometries and new packaging techniques, traditional test techniques requiring physical access to devices had become increasingly outmoded. The boundary-scan standard specifies an architecture which gives engineers the electronic access and control over devices and systems that they need without requiring physical access to pins or pads. For an online video introduction to boundary scan or a tutorial on the technology, go to http://www.asset-intertech.com/access_world_of_benefits.html

In the near future, the electronics industry's migration to lead-free soldering techniques will cause additional growth of boundary-scan test. The European Union, for example, has already required lead-free solder in all electronics equipment. Replacement solder compounds will place greater force on PCBs from invasive testing technologies like ICT,

increasing the strain on circuit boards at a time when manufacturers are striving to reduce it for reliability reasons. Boundary scan offers a test solution that places no strain whatsoever on PCBs. This is a critical concern for manufacturers of mobile devices.

Since its beginning, IEEE 1149.1 Boundary-Scan Standard has evolved from a physical access-less interconnect test capability for PCBs to a board- and system-level infrastructure technology that provides the basis for much, much more than simple interconnect test. Boundary scan has emerged and will continue to evolve in the future as a foundational technology for a host of complementary capabilities, like IEEE 1532 in-system configuration (ISC) of programmable logic, in-system programming (ISP) of flash memory, IEEE 1149.4 analog test, processor-based emulation test, IEEE 1149.6 high-speed AC-coupled test and, most recently, Intel® IBIST (Interconnect Built-In Self Test). For this trend to continue, the boundary-scan functionality at the disposal of engineers and technicians must be based on powerful yet simple capabilities. And that's what ASSET ScanWorks provides. For a fuller explanation of ASSET's vision of boundary scan's evolution in the future, go to <http://www.asset-intertech.com/connect/2004Q4/observations.htm>

What's New

The ScanWorks JTAG system has recently been enhanced significantly with new hardware and software. A new PCI-based hardware controller board for ScanWorks is a combinational test platform capable of applying both JTAG structural tests and programming operations, as well as processor-based functional emulation tests. The PCI-200EJ streamlines the entire test application process by combining both types of tests on one platform. Developed in collaboration with strategic partner, International Test Technologies (ITT) of Ireland (www.intertesttech.com), the PCI-200EJ controller increases test coverage by supporting ScanWorks' JTAG operations and the functional testing capabilities of ITT's μ Master emulation testers.

In addition to the PCI-200EJ, the ScanWorks JTAG system has been enhanced with increasing openness to third-party technologies and products. The latest version of ScanWorks (3.8) incorporates new features such as External I/O Management which allows for the easy integration of third-party hardware to test signals that are routed off the circuit board through a connector. Moreover, the new ScanWorks now is open to the data mining probes of SigmaQuest (www.sigmaquest.com), a third-party supplier of automated test and quality data management systems. By opening ScanWorks to SigmaQuest's products, ScanWorks users are able to leverage consolidated business intelligence across their product design, manufacturing, supply chain and repair/return operations.

For a complete news release and photo of the PCI-200EJ controller, as well as a news release on ScanWorks 3.8 functionality, go to the Press Room on the ASSET web site (http://www.asset-intertech.com/press_room.html).

The ASSET ScanWorks Product Family

ScanWorks operates from a hardware controller board installed in a PCI bus-based PC or a PXI chassis. In addition, ScanWorks supports a USB controller pod which interfaces to a host PC via its USB port and the circuit board being tested through the usual boundary scan cable and connector. ScanWorks runs in the Windows® XP, Windows 2000 and Windows NT™ environments, although it can also interface to a UNIX-based 3070 system. ScanWorks reduces test and programming costs significantly throughout the entire product lifecycle, beginning with development, continuing through manufacturing test, including functional and environmental test, and culminating in field service. Moreover, ScanWorks' many automation features and technologies, such as TopCAT™, vastly improve the productivity of test engineers and facilitate efficient test operations.

How and Where ScanWorks Is Used

ScanWorks targets and is deployed in three major areas within user organizations:

- Development
- Manufacturing
- Repair

Development Stations

ScanWorks development stations include the Test Development Station (TDS) and the Interconnect Development Station (IDS). Both systems include tools that will create a database description of a scan-based system, automatically verify a boundary-scan path, automatically generate test vectors and display failures in the unit under test (UUT). ScanWorks' analytical capabilities help development teams quickly isolate problems in prototypes and streamline the creation of test vectors in both development and manufacturing environments.

The Interconnect Development Station bundles many of the key capabilities of Scanworks for new or occasional boundary-scan users who need to quickly develop and deploy effective JTAG tests. The IDS includes ScanWorks hardware and pre-configured software at an affordable price. The TDS includes all of the features of an IDS in addition to several more advanced features that are bundled into the TDS for experienced and power users.

In addition, in-system programming (ISP) operations for the loading of program data into flash memory or configuration data into programmable logic devices (PLDs) can be developed on a TDS or an IDS. ScanWorks is compatible with programming standards and methods, including the IEEE 1532 In-System Concurrent Configuration standard, Serial Vector Format (SVF), Jam™ and STAPL.

Manufacturing Station

The ScanWorks Manufacturing Station will apply any test or programming operation that has been created on a ScanWorks development station or Programming Development Station. The portability inherent in the ScanWorks environment makes it easy for many of the test vectors developed during a product's design stage to be migrated and re-used in assembly and manufacturing. The ScanWorks Manufacturing Station is a complete test system because it comes with an easy-to-use and intuitive user interface. But, should the organization have a third-party or custom-developed test executive, the ScanWorks Manufacturing Station can be easily integrated into test executives that have been created with the most popular tool sets, such as National Instruments' LabVIEW®, TestStand, LabWindows/CVI®, HP-VEE™ or Visual Basic, reducing any training requirements for manufacturing test technicians. The ScanWorks application programming interface (ScanWorksAPI) features a library of NI Virtual Instruments (VIs) and a Dynamic Link Library (DLL) interface to facilitate the speedy integration of ScanWorks into test executives. In addition, popular scripting languages such as Tcl and Perl are also supported.

Diagnostic and Repair Stations

When failures are discovered on the manufacturing floor, the ScanWorks Diagnostic Repair Station (DRS) and Interconnect Repair Station (IRS) can rapidly isolate faults and debug failed production units. Both systems are configured with ScanWorks' diagnostic and repair features, including automated pin-level diagnostic capabilities. Thus, interconnect and memory failures can be readily diagnosed.

The Interconnect Repair Station (IRS) is a bundled solution that can be rapidly deployed to meet the needs of new or occasional boundary-scan users. Later, as the needs and expertise of the operation increases, the IRS can be upgraded with the greater capabilities of the DRS. The DRS includes all of the features of the IRS in addition to several advanced functions. In field test or repair depot operations, for example, a DRS can be used for its advanced diagnostic and debugging capabilities.

DFT Analyzer

ASSET has also introduced the industry's first JTAG design-for-test (DFT) system, DFT Analyzer. This standalone system is used during the design of a circuit board or system to ensure maximum boundary-scan test coverage long before prototypes of the product are assembled. This reduces the manufacturer's costs by reducing the need for expensive design re-spins after prototypes have been built to include better test coverage and by reducing production schedule risks resulting from inadequate test coverage when the product moves into manufacturing.

Strategic Relationships

ASSET has established strategic relationships with several prominent electronics companies, including Agilent Technologies, Intel® Corporation, Parametric Technology Corporation, Altera, Xilinx, Lattice Semiconductor, International Test Technologies and others.

Under the company's agreement with Agilent, ScanWorks has been integrated into PC- and UNIX-based Agilent Medalist i5000 and 3070 Series ICT systems. Customers are able to re-use boundary-scan tests and programming algorithms developed during design debug throughout a product's entire lifecycle, including high-volume manufacturing testing on the i5000 or 3070, functional and environmental test, and in-the-field troubleshooting or repair.

Intel and ASSET have worked closely together on support tools in ScanWorks for Intel's next-generation embedded test technology, Intel IBIST (Interconnect Built In Self Test). ScanWorks is the only boundary scan system to offer support for Intel IBIST, which the company is incorporating into many of its next-generation chips and chipsets.

As a result of the strategic relationship between ASSET and Parametric Technology, ScanWorks became the first boundary-scan environment with an electronic design browser. By integrating Parametric's InterComm design browser, designers and test engineers are able to correlate boundary-scan test information and design data like schematics and layouts from within ScanWorks.

ASSET and Altera have a long history of collaboration on in-system programming practices. ASSET was the only boundary scan tools company to participate with Altera on the JDEC-sponsored efforts to develop the Standard Test and Programming Language (STAPL – JESD-71), which utilizes the on-board infrastructure of boundary scan.

Xilinx Corporation, a leader in programmable logic devices and gate arrays, and ASSET have a strategic relationship whereby ASSET validates the accuracy of the boundary scan description language (BSDL) files for all Xilinx devices.

Lattice Semiconductor's concurrent programming engine, the ispVM System, has been integrated into ScanWorks. Conforming to the IEEE 1532 Standard for In-System Configuration, the ispVM engine gives SanWorks the ability to program multiple on-board logic devices simultaneously.

ASSET and International Test Technologies have collaborated on ScanWorks Extended JTAG Coverage, which combines the emulation-based functional test technology of µMaster from International Test Technologies with ScanWorks.

Partner Providers

ASSET's Partner Provider program teams ASSET's expertise in test strategies and implementation techniques with third parties that have extensive experience in migrating boundary-scan tests from a company's design group to volume manufacturing. These third-party partners include:

BreconRidge Manufacturing Solutions Corporation, Ottawa, Canada.

Datest, Inc., Fremont, Calif.

Solution Sources Programming, Inc., San Jose, Calif.

The Testing House, Fremont, Calif., Guadalajara, Mexico, and Seoul, South Korea

Saab Test Systems, Stockholm, Sweden

Complementary Technologies

The ScanWorks boundary-scan environment works in conjunction with several other technologies. ASSET InterTech has effective working relationships with many of the companies that provide these technologies.

Electronic Design Automation (EDA)

All EDA vendors such as Mentor, Cadence, Synopsis, LogicVision and Syntest have developed certain built-in self test (BIST) capabilities which can be accessed through boundary scan. As a consequence, to the extent that these tools are compatible with the IEEE 1149.1 boundary scan standard, ScanWorks is compatible with them and complements their functionality.

In addition, ScanWorks re-uses data from printed circuit board tools from the most prominent schematic capture and layout tools from vendors such as Mentor Graphics, Cadence, Zuken and Altima, in order to automatically generate test patterns and display faults.

Vendors of Boundary-Scan Technology

Lattice Semiconductor -- A leader in programmable logic devices (PLDs), Lattice Semiconductor has developed the Multiple Scan Port Linker, a reference design for four scan ports that can be loaded into a programmable logic device to enhance the scan capabilities of a design.

National Semiconductor Corporation -- ScanWorks supports National's SCANTM Bridge, a hierarchical and multidrop addressable boundary-scan port, as well as other devices that are needed to perform IEEE 1149.1 boundary-scan test or on-board programming.

Texas Instruments, Inc. -- ScanWorks supports TI's testability support devices, including the Addressable Scan Port (ASP), Scan Path Linker, 8890 and 8980 test bus controllers and other 1149.1 devices.

Firecron -- ScanWorks supports Firecron's boundary-scan semiconductors, including its gateway device and controller.

Functional Test Companies

Agilent Technologies -- ASSET's ScanWorks supports various test and programming tools from Agilent, including the company's graphical test programming environment, Agilent VEE.

National Instruments -- As previously mentioned, ScanWorksAPI facilitates the easy integration of boundary scan tests into test executives developed with any of NI's tool sets, such as LabVIEW, LabWindows and TestStand.

Teradyne -- Teradyne's automatic test pattern generation software, VICTORY, Virtual Interconnect Test (VIT), Access Analyzer and Boundary-Scan Intelligent Diagnostics (BSID) have been integrated with ScanWorks. This integration allows for a seamless test flow from prototype debug to Teradyne Z, Spectrum and L-Series ICT systems and on to environmental test and field test.

Management Team and Board of Directors

Management Team

Glenn Woppman, President and CEO

Prior to being named president and CEO in 1995 when ASSET InterTech became an independent company, Mr. Woppman was product manager for the ASSET business unit within TI. He was responsible for all business functions relating to ASSET, including sales, marketing, R&D and finance. Mr. Woppman has managed 30 percent annual growth for the group and has helped to establish the ASSET ScanWorks product family as a leading technology in the test industry. He has an MBA from Southern Methodist University and a BSIE from the University of South Florida.

Gerry Morgan, Vice President, Product Development

Mr. Morgan has more than 20 years of experience in the test industry. He has worked for Fairchild Semiconductor, GenRad®, where he led development projects such as the Encompass software that runs on the GENEVA Test System, and Brooks Automation. He holds an MBA from Northeastern University, and BS and ME degrees in Electrical Engineering from the University of Maine.

ASSET InterTech Company Background

Alan Sguigna, Vice President of Sales and Marketing

Mr. Sguigna has more than 20 years of experience in senior-level general management, marketing, engineering, sales, manufacturing, finance and customer service positions. Before joining ASSET, he worked in the telecom industry. He has had profit and loss responsibility for a \$150 million division of Spirent Communications, a supplier of test products and services. Prior to his tenure with Spirent, Mr. Sguigna also served in business development positions with Nortel Networks, overseeing the growth of its voice over Internet protocol (VoIP) products.

Adam Ley, Chief Technologist

Mr. Ley is responsible for plotting the direction of ASSET's industry-leading boundary scan technology. Additionally, he participates in various industry bodies, including the IEEE 1149.1 working group on boundary scan and the IEEE 1149.6 committee that is developing test methodologies for high-speed serial AC-coupled nets. He has been involved in boundary-scan technology since 1991 and was a key technical leader for Texas Instrument's Logic Products division's efforts to develop and bring to market its line of boundary-scan bus interface and scan support products. He holds a BSEE degree from Oklahoma State University.

Tim Caffee, Vice President of Design Validation

Mr. Caffee's business unit is responsible for bringing new tools to market that will validate the design of next-generation products. Previous to this position, he played a key role in new business development, facilitating global deployment of boundary-scan tools and managing key customer accounts. He was a founder of ASSET and has spent 15 years working with boundary-scan tools. Prior to ASSET, he spent several years at Texas Instruments in the defense business unit. Mr. Caffee obtained B.S. degrees in Mathematics and Computer Science at Old Dominion University.

Arden Bjerkeli, Director of Customer Applications Support

As director of customer applications support, Mr. Bjerkeli manages a group of engineers that provides pre- and post-sales support, customer-driven maintenance and other services, and customer training. Prior to joining ASSET, He held various engineering management positions for Compaq Computer Corporation for more than 16 years. At Compaq, he managed several engineering groups that were responsible for developing and testing new desktop computer and server products. In addition, he served in several testability research and development positions. He has a bachelor's degree in Electrical Engineering from the University of Houston.

Board of Directors

Glenn Woppman, President and CEO

See biographical information under Management Team above.

Bill Drobish

Mr. Drobish has over 30 years of executive and management experience in the high tech and software industry. He was one of the three founders of Silicon Systems and helped manage that company as its sales grew to more than \$100 million. Mr. Drobish has been involved to varying degrees with several other start-up electronics companies. He currently has served on the board of TMA, Microsim (P-Spice), Kofax Image Products and many others. He has an electrical engineering degree from Purdue University.

Andy Mindlin

Mr. Mindlin of Corona del Mar, Calif, is a management consultant and president of RealWorld Marketing, Inc., which provides marketing and general management assistance to high technology and high-growth firms. Mr. Mindlin has over 18 years of experience in product development, marketing, general management and sales. He previously held marketing positions with Proctor & Gamble and Richardson-Vicks. Mr. Mindlin is a Phi Beta Kappa graduate of Vanderbilt University.

Anthony J. LeVecchio

Mr. LeVecchio is the president and owner of The James Group, Inc., a business support and development company in Dallas. At various times during his career, Mr. LeVecchio has acted as both an interim chief financial officer and as a financial oversight executive to assist companies with financial planning, cash management, internal controls, strategic and operating plans, negotiated settlements and stock structures. He has served as CFO of VHA Southwest and Phillips Information Systems. He also worked for Exxon Office Systems and Xerox Corporation. He has a BA in Economics and an MBA in Finance from Rollins College.

Steven Ho

Mr. Ho is an investment manager at Technology Associates Management Co. (TAMC), Ltd., a venture capital fund management company in Plano, TX. Prior to joining TAMC, he worked in the semiconductor and IT industries, most recently with Cyrix Corp., in microprocessor design, and earlier with Pacific Microtech, a startup venture in PC manufacturing and services. Mr. Ho has a B.S. degree from National Taiwan University, a Master's Degree from Stanford University and a Ph.D. from the University of Illinois.

Technical Advisory Board

Dr. R. G. "Ben" Bennetts

Dr. Bennetts is a noted pioneer in digital test. He was one of the original members of the group that first defined the boundary-scan specification, the Joint Test Action Group (JTAG). For the last 20 years, Dr. Bennetts has been a recognized textbook author, lecturer and consultant on digital testing. Dr. Bennetts received his Bachelor's of Science degree from Famborough Technical College and his Master's and Doctoral degrees from Southampton University.

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Dr. Arnold Jang

Arnold Jang is a senior investment manager of TAMC, Ltd., a venture capital fund management company with headquarters in Plano, TX. Prior to TAMC, Dr. Jang managed an investment portfolio for Springfield Financial Advisory of Taipei, Taiwan. He has also taught management information systems at the Chinese Culture University in Taiwan. He has a Ph.D. in Computer Science and an MSEE in VLSI Computer Aided Design from the Graduate School of Electrical Engineering at the National Taiwan University.

Jim Wolfe

Jim Wolfe is a principal at Red River Ventures. Previously, Mr. Wolfe spent eight years at Banc One Capital Partners where he managed a portfolio of investments in a variety of industries including financial services, environmental consulting, transportation and business services. Mr. Wolfe has held various positions within MBank Dallas' international lending groups developing the bank's portfolio of loans in Latin America and Europe. He managed the MBank Dallas' commercial syndication efforts within the bank's statewide bank network. He has both a BBA and MBA from Southern Methodist University

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