

Home	EDA/ EDA Tools	FPGAs/ PLDs/ CPLDs	Intellectual Property	ESL Design	Special Topics/ Feature Articles	Vendor/ Organization Directory	About SOCcentral		
News	Major RSS News Feeds	Blog Roll	Articles Online	Tutorials, White Papers, etc.	Webcasts	Online Resources	Software	Tech Books	Conferences & Seminars

You are at: The item(s) you requested.

Monday, October 26, 2009

Test Standards Emerge to Improve 3D-Chip Yield Featured

Contributor: ASSET InterTech, Inc.

 [Printer friendly](#)
 [E-Mail Item URL](#)

October 5, 2009 -- Some industry experts have been so bold as to assert that stacking multiple silicon die in a single package is the most effective way for the industry to continue along the trajectory of Moore's law. This may or may not be true, but the fact remains that 3D chips with multiple stacked die are becoming critical to many types of electronic systems. Unfortunately, the yield on 3D chips can be surprisingly low because of the inadequacies of older chip-level validation and test technologies. Fortunately, several industry standards and advances by test companies are providing a glimmer of light at the end of the tunnel.

Through-silicon test

The problems associated with testing 3D chips begin with access – or a lack thereof – to the multiple die that make up the 3D device. All too often, one or more of the die in a multiple die system-in-package (SiP), package-in-package (PiP) or package-on-package (PoP) device will block any sort of intrusive probe-based test access to the other die in the package. When that happens, yield problems skyrocket.

With a single-die device, for example, a failure rate of one in 10 die is a 90% yield or a 10% loss rate. If three die are placed in a 3D chip and each of the die have a 10% loss rate, then the 3D device could also have a 10% loss rate. But, the three in 30 3D devices that fail will cause another six good die to be thrown away. That's a 30% yield for all 30 of the die in the 10 3D packages. A slightly worse yield on the individual die further degrades these numbers. For example, if each individual die family has a 70% yield, then the yield on the 3-die stack could theoretically become a mere 10%. (See Figure 1.) Furthermore, it should be noted that testing individual die before they are assembled into a multiple die 3D package is not adequate. The assembly process invariably introduces additional flaws and failures that must be found.

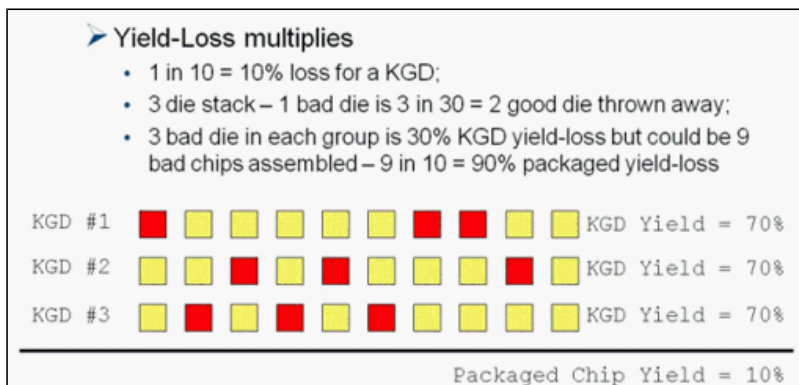


Figure 1. Known-good-die (KGD) integration issues. Yield on 3D chips can quickly degrade.

Since traditional probe-based intrusive test technologies are shut out from 3D chips, new non-intrusive test access methods are needed to continue the use of proven chip-test concepts and, by implication, improve the yield rate on 3D chips. Fortunately, several industry standards that are winding their way through the ratification process address these issues. In addition, semiconductor companies are embedding their die with various test and measurement instruments to mitigate the loss of access to external instruments, to overcome the growing inadequacy of external test equipment and to improve testability.

Two new standards in particular address the need for better test techniques for 3D chips. These are IEEE 1149.7, the so called "compact boundary-scan" standard, and the IEEE P1687 internal JTAG (IJTAG) standard. Other more established standards also come into play, such as the original boundary-scan standard, IEEE 1149.1 (commonly referred to as JTAG after the Joint Test Action Group which initiated development of the standard) and the IEEE 1500 Embedded Core Test Standard. In addition, proprietary test and measurement technologies are being embedded by semiconductor companies into chips and these too can be used to test 3D chips. One example of this is Intel's

Search site for:

[Search Tips](#)

Subscribe to SOCcentral's SOC Explorer Newsletter and receive news, article, whitepaper, and product updates bi-weekly.

[Subscribe](#)

New Tech Press Interview

A Lot of Hope for EDA



Gary Smith
President,
Gary Smith EDA

Want to put Audio in your next SoC?



Odd Parity MEMO-ries Are Made of This



Mike Donlin
The Write Solution
[Odd Parity Archive](#)

Find IP you need

SOCcentral makes it easy by providing listings for nearly 400 IP vendors and an interface to the [ChipEstimate](#) IP search engine.

[Search for IP Now!](#)

Special Topics/Feature Articles

- Design for Manufacturing
- Design for Test
- ESL Design
- Floorplanning & Layout
- Formal Verification
- Logic & Physical Synthesis
- On-Chip Interconnect
- Low-Power Design
- Reconfigurable Computing
- Selecting & Integrating IP
- Signal Integrity
- SystemC
- SystemVerilog
- Transaction Level Modeling (TLM)
- Verilog
- VHDL

SOCcentral Job Search

[SOC Design](#)
[ASIC Design](#)

[Analog Design](#)
[Mixed-Signal Design](#)

Interconnect Built-In Self Test (IBIST), which that company has embedded into its next-generation devices.

New standards for testing 3D chips

Of the two new IEEE standards which are pertinent to testing 3D chips, IEEE 1149.7 has deeper roots than IEEE P1687. 1149.7 is a complementary and enhanced derivative of IEEE 1149.1, the original boundary-scan standard, which was ratified in the mid-1990s. The two standards are fully compatible with each other. Many of 1149.7's test enhancements are squarely aimed at testing 3D chips. Most people refer to 1149.7 as a reduced-pin count 2-wire interface, but the standard allows for wide 4- and 5-wire implementation as well and there will certainly be many of these.

Some of the architectural aspects of 1149.7 will enhance 3D chip testing. Whereas the original 1149.1 boundary-scan standard restricted implementations to daisy-chain and limited star architectures, 1149.7 enables a broadcast star architecture which is far more appropriate for testing SOCs, SiPs, PiPs and PoPs in that it allows multiple 1149.1 Test Access Port (TAP) controllers to be dealt with in an addressable network manner.

For SOCs, this and other architectural enhancements in 1149.7 allow for the test and debug interfaces of each core to be consolidated onto a single 1149.7 interface at the package level. This can be a reduced pin-count interface (two rather than four) and it provides higher bandwidth because data is packetized. A 3-core SOC, for example, could conceivably have an 8-wire test interface for each core for a total of 24 signals on the SOC devoted to the test controller. With 1149.7 these signals could be consolidated into one 2- or 4-wire 1149.7 interface for the entire SOC.

For multi-die packages like SiPs, PiPs or PoPs, 1149.7 can be effectively implemented in tandem with through-silicon vias (TSV). If 1149.7 had been limited to 1149.1's daisy-chain architecture, a costly connectivity layer or substrate would be required in the package. Because 1149.7 is compatible with TSVs, each die can be connected for test purposes through a vertical via and a 1149.7 interface on each die. In addition, each die would have an addressable 1149.1 TAP controller.

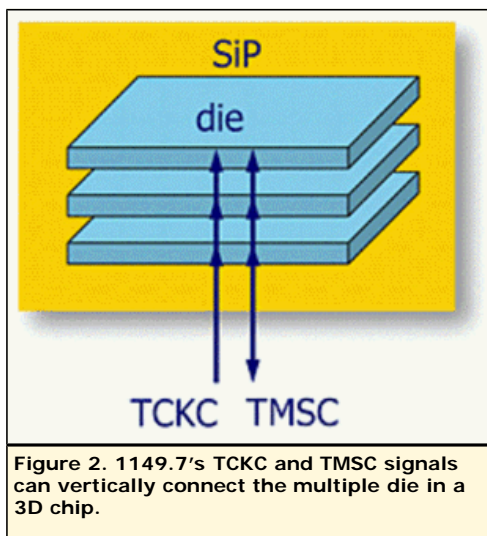


Figure 2. 1149.7's TCKC and TMSC signals can vertically connect the multiple die in a 3D chip.

IEEE P1687 IJTAG uses boundary scan (1149.1 or 1149.7) for access to 3D chips. The targets for this access are the test and measurement instruments that are embedded on-chip. Logic BIST, memory BIST, scan compression architectures and embedded-core wrappers are some of the various instruments that are commonly embedded. Intel's IBIST, is a prime example of proprietary embedded instrumentation technology. IBIST validates and tests high-speed serial buses such as PCI Express which can't be tested with physical probes and external instruments.

Since embedded instrument IP (intellectual property) can come from a number of sources, such as chip suppliers, third-party providers, EDA tools or in-house design groups, P1687 is intended as a standard way of connecting, accessing, analyzing and describing embedded instrumentation no matter what the source. This kind of open access to embedded instruments will ensure the development of third-party tools to take advantage of these instruments. As long as a tool or tool platform and the embedded instruments conform to the P1687 IJTAG standard, the two can work together.

IJTAG enables a number of embedded instrumentation functions that will improve the testability of a single chip or multiple die in a 3D chip. For example, IJTAG would simplify the parallel operation of multiple embedded instruments. An embedded logic BIST engine for chip test might be operated simultaneously with a voltage monitor intended for yield analysis. The resulting simultaneous operation of these two embedded instruments could determine whether failures identified at the ATE- or board-levels correlated with voltage starvation.

Re-using tests

Typically, the die that will be stacked into a 3D chip will be tested individually before they are stacked. It would be extremely cost effective if the same tests that were performed on the individual die to obtain "known good die" could be performed again on each die after they have been stacked into a 3D chip. Figure 3 shows how 1149.7 and P1687 IJTAG could be deployed to accomplish this.



ASIC Verification
FPGA/CPLD Design
PCB Design
DSP Design
Digital Design

DFT
VHDL
Verilog
SystemC
SystemVerilog

Post a Job Only \$30 for 30 days

SOCcentral.com focuses its news coverage on SoC/ EDA/ ASIC /FPGA/ IP technology, products, and standards. Because this doesn't keep you up-to-date on *everything* that might be important to you individually, we've made it easy to quickly check the RSS news feeds from major industry sources. Just go to:

[SOCcentral RSS News Feeds](#)

[About SOCcentral.com](#)

[Sponsorship/Advertising Information](#)

© SOCcentral

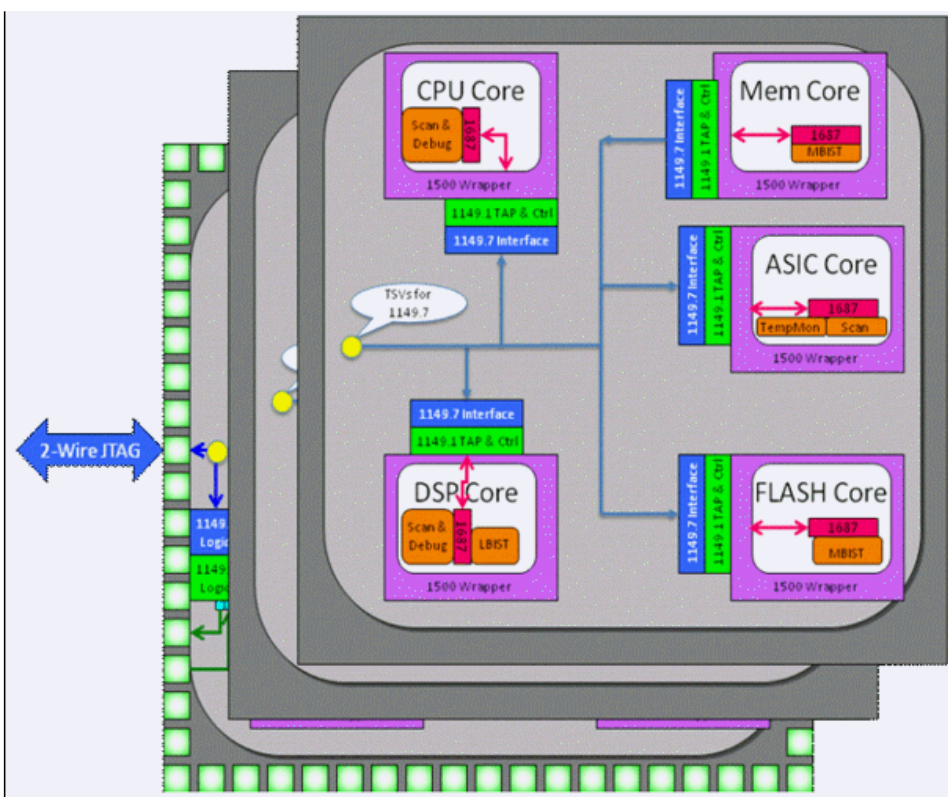


Figure 3. How a 3D chip could be tested with 1149.7 and P1687 JTAG. Note that three die are stacked on top of each other. The yellow dot represents a vertical TSV with 1149.7 access.

In this case, a 2- or 4-wire 1149.7 interface would connect the multiple die vertically through a TSV to the device's 1149.1 Test Access Port (TAP). A broadcast star architecture would connect each of the on-chip cores and P1687 JTAG would be utilized to coordinate the operations of all of the embedded instruments. In this scenario, a traditional boundary-scan platform, such as ASSET InterTech's ScanWorks platform for embedded instrumentation, could act as a test executive for 3D chip testing. All of the 3D chip's embedded test instruments and structures, including the environmental process monitors, could be engaged. The entire 3D chip could be tested as though it were one single-die chip. In addition, test data collected on the die in the 3D chip as well as the 3D chip itself could be correlated back to the test data collected on the individual die to quickly improve yields on 3D chips.

Testing throughout the product lifecycle

If re-using single-die tests on 3D multiple-die chips is intuitively cost effective, it certainly will be even more cost effective if these same tests can continue to be accessed and used throughout the entire lifecycle of the chip and the system that it is a part of. P1687 JTAG is being developed to carry this out. Figure 4 illustrates how this lifecycle test flow could become a reality.

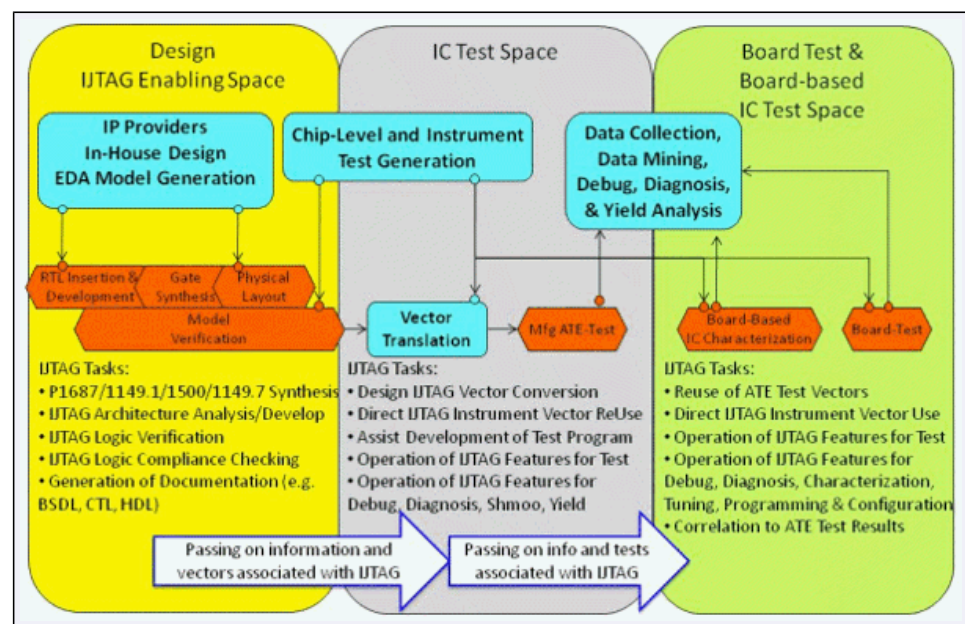


Figure 4. Lifecycle test flow within the context of the IEEE P1687 JTAG standard.

Encouraging signs

With regards to 3D chip test, it is very encouraging that standards such as IEEE 1149.7 and IEEE P1687 IJTAG are being put in place. The history of the chip and electronics industry has shown that open industry standards can provide the basis for markets to develop where multiple vendors innovate and compete with one another to provide the most cost-effective solutions possible. Certainly this is what will transpire in the emerging marketplace for test tools for 3D chips.



By Al Crouch.

Al Crouch is Chief Technology Officer, Core Instruments, at ASSET InterTech, Inc. of Richardson, Texas. He is a Senior Member of the IEEE and vice chairman of the IEEE P1687 IJTAG working group. He has filed for more than 30 DFT-related patents and been granted 15.

[Go to the ASSET InterTech, Inc. website to learn more.](#)

Keywords: ASICs, ASIC design, custom IC design, EDA, EDA tools, electronic design automation, packages, packaging, 3D ICs, 3D chips, ASSET InterTech,

488/29799 10/5/2009 407 407

[Add a comment or evaluation \(anonymous postings will be deleted\)](#)

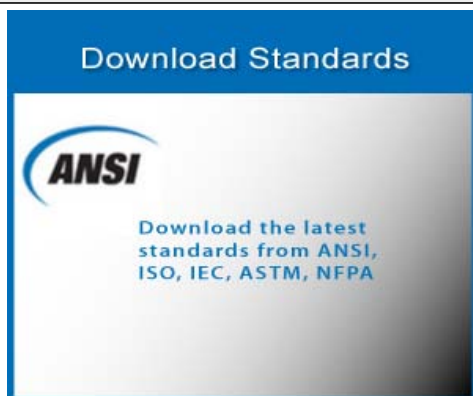
Design Mall

[Improve Viterbi Decoding Speed 250%](#)

Use Xtensa configurable processors to beat a high-end DSP core at Viterbi Decoding. Add Viterbi instructions and use the processor's configurable 128-bit I/O bus to load data for 8 symbols at a time to get this outstanding performance.

[The 11 Key Criteria for Selecting Custom Design Tools](#)

Learn about the expanded criteria that must be addressed to guarantee that the design ecosystem will optimize the often-conflicting needs and constraints within a company— including technical needs as well as matters related to internationalization, communication, workflow, finance, and security.



[Back to Top](#)

[The Home Port](#) [EDA/EDA Tools](#) [FPGAs/PLDs/CPLDs](#) [Intellectual Property](#) [Electronic System Level Design](#) [Special Topics/Feature Articles](#) [Vendor & Organization Directory](#)
[News](#) [Major RSS Feeds](#) [Articles Online](#) [Tutorials, White Papers, etc.](#) [Webcasts](#) [Online Resources](#) [Software](#) [Tech Books](#) [Conferences & Seminars](#) [About SOCcentral.com](#)

Copyright 2003-2009 Tech Pro Communications 1209 Colts Circle Lawrenceville, NJ 08648 Phone: 609-477-6308 Skype: john_miklosz
1 Execution time: less than 2 second(s)