

Embedded instrumentation delivers test/validation coverage on Intel Xeon 5500 boards

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Getting adequate test and validation coverage on ATCA boards based on the Intel Xeon Processor 5500 Series (codenamed Nehalem) can be difficult if you rely exclusively on older intrusive probe-based test equipment like in-circuit test (ICT) systems. Non-intrusive software-driven test technologies based on embedded instrumentation can deliver the coverage that intrusive technologies have lost in recent years.

Intrusive probes must make contact with device pins or test pads and both of these are hard to come by on Xeon 5500 ATCA boards. For example, with ball grid array (BGA) packaging a chip's pins are hidden underneath the silicon. And the test pads which had been on the surface of boards cannot be placed on the high-speed serial buses that are typically found on Xeon 5500 boards, such as Intel QuickPath Interconnect (QPI) or PCI Express. Test pads placed on these high-speed buses introduce capacitive anomalies which raise signal integrity issues.

Enter Embedded Instrumentation

The alternative to intrusive test is software-driven non-intrusive test technologies which make use of the embedded instrumentation that is being implemented in chips these days. This embedded instrumentation is either proprietary or open standards-based intellectual property (IP) which enables the test and validation of chips, boards and systems. Examples of embedded instrumentation include Intel's proprietary Interconnect Built-In Self Test (IBIST), the IEEE 1149.1 boundary-scan standard and processor-controlled test (PCT).

IBIST embedded instrumentation can be employed non-intrusively to perform structural tests on Xeon 5500 circuit boards or in design validation applications to validate the performance of high-speed serial buses. The boundary scan standard specifies a four-wire serial interface on chips, which is commonly referred to as the test access port (TAP) or simply the JTAG port. Structural boundary-scan tests are applied via a connector on the board and are scanned through the boundary-scan devices on the board. And fortunately the ATCA architecture specifies a JTAG backplane interconnect management bus. A third non-intrusive technology, processor-controlled test (PCT), uses the JTAG infrastructure in chips and on boards to access and apply the extended debug commands provided by the Xeon 5500 and other processors. The PCT system temporarily takes control of the processor and reads and writes memory and input/output (I/O) registers in the addressable devices on the board. In this way, PCT exercises the functionality of the board, and detects and diagnoses structural faults.

A Platform for Embedded Instrumentation

The ASSET ScanWorks platform for embedded instrumentation is the only system that supports all three non-intrusive test and validation technologies. By replacing the test coverage lost by the older probe-based technologies or complementing those technologies, ScanWorks is able to significantly improve coverage on Xeon 5500 boards.

The Test Challenge

Xeon 5500 boards present a number of test and validation challenges that, by and large, cannot be overcome solely by the older intrusive test technologies. Fortunately, software-driven non-intrusive test technologies like those running on the ASSET ScanWorks platform for embedded instrumentation offer alternatives. In the end, the goal of high test and validation coverage can be achieved.

