

Interconnect Built-In Self Test in Practice (INTEL[®] IBIST)

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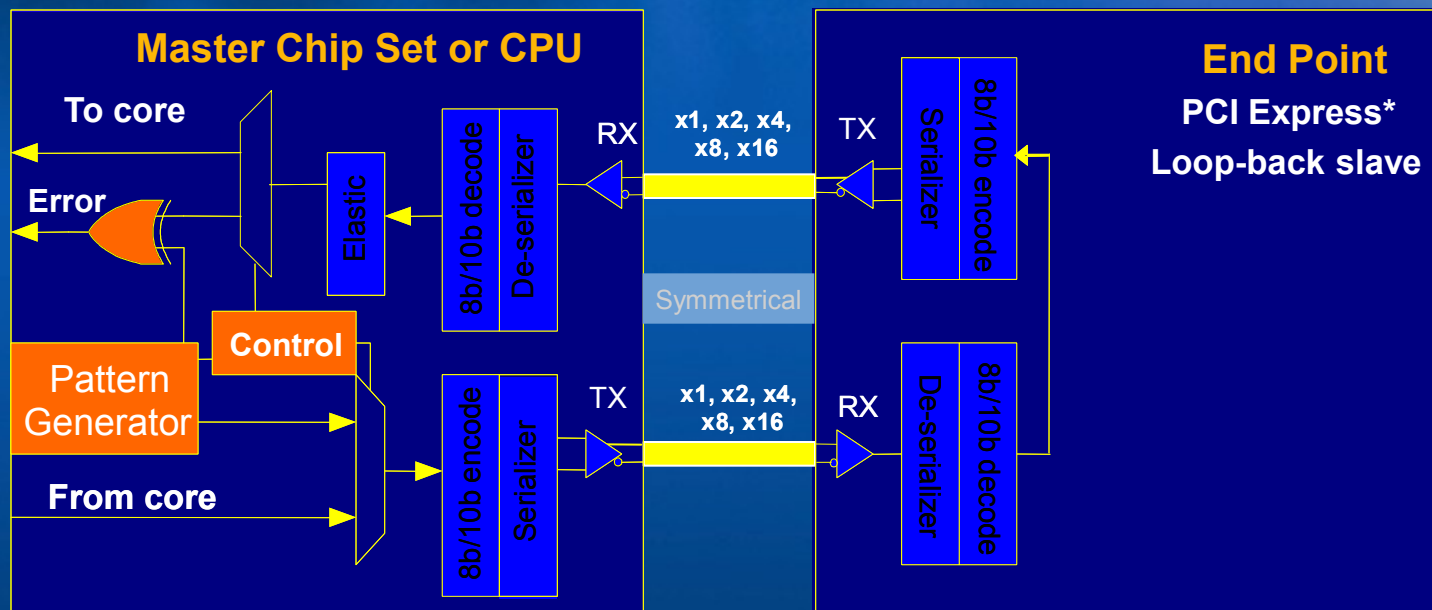
Current Test Tools Reaching Limitations for High Speed Buses

- **In-Circuit Test (ICT) points impractical**
 - High routing densities, small via size and spacing on PCBs
 - ICT test points create stubs that limit bus speeds
 - No Test pads allowed on 5 GHz and higher buses
 - CAD & SI groups reluctant to give us test pads
 - No AC or high speed tests are practical on ICT
- **BScan (IEEE 1149.1) limited**
 - Cannot test AC coupled high speed buses (PCI Express, SRIO, FC)
 - Buses sensitive to more than just opens, shorts
 - Signals sensitive to RF parameters of boards and chips.
 - Many PCI Express devices do not support IEEE 1149.6 AC EXTEST
- **Functional Test has Test Escapes**
 - Cannot detect opens and missing caps due to error correction
 - Requires very long test times to detect faults
 - Fault detection not reliable and cannot diagnose to the failing lane
 - Test Escapes can cause latent failures in the field (and lots of expense !)

What is INTEL® IBIST ?

- Interconnect Built-In Self Test
- Built-in test logic in Intel chip sets to test high speed serial links
- Designed to test structural and RF faults between chips
- First generation designed for PCI Express and FBD buses (Fully Buffered DIMM)
- Second generation supports PCI Express and QPI (QuickPath Interconnect)
- BIST logic in chipset will send/receive packets to PCIe peripherals
- Enables chip-to-chip interconnect testing at full speed
- Invented at Intel to enable high speed serial bus debug and analysis
- First offered by a tool vendor in 2005 (ASSET InterTech, Inc.)
- We had working demo board in May, 2006

How does IBIST work ?



- Master chip set or CPU has all IBIST logic – Pattern gen, Control, Compare
- Master device commands link to train with remote device in loopback mode
- Master on the bus initiates bus cycles to send patterns to the remote device
- Remote device retransmits same pattern information back to the master
- Master receives the data and performs error checking on the patterns
- Control, pattern, and error data stored in registers in core of chip

Features of IBIST Generations

- 1st GENERATION

- Supports validation and testing high-speed PCI Express buses at full speed
- Supports validation and testing high-speed FBD memory buses at full speed
- Provides ability to margin driver I/O voltage
- Provides ability to adjust receiver sensitivity

- 2nd GENERATION

- Supports validation & testing high-speed PCI Express buses at full speed
- Supports validation & testing high-speed QPI front-side buses at full speed
- Provides ability to margin driver I/O voltage
- Provides ability to adjust receiver threshold
- Can do BERT tests to check stability of the link
- Can produce receiver “eye” plots – depends on the chipset
- Can force a static 0 or 1 value on selected lanes
- Compliance mode allows comparing data on the slave device

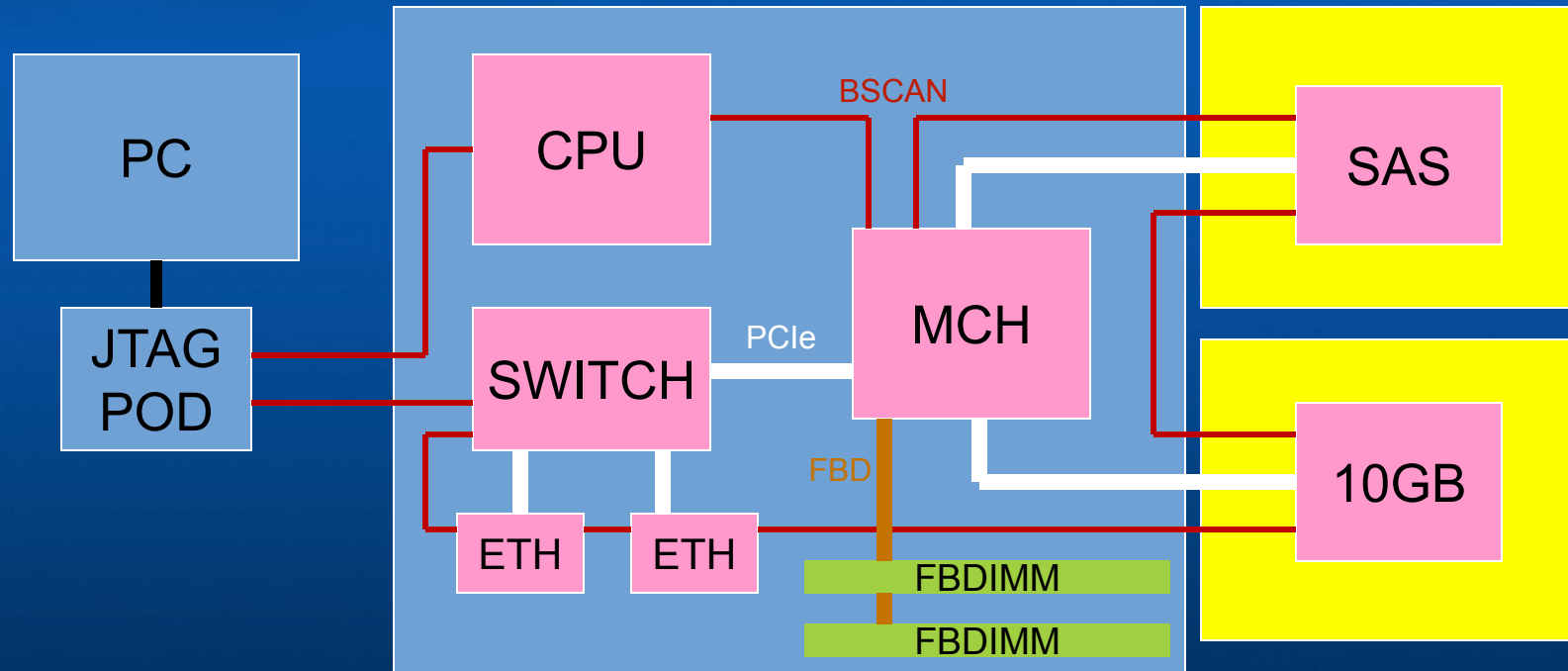
IBIST features Common to both Generations

- Can produce diagnostics down to the failing lane
- Facilitates design validation & characterization
- High Volume Manufacturing test of PCIe, FBD, QPI buses at speed
- Pre-boot test and debug of PCIe busses
- Can apply built-in worst case test patterns or custom made
- Operates independently of normal bus protocols
- Can provide data to display a receiver eye pattern for each lane
- Built On-die to eliminate need for ICT test pads on boards
- Requires no extra test hardware – comes for “free” in chipset
- Supported by 3rd party tool vendors – Turnkey software package
- IBIST test is re-usable throughout manufacturing processes

Requirements for IBIST Test Operation

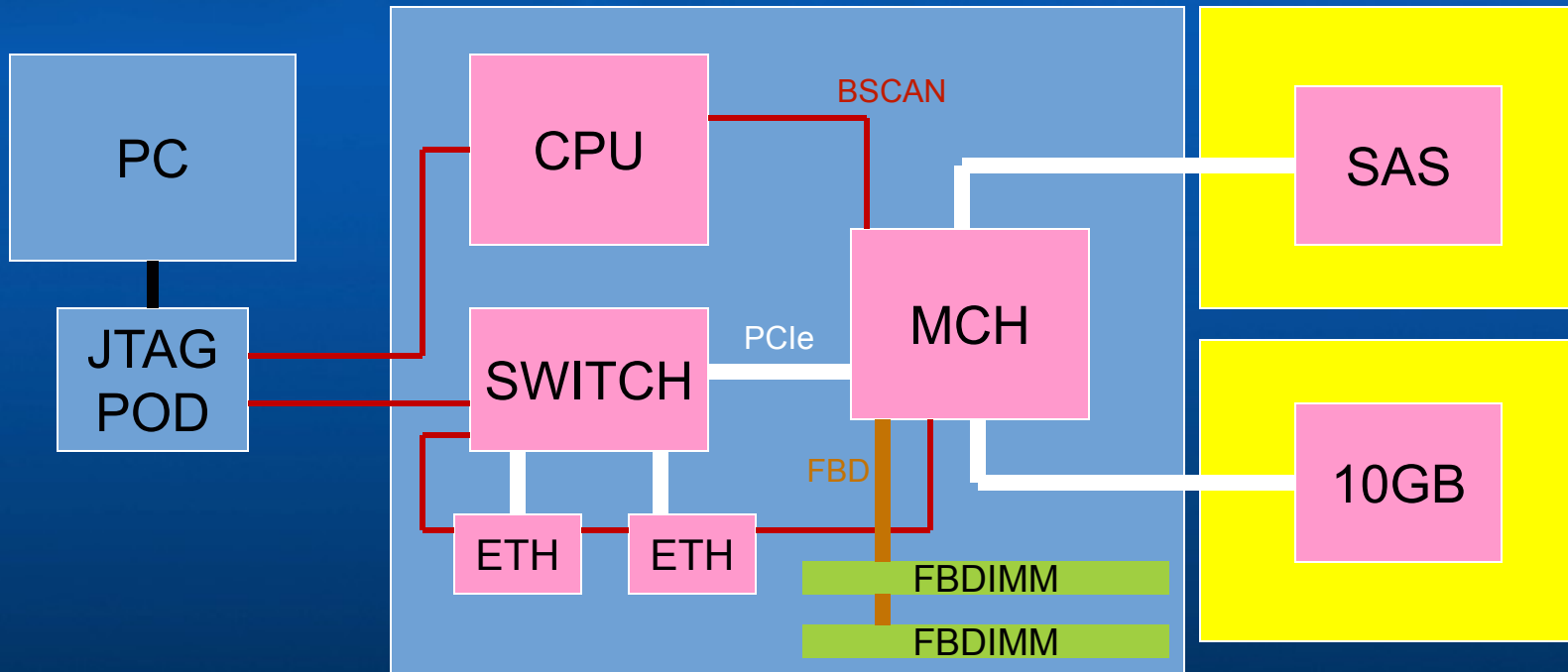
- JTAG chain that includes CPUs and Intel MCH or IOH Chipset
- Or can use Emulator or Diagnostic software to access registers
- JTAG software from 3rd party tool supplier can provide the best diagnosis info for manufacturing test
- 3rd party software requires netlist of motherboard and BSDL files
- Optionally requires netlist of daughter cards (if not captive)
- If daughter cards are not captive, then need to merge netlists together
- PCIe peripheral chips (end points) do not need IBIST logic
- End point chips can be made by any manufacturer
- Endpoints must support PCIe spec for In-Band Slave Loopback mode
- Can use 3rd party XDP pod for connection to JTAG tester
- Or can use your existing JTAG test connector and scan chain

Typical IBIST setup with Tested I/O Cards



- With non-captive I/O cards, can get chip/pin info from IBIST
- Need netlist and Bscan on I/O card
- Useful when I/O card designed in-house

Typical 1st Gen IBIST setup with Captive I/O Cards



- With Captive I/O cards, can still do IBIST test
- To test the PCIe buses to the I/O cards
- No need for netlist or Bscan on I/O card
- Useful when I/O card designed outside

Our IBIST Test Setup

- Using our standard scan chain on motherboard
- Uses standard PCI-100 JTAG pod connected to PCI card in PC
- Testing 2 PCIe buses local to Motherboard (ICH, PCIe Switch chip)
- Can test 4-lane buses going to each of 4 I/O cards
- Testing 4 channels of FBD DIMMs
- Bscan Test takes 6 seconds
- IBIST PCIe test takes 20 seconds
- IBIST FBD test takes 20 seconds
- Can test in standard product chassis or special debug fixture
- Data accessed through JTAG, Emulation, or Software Diagnostics

Problems Overcome in Test Development

- Endpoint chip on I/O card does not support slave-loopback.
 - Causes timeout errors on all I/O card ports
 - Vendor fixed in next generation of chip
 - But still had to GND a pin to get slave loop-back mode
- Endpoint chip that is in the chain fails to loopback the packets
 - Vendor was putting all chips in HIGHZ mode which shut off PCIe outputs
 - Vendor patched software to put all chips in bypass except CPU which is HIGHZ
- FBD memory test not testing 2nd DIMM in the channel
 - FBD DIMMs are daisy-chained with 24 high speed serial lanes
 - 1st DIMM is only one tested with standard vendor software
 - Vendor provided register settings to pass through 1st DIMM and test 2nd DIMM
- FBD memory tests always fail right after power up
 - Need to wait for 30 seconds of boot-up so memory controller is configured

IBIST Fault Detection Capabilities

- Reliably finds these faults
 - Short P cap to N cap on MCH side
 - Short P cap to N cap on endpoint side
 - Short N cap to GND on endpoint side
 - Short P cap to GND on endpoint side
 - Short P cap to GND on endpoint side
 - Short N cap to GND on endpoint side
 - Remove or Tombstone cap on P side
 - Remove or Tombstone cap on N side
 - Remove or Tombstone both caps
 - Short P res to N res (side not noted)
 - Short P res to 3 volts (side not noted)
 - Short N res to 3 volts (side not noted)
 - Short Lane 0 N cap and Lane 1 P cap on endpoint side
 - Short Lane 0 P cap and Lane 1 P cap on endpoint side
 - Short Lane 0 N cap and Lane 1 P cap on MCH side
 - Short Lane 1 N cap to Lane 2 P cap on MCH side

IBIST Fault Detection

- Intermittent Detection
 - Short P cap to GND on MCH side
 - Short P res to GND (side not noted)
 - Short N res to GND on endpoint side
 - Short Lane 2 N cap and Lane 3 P cap on endpoint side
- No Detection
 - Some lane to lane shorts

Advantages for EMC Manufacturing

- Catches high speed failures on about 1.5% of all JTAG failures
- These failures would not be found by other test processes
- No extra hardware in tester, fixture, or on product motherboard
- Tests easily added to existing testware infrastructure
- Addition of IBIST test does not add to manufacturing license costs
- Only cost is development license
- Actual development labor is approximately 1 day
- Gathering more data on new products

Future Wish List for IBIST test

- Need it available on all SERDES based CPU complexes
- Currently only on “Enterprise” chipsets
- Need support for some kind of BIST on DDR3 buses
- Need more chip or 3rd party vendors to provide tools for embedded test
- Need IJTAG standard now so that 1 tool set could allow access to all vendors’ chips
- Need IBIST to be able to test through a switch chip to end points on the other side of the switch
- Or we need switch vendors to build in IBIST logic
- Need enhancements to allow diagnosis of which wire failed
- Thanks for listening !

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