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## SiliconAid JTD Chip Debugger to Integrated into ASSET ScanWorks

Posted by Ken Cheung in [Test Solution](#) on Wednesday, November 4, 2009

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ASSET@ InterTech, the leading supplier of open tools for embedded instrumentation, and SiliconAid Solutions, Austin, TX., have formed a strategic relationship whereby ASSET will integrate its first integrated circuit (IC) test tool into the ScanWorks® platform for embedded instrumentation and resell SiliconAid's insertion and verification tools that support the emerging IEEE P1687 Internal JTAG (IJTAG) standard. SiliconAid is a supplier of world class chip verification and debug tools that support the IEEE 1149.1 Boundary-Scan Standard, which is commonly referred to as JTAG after the Joint Test Action Group which initiated development of the standard.

"This is just the first step toward our vision of a continuous test flow beginning at the chip level and extending to circuit boards and systems," said Glenn Woppman, president and CEO of ASSET. "Beyond this chip debugger that we'll be integrating into the ScanWorks platform, we can see a time when extensive chip tests can be re-used in board and system test, saving manufacturers considerably on test development and shortening time-to-market. We're also excited about promoting SiliconAid's IEEE P1687 IJTAG tools. We want to encourage the adoption of this emerging standard because we believe it will be critical to the effective utilization of embedded instrumentation in future test and measurement applications."

SiliconAid's JTD[tm] chip debugger, which will be integrated into ScanWorks immediately, is a robust real-time test and debug tool that can monitor structures inside chips and give visibility through an intuitive graphical interface to the engineer who is debugging the device. Although ASSET will initially resell SiliconAid's IEEE P1687 IJTAG synthesis (JTS[tm]) and verification (JTV[tm]) tools, future plans could call for these tools to be integrated into ScanWorks as well. JTS[tm] and JTV[tm] allow chip designers to automatically insert IJTAG capabilities into chips and subsequently verify the implementation. IEEE P1687 provides a standard interface to instrumentation embedded in chips.

"We are excited about teaming up with ASSET to resell our tools and to help lead the industry's adoption of the IJTAG IEEE P1687 standard," said Jim Johnson, president of SiliconAid. "This standard is not just important for our two companies. It will be critical to the industry as embedded instrumentation proliferates in next-generation devices. Standards like P1687 enable a higher level of integration and automation, beginning with chip design and test, and then transitioning seamlessly into board test. Adding IEEE P1687 IJTAG tools into our suite is a natural next step for us to leverage our existing products and offer more value to our customers."

As part of the new relationship, the two companies agreed to do joint marketing. The first such activity will be the 2009 International Test Conference (ITC), Nov. 2-6 in the Austin Convention Center, Austin, TX. Both companies will have booths at this year's ITC and ASSET's booth (No. 117) will feature a demonstration of SiliconAid's JTDdebugger. In addition, ASSET will feature the JTD[tm] debugger at Productronica in Munich, Germany, Nov. 10-13 (Hall A1, Stand 470).

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ASSET, through its ScanWorks platform, is applying the experience it has gained from two decades as a leading supplier of IEEE 1149.1 boundary-scan (JTAG) test tools to the development of open embedded instrumentation tools. The boundary-scan infrastructure that is embedded into chips and circuit boards is one of several technologies which can form the basis for an embedded instrumentation toolset. In recent years, ASSET has significantly enhanced ScanWorks beyond boundary-scan test with the addition of other embedded instrumentation technologies, including processor-controlled test (PCT) and tools for Intel® IBIST (Interconnect Built-In Self Test).

#### SiliconAid's SAJE Tool Suite

The SiliconAid JTAG Environment (SAJE) is comprised of tools (JTV, JTS, JTD) that focus on chip level JTAG needs for 1149.1, 1149.6, and now IEEE P1687. SAJE can be integrated into any major chip design process to handle JTAG requirements. The SAJE suite performs semantic checking, simulation-based verification, automatic test program generation (ATPG) and interactive debugging. Now the SAJE suite offers these functions in support of the IEEE P1687 standard. SAJESM can leverage design simulation information into automatic test equipment (ATE) and board test with test patterns and an interactive debugger (JTD).

#### About [ASSET InterTech](#)

ASSET InterTech is the leading supplier of open tools for embedded instrumentation for design validation, test and debug. The ScanWorks platform provides automation, access and analysis tools in one environment. Users can quickly and easily validate and test semiconductors, circuit boards or entire systems during every phase of a product's life, including design, manufacturing/repair and field maintenance. ASSET InterTech is located at 2201 North Central Expressway, Suite 105, Richardson, TX 75080.

#### About [SiliconAid Solutions, Inc.](#)

SiliconAid Solutions, Inc. was founded in 2001 and is headquartered in Austin, Texas. SiliconAid has a JTAG software development group and a world class design-for-test (DFT) consulting group supporting all electronic design automation (EDA) DFT tools. SiliconAid has developed a full suite of tools for JTAG creation, verification and debug. SiliconAid Solutions, Inc. is a privately held Texas corporation located at 9901 Brodie Lane, Suite 160217, Austin TX 78748.

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