

SCANWORKS® IBIST QPI VALIDATION TOOLKIT



Comprehensive yet easy-to-use test tools enable rapid validation of Intel® QuickPath Interconnect buses

TODAY'S TEST CHALLENGE

Getting to market quickly with products that incorporate high-speed signal paths such as Intel QuickPath Interconnect (QPI) has become a challenge. As these buses reach into the gigabit speeds, traditional validation and test methods are becoming increasingly costly and difficult. The addition of on-board Intel Interconnect Built-In Self Test (IBIST) technology provides a powerful alternative for testing and validating QPI-based designs.

THE ASSET INTERTECH SOLUTION

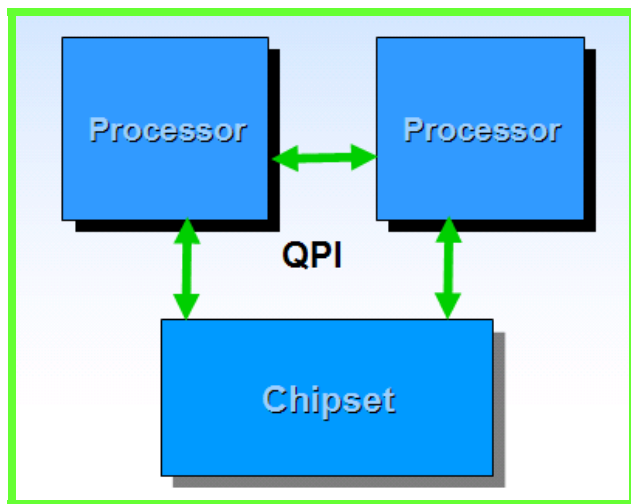
ScanWorks Intel® IBIST provides a comprehensive turn-key solution for interfacing and manipulating

embedded Intel IBIST technology. This powerful solution can reduce the cost of test and provide a more effective validation of high-speed buses compared to tradition test methods. The complete ScanWorks solution includes everything you need to immediately start testing your QPI-based designs. This includes software and hardware, customization services, training, and product support. The ScanWorks suite of IBIST test tools include:

- Pattern Generation and Checking
- Bit Error Rate Test (BER)
- Margining

SCANWORKS PATTERN GENERATION AND CHECKING

Pattern Generation and Checking (PG&C), the foundation for the ScanWorks BER and Margining tools, provides a basic yet capable tool for validating the transfer of rudimentary test patterns across platform I/O channels. Users can easily specify patterns, bit count and which links and lanes to test using pull down menus in the PG&C graphical user interface. A single lane can be tested, or ScanWorks can target all lanes on all QPI links concurrently. The result is a quick and easy test for determining bus connectivity and integrity.

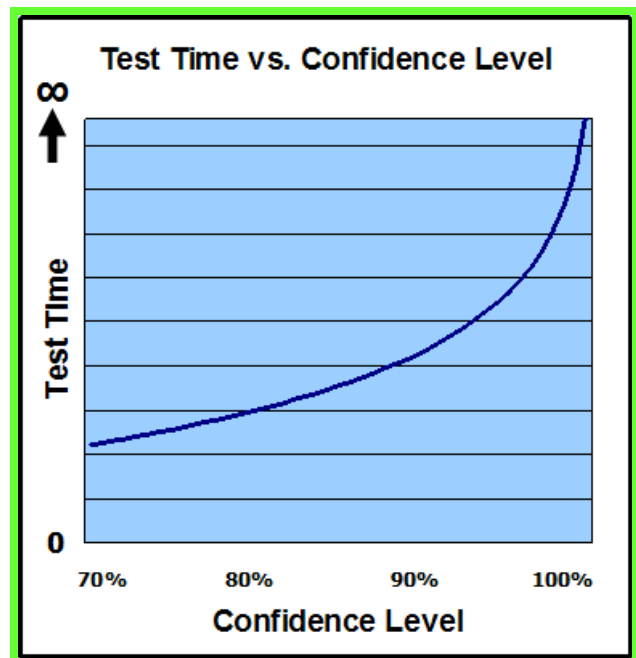


SCANWORKS BIT ERROR RATE TESTING (BER)

For a more robust analysis with quantitative results, ScanWorks BER tools can perform exhaustive testing with large data counts while accurately tracking total bit count and bit errors.

As with the PG&C test, ScanWorks BER can test a single lane, or all links simultaneously, accelerating design validation time as well as adding useful system stress during the test. In a typical Bit Error Rate test scenario, users can input a BER specification then run a comprehensive set of tests to determine the confidence level of meeting that specification. Achieve high

confidence in your QPI bus performance with ScanWorks BER.



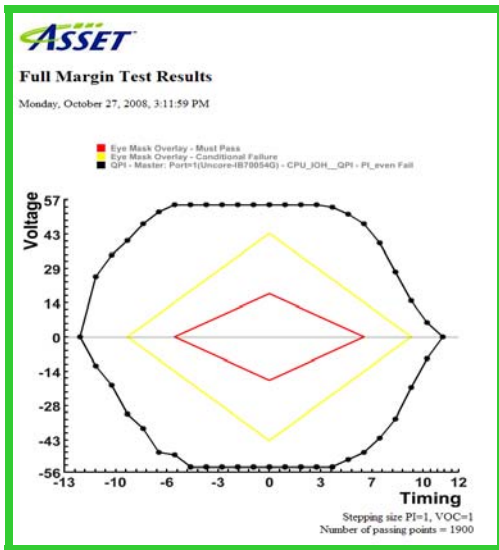
In addition, ScanWorks takes the guesswork out of running BER tests by providing a built-in calculator that estimates execution run time and confidence levels before the test is actually run.

SCANWORKS MARGINING TOOL

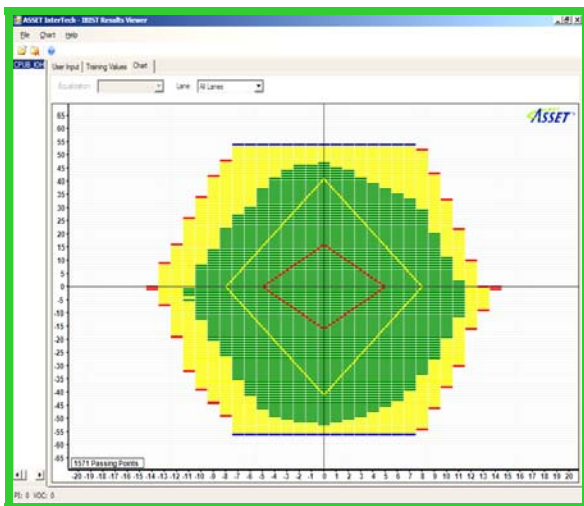
For further insight into your QPI links, ScanWorks offers easy-to-use pushbutton margining tools that generate text and graphical results for each high-speed channel.

ScanWorks can perform Full Eye analysis, or a quicker Cross Margin Test. The Cross test provides the user with information about the height and width of the eye, and runs in much less time than required for a Full Eye test. The tool can identify relative receiver performance margins when voltage and timing offsets are introduced. The ScanWorks user interface makes test setup and execution a snap. The user simply enters 'start', 'stop' and 'increment' values for both the voltage and time

axes. The tool automatically performs the tests and produces easy to read charts.

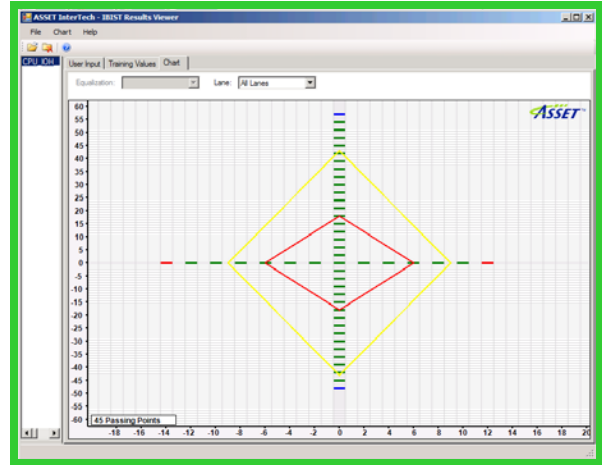


The results are provided in text, html, .csv, and an internal binary format. The html report is easily viewed in Internet Explorer. The text and .csv files can be post-processed by other tools for custom graphing solutions if required. The binary format can be read with the ASSET IBIST Results Viewer.



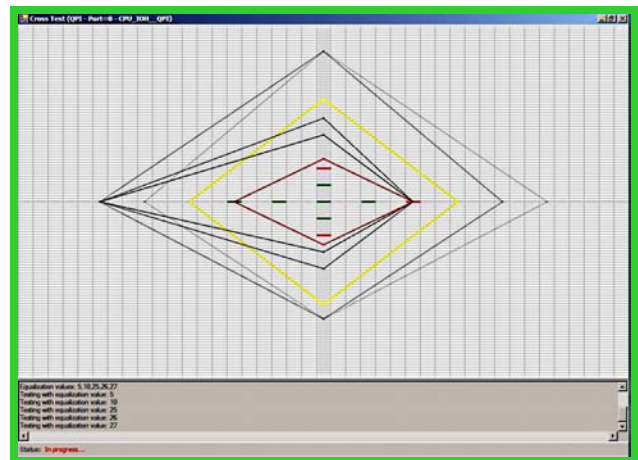
The Results Viewer provides an interactive UI allowing the user to see all details about the test setup, and interact with the output. The user can choose to plot a composite

of all lanes, or a chart of any single lane. Additionally the Results Viewer can export any view into either an image file or a PDF document for your records.



The ScanWorks Margining tool provides an excellent tool for visually characterizing bus design integrity. When used in conjunction with ScanWorks PG&C and BER, margining rounds out a powerful and efficient toolset for validating the QPI links on your platform.

In addition to standard margining tests, the equalization settings can be automatically adjusted by the test, providing a graphical view of link performance over a range of equalization settings.



A TURN-KEY SOLUTION FROM ASSET

Your total solution from ASSET includes everything you need to successfully deploy your custom solution and allows you to quickly begin validating your QPI links.

Your complete solution set includes:

- ScanWorks IBIST QPI-based platform validation application software and hardware
- On-site application tool training
- Customization services for your first product
- Software tools support

REDUCE YOUR RISK, GET STARTED TODAY

Let ASSET help you manage the risk of adopting and deploying this exciting new technology. Contact your local ASSET sales representative to get started with ScanWorks IBIST today.

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INTEL IBIST BASICS

WHAT IS INTEL IBIST?

Intel's IBIST (Interconnect Built-In Self Test) technology is a new test architecture that Intel has integrated into its next-generation processor chips and chipsets. It enables chip-to-chip interconnect testing and design validation of high-speed buses. This embedded "virtual instrument" can be used to test high-speed serial links such as QuickPath Interconnect (QPI).

WHY WAS INTEL IBIST CREATED?

With bus speeds in the multi-gigahertz range, traditional methods for measuring signal quality are becoming more difficult, less reliable, and more expensive. Intel IBIST was developed to provide engineers with an on-board virtual test instrument that can quickly deliver accurate measurement results, thereby reducing the cost of design validation.

HOW IS INTEL IBIST ACCESSED?

The IBIST test hardware is embedded in the chip and controlled externally. One method for accessing this hardware is via the IEEE 1149.1 (JTAG) Test Access Port (TAP) with its supporting Instruction Register and TAP Controller used as the IBIST control mechanism. Special 1149.1 instructions set up the tests, start them, determine when they complete, and read back failure information. A JTAG controller is connected to the eXtended Debug Port (XDP) connector on the unit under test. The ScanWorks boundary-scan system is the only JTAG platform that supports Intel IBIST.